Design of a Data Concentrator Card for the CMS Electromagnetic Calorimeter Readout

J. C. Silva[1], N. Almeida[1], V. Antonio[2], A. Correia[2], P. Machado[2], I. Teixeira[2], J. Varela[1][3],

[1]LIP-Lisbon, [2] INESC, Lisbon, [3]CERN

Abstract

The Data Concentrator Card (DCC) is a module that in the CMS Electromagnetic Calorimeter Readout System is responsible for data collection in a readout crate, verification of data integrity and data transfer to the central DAQ. The DCC should sustain an average data flow of 200 Mbyte/s. In the first part of the paper we summarize the physics requirements for the ECAL readout and give results on the expected data volumes obtained with the CMS detector simulation (ORCA software package). In the second part we present the module's design architecture and the adopted engineering solutions. Finally we give results on the expected performance derived from a detailed simulation of the module's hardware.
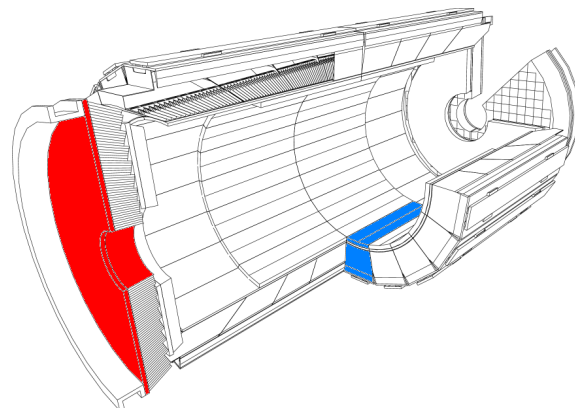
Figure 1: ECAL Endcap and Barrel geometry.

1. INTRODUCTION

The CMS Electromagnetic Calorimeter comprises approximately 77.000 crystals, organized in supermodules, in the barrel, and D-shaped modules in the endcaps (Figure 1). After amplification, the crystals signals are digitized (on the detector) and then transmitted to the counting room by high-speed optical links (800 Mbit/s). The upper level readout and trigger boards (ROSE boards) are designed to receive 100 optical links corresponding to the same number of crystals. Within each ROSE, data is stored in pipeline memories waiting for the first-level trigger decision (L1A), and in parallel it is used to compute trigger primitives that are sent to the regional calorimeter trigger system. Seventeen ROSE boards, filling a single VME-9U crate, handle the 1700 crystals in a barrel supermodule. Endcap crates are equipped with 14 readout boards. In each crate, the DCC is the common collection point of data from the ROSE boards, performing local event building and data transmission to the DAQ system.

If every crystal (ten data samples each) were read-out, something like 2.4 Mbytes would need to be handled for each triggered event. Due to several constraints this data volume is unacceptable. By agreement, the ECAL fraction of the DAQ bandwidth is constrained to be approximately 10% of the CMS total, bringing the average data rate per DCC to 200 Mbyte/s, for the maximum first-level trigger rate (100kHz). Techniques for obtaining optimal, efficient use of the allocated bandwidth, such as zero suppression and selective readout were studied using data generated with the CMS physics simulation and reconstruction software (ORCA-Object Oriented Reconstruction for CMS Analysis) [1].

This paper presents the DCC conceptual design, validated by a detailed modeling and simulation of the hardware using ECAL physics data as input. In section 2 we describe ECAL data generation process, section 3 presents the DCC conceptual design, section 4 describes the hardware modeling and finally in section 5 we present the hardware simulation results.

2. ECAL RAW DATA GENERATION

To motivate the best DCC design, the DCC hardware simulation was done using as input the expected ECAL data, for both Endcap and Barrel, as derived from a detailed detector simulation with ORCA version 4_4_0 optimized.

The simulation was performed for jet events, generated with transverse energy between 50 and 100 GeV, which are representative of the CMS triggered events. High luminosity ($L \sim 10^{34}/cm^2/s$) running was assumed, corresponding to approximately 17 pileup events per crossing. The pileup simulation is particularly important since a large fraction of the ECAL data volume results from the pileup minimum-bias events. Various scenarios of zero suppression and tower selective readout were applied to the data, allowing the evaluation of the DCC performance under different data rate conditions.

The target data volume for the ECAL is approximately 2KByte per DCC, which implies a reduction factor of ~20 on the total ECAL data volume. This data reduction can be achieved, without hurting the ECAL physics potential,

applying selective readout and zero suppression techniques to the data. Zero suppression implies the suppression of crystals with energy lower than a programmable threshold (typically, the threshold is set between zero and two r.m.s. of the electronics noise). Zero supression is complemented by a Selective Readout scheme based on the Trigger Towers transverse energy sum. The tower transverse energy is compared to two programmable thresholds, typically set at 1.0 and 2.5 GeV. Crystals in towers with E_T above the lower threshold, as well as crystals in towers surrounding a central tower with E_T larger the higher threshold, are selected for readout. As shown in figure2 the average data volume per DCC is reduced from ~3.3KB to ~1.3KB when Selective Readout is used together with a milder Zero Supression. On the other hand, the choosen organization of the readout channels garanttees that the DCC event size is constant in the whole detector, as it is shown in figure 2.
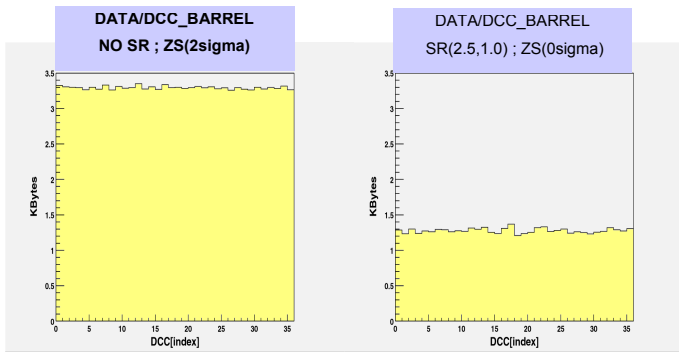

Figure 2: Event size per DCC in the barrel (without and with SR).

Figure 3 shows the total ECAL event size for various combinations of the Zero Suppression and Selective Readout thresholds. The target value of 100 kBytes is easily achieved using very low thresholds and consequently without loosing significant physics data.
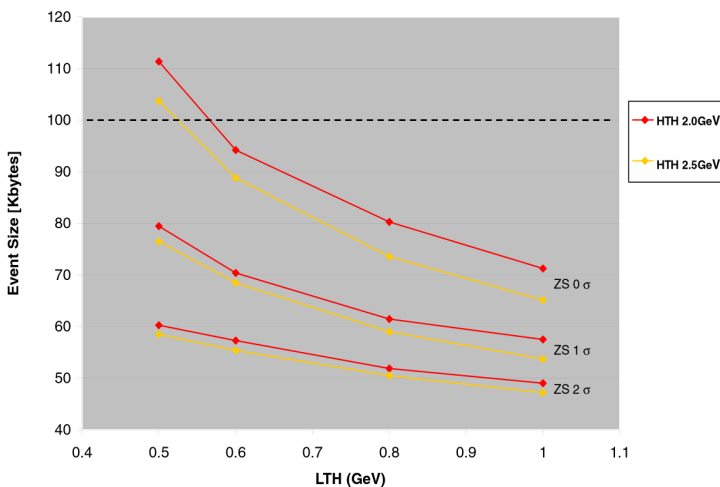

Figure 3: Zero Suppression and Selective Readout Scenarios

3. DCC CONCEPTUAL DESIGN

The DCC is implemented, or partitioned, in two p.c. boards: a main 9U board (DCC Mother Board) and a 6U transition board (DCC Input Board). In this way the interconnection at the crate level is simplified. The DCC Input Board contains 17 input links (point to point links), input memories and respective handlers. The DCC Mother Board houses the Event Builder, the output memories and the output links. Two output links are included, one transporting ECAL data to the main DAQ, and another transporting only trigger data to the trigger monitoring system. The DCC can be accessed via the VME bus, for initialization, board monitoring and data readout in spy mode.

The Event Builder is the most important and complex part of the DCC. The main purpose of this block is to assemble the data fragments arriving from 17 ROSE boards in a single data packet (DCC event), and to store it in the output memories ready for transmission. A number of checks and complementary operations are performed by the Event Builder. It verifies the integrity of the input data fragments, checks the event fragments synchronization, monitors the occupancy of the input and output memories and generate "empty events" on special error conditions. A complete description of the Event Builder design is described on [2].

Some technological choices have been made to fit the DCC performance requirements. All inputs use LVDS Channel Link that insures quality and reliability while reducing the interconnection pins. The Input Handlers, Event Builder and Output Handlers are implemented using re-programmable logic circuits (ALTERA). The output ports have been defined to be S-Link-64 compatible, the protocol adopted for transmission to the central DAQ. The DCC Internal Data Bus, bridging the input memories to the output link, is being now designed to have a throughput of 528MB/s.

4. DCC MODELING ...

The modeling of the DCC hardware was done using the Rational Rose Real Time software.

From the DCC conceptual design three main classes emerge: the Input Handler, the Event Builder and the Output Handler. These classes were modeled on so called "capsules" that reproduce the behavior of the three classes using a real time simulation. To complete the modeling two more classes are needed, the clock emulator and L1A trigger emulator and a Data capsule that uses the ECAL raw data as input. Each of these classes allows us to model, configure and modify the main parameters of the DCC design.

The Input Handler capsule, controls the occupancy of each input memory, allows to modify the segmentation of each input memory (technically called iFIFO's) and to set up the handshake timing.

The Event Builder performs all the data checks, builds the DCC event from the different selected inputs and updates the status and error registers.
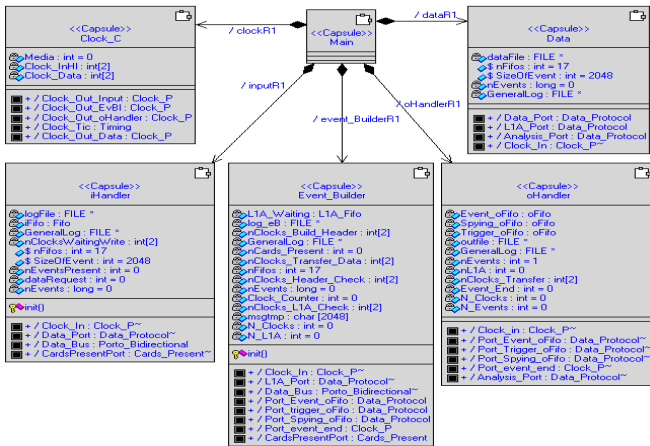
Figure 4: DCC modeling overview

The Output Handler controls the communication with the output link and sends each entire event to the DAQ.

The Data capsule reads from a file the input data. The data used on the modeling and simulation is the physics data generated by the ORCA software, as referred before.

The Clock capsule controls the clock frequency and the L1A trigger generation.

5. ...AND SIMULATION RESULTS

In this chapter we will present the first (preliminary) results from the simulation of the DCC conceptual design.

Two simulated data sets were applied to the Data capsule. Both data sets were obtained with selective readout high threshold set to 2.5GeV and low threshold set to 1GeV.

Zero suppression thresholds of 1σ and 0σ were used. The corresponding ECAL event sizes were 53 Kbytes and 65Kbytes, respectively, per triggered event.
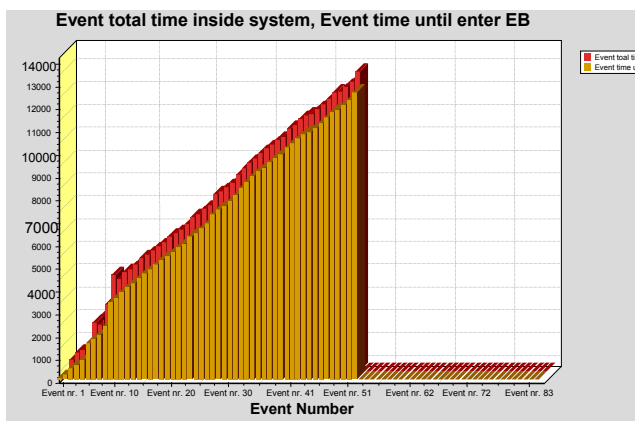

Figure 5: An example of input memory overflow. The plot shows the event time within the system as a function of the event number.

Various simulations for different options of the DCC Internal Bus bandwidth, Event Builder processing speed and Output Link speed were performed. The maximum simulated DCC bandwidth was 320MB/s. For each condition, the occupancy of the input and output memories and the event latency inside the DCC were investigated. Figure 5 shows an example of a simulation were an overflow of the input memories is observed (simulated bandwidth was 160 MB/s).

Simulation results showed that, relatively to the 320 MB/s deled design, either the input memory or the processing speed needs to be increased. For 65Kbytes per triggered event we estimated an overflow probablilty of 5.10^{-8} (figure 6). This corresponds to an overflow condition every 3 min which is far from acceptable (even more if we aim ~100Kbytes per event). One must notice that no trigger rules have been appiled to the simulation inputs, and therfore this results are "whorst case" figures. Further results are expected in the near future for the aimed bandwidth of 528MB/s.
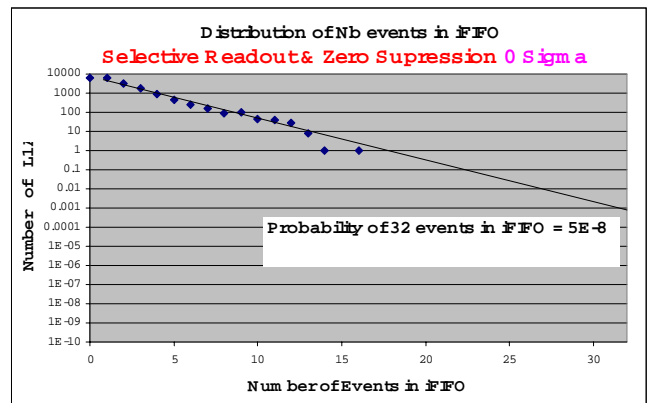

Figure 6: iFIFO overflow probability.

6. CONCLUSIONS

Detailed ORCA simulations showed that a combination of Selective Readout and Zero Suppression techniques reduces the CMS-ECAL average data to the target value (100KB/event) without loosing significant physics data.

A conceptual design of the ECAL data concentrator was developed aiming a data throughput of 528MB/s.

Simulations of the DCC hardware, using physics data as input, were used to guide the design. Further simulations are undergoing to validate the final design choices.

7. REFERENCES

[1] Selective Readout in the CMS ECAL, T. Monteiro, Ph. Busson, W. Lustermann, T. Monteiro, J. C. Silva, C. Tully, J. Varela, in Proceedings of 'Fifth Workshop on Electronics for LHC Experiments', Snowmass, Colorado, USA, 1999.

[2] Description of the Data Concentrator Card for the CMS-ECAL, Jose C. Da Silva, J. Varela, CMS NOTE in preparation.