Production and Test of the ATLAS Hadronic Calorimeter Digitizer

S. Berglund, C. Bohm, K. Jon-And, J. Klereborn, M. Ramstedt and B. Selldén

Stockholm University, Sweden October 2001

mank@physto.se

Abstract

The pre-production stage of the full-scale production of the ATLAS TileCal digitizer started during the summer 2001. To be able to ensure full functionality and quality, a thorough test scheme was developed.

All components are radiation tested before start of production. After mounting components all digitizer boards will pass burn-in and tests in Stockholm. Custom designed software ensures that full functionality is maintained. A record of the test results is stored in a repository accessible via Internet for future reference. Similar test software is later used at the site of full electronics assembly in Clermont-Ferrand cross referencing their results with the test data entries.

I. Introduction

A. The Digitizer

Stockholm University is responsible for design, manufacture and quality control of the digitizing unit of the ATLAS Hadron Calorimeter [1]. The calorimeter is often called TileCal because of its interleaved iron and scintillating tiles. Heavy particles interact with the iron tiles and form showers of charged particles that produce light in the adjacent scintillating tiles. This light is transferred to an array of PMTs via wave length shifting fibers. The PMTs and all the front-end electronics are contained in so called drawers at the base of the calorimeter modules. There are 32 or 45 PMTs in a drawer depending of its position in the detector. The PMTs are connected to 3-in-1 cards [2] that shape and amplify the pulses. The 3-in-1 cards are in turn connected to digitizers that sample the pulses.

Each digitizer board serves six 3-in-1 channels. There are two TileDMUs, a specially designed controller and readout ASIC, on each digitizer board. Data from the TileDMUs are read out via a G-link based interface board (Fig.1). The TTC-system [3] delivers timing and slow control to the interface board via fibers. The TTC signal is then distributed to the digitizer boards. A drawer contains eight or six digitizer boards depending on its placement in the detector with the interface board placed in the middle. When a digitizer board at the far end of the drawer is read out, data and TTC signals pass through lines with no active components on intermediate boards. Thus, any malfunctioning components on a digitizer board will only corrupt its own data.

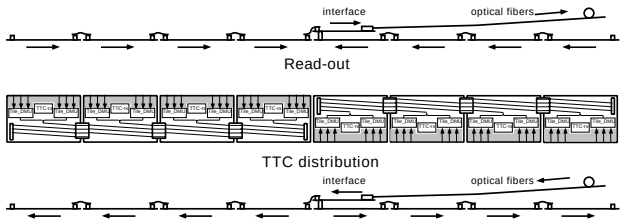

Fig. 1 The data flow along a chain of eight digitizer boards

The main components of the digitizer board are the ADCs, the TileDMUs and the TTCrx. The ADCs are ten bits converters. To provide an effective dynamic range of 16 bits there are two ADC channels per PMT channel digitizing the two signals from the 3-in-1 card. These are high and low gain signals with an amplification ratio of 64.

Data from all channels are stored temporarily in pipeline memories in the TileDMUs. When the first level trigger validates an event the TileDMU will choose the appropriate gain, according to the amplitude of the signal, format the data and store it in a readout buffer. Functions for tests and calibration are also part of the TileDMU.

B. Production of the digitizer

In order to ensure the quality of the full production, the pre-production has been made as close to the real production as possible including all steps: manufacture, mounting, burn-in, tests and logistics. All design is now almost completed and final manufacturer and assembly-company will soon be chosen. A few small design modifications will be made to take care of a yield problem that was discovered during pre-production when mounting a high-density surface connector.

The production and the test routines will also be improved to implement some additional features suggested by the pre-production experience.

In the pre-production 86 boards were manufactured and assembled with a surprisingly high fault rate level of about 35 %. The sources of these faults have been investigated and are to a large extent understood. About 20% failed due to badly soldered data connectors. To fix this the connector surface mount pads will be modified. About 5% failed due to malfunctioning TileDMUs. This number was expected since the TileDMUs of the pre-production were not fully tested before delivery. The remaining 10% failures are being investigated in more detail. When this is done there will be a final product readiness review (PRR) and the mass production will start, most likely in November this year.

II Tests

A. Test procedure

To ensure the quality and functionality of the digitizer boards, tests are made at several checkpoints along the production process. Components used on the board are required to be radiation tolerant and are tested according to the ATLAS recommendations [4]. Unassembled boards are checked for breaks and shorts at the board manufacturer.

Functionality of the TileDMUs are tested before and after packaging i.e. just before they are sent for assembly. After mounting the components the boards will be superficially tested before delivery to the burn-in and test facility at Stockholm University. The burnt in boards are thoroughly tested and then sent to the drawer assembly plant at Clermont-Ferrand for assembly and final tests.

B. Test Bench Setup

A test drawer has been set up for the purpose of production tests. This set-up is quite similar to a final ATLAS drawer. A RIOII VME processor is used as readout buffer and a TTCvi module as a source of clocks and for configuration of the digitizer boards (Fig. 2). These tests are all controlled by RIOII software. The main electronic parts in the test drawer are the 3-in-1 system, the digitizer boards and the interface link board.

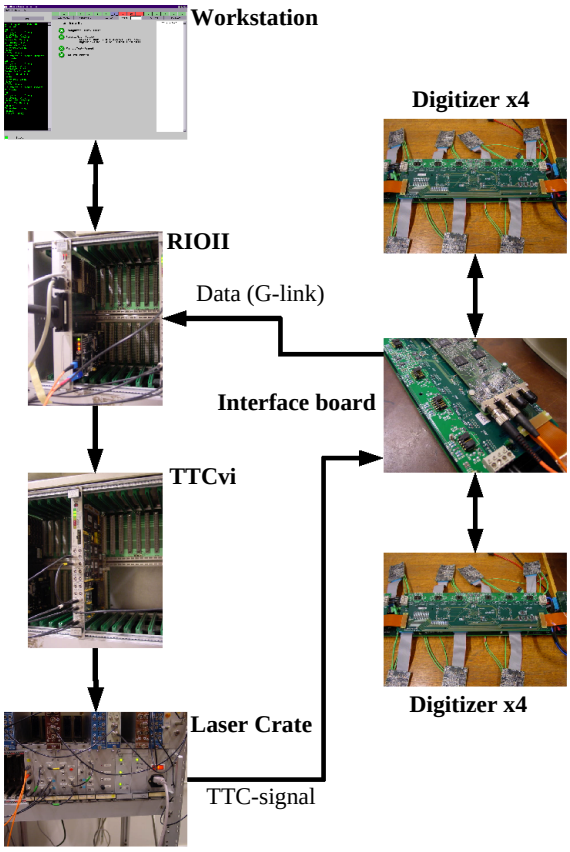

Fig. 2 Schematic picture of the test bench components and signal flow

C. Radiation Tests

Most active components have been tested for radiation tolerance and the remaining tests will take place before the final PRR and start of production.

According to ATLAS requirements the digitizer should, without damage, resist the following doses: 3.5 krad ionizing radiation and $2.3*10^{12}$ 1MeV eq neutrons/cm^2. Corresponding numbers for components containing bipolars are 17.5 krad and $2.3*10^{12}$. These figures include the appropriate safety factors. Tests for single event effects (SEE) [4] should also be performed. With one exception (TTCrx), none of the digitizer components have a formal specification on radiation tolerance from the manufacturer. Several tests have therefore been made to select components with the best radiation tolerance, which also are acceptable from the price/performance point of view. During the process several types of components have been rejected.

The full installation will contain around 22000 ADCs. About 40 samples from various batches have been radiated up to 50 krad and a subsample even up to 100 krad. Our result is that all samples stand 30 krad and some even 100

krad of ionizing radiation. 18 samples have been exposed to $7.5*10^{12}$ 1 MeV eq n/cm^2 with no malfunction detected.

Between 8 and 20 samples from each of the digitizer CMOS circuit have been exposed to 10 krad ionizing radiation and $5*10^{12}$ 1 MeV eq n/cm^2. No errors were detected.

Only one sample of the TileDMU (CMOS) has been tested with radiation levels as above. For that sample no malfunction was detected. Eight more will be tested shortly. A special test bench that tests the TileDMU has been developed for the study of transient errors.

In the near future we plan to make SEE tests on system level using a 170 MeV proton beam. Also here we need to develop a dedicated test bench.

D. Test of the PCB

The vendor will test non-assembled boards for circuit breaks and short circuits. Faulty boards are rejected. After assembly the boards are visually inspected for obvious mistakes and tested for power short circuits. A superficial test using a dedicated test bench, similar to the one that will be used in the board SEE tests, is planned. A more thorough test is made after the burn in.

E. Test of data and TTC connector

In a drawer four digitizers are read out in a chain to the interface board. Data from the TileDMU, and data and the TTC signals from boards further away from the interface will pass through a high-density surface mounted connector on each digitizer board. A faulty connector can therefore generate errors when passing signals from another board. Before starting the full test procedure the connectors must be thoroughly tested. This will be done using three fully functional boards as reference boards. The board to be tested is placed close to the interface board so all connector pins are used. This is not the most efficient method since one would like to test more than one board at a time in the drawer. By testing the connector in a special connector test tool, much time can be saved. Such a tool is being developed.

F. Functionality Test

After burn-in and test of the data connector, the functionality of the entire board will be tested. The only way to do this is to first configure the digitizers and the 3-in-1-system and then read out data. This is done simulating the TileCal front-end electronics environment. It can be difficult to identify the error in faulty boards by analyzing the data since most components interact. However, if a board passes the test this will guarantee that ATLAS functionality is maintained [5].

First of all the TTCrx is tested to verify that the proper clocks are generated and that commands can be transferred to the digitizers. The TTC single error and double error flags [3] are monitored to verify the TTC transmission quality. This test also verifies that the TileDMUs are able to read out.

The next step is to exercise the TileDMU verifying that all programming parameters can be set. The memory is tested with different bit patterns. This is done using a test mode where all data are generated internally.

Test pulses are produced by the 3-in-1 system to verify that none of the ADC bits are stuck at one or zero. The pedestal RMS is then calculated to estimate the noise level. The pedestal levels are examined to determine whether a component adjustment is needed. An on-board DAC is used to scan part of the dynamic range to determine the linearity. All readout is protected by data word parity and cyclic redundancy check. Errors are not accepted.

G. History files and QC-Sheet

For all digitizer boards the history of modifications, test data and some characteristics are stored in a history file. These are auto-generated from the software and are stored in HTML/ASCII-format for accessibility. When a board has passed all tests a quality control sheet is generated in HTML-format for easy access by the collaboration.

H. Software

The test software is split into two programs, the configuration and readout software (CRS) and the graphical user interface and analysis software (GUI). The CRS is running on the RIOII in the same crate as the TTCvi. It controls the configuration of the digitizers and the 3-in-1 system via the TTCvi and receives data from the digitizers via an S-link PCI card attached to the RIOII. This part is called Coot-Boot. The GUI, called Baltazar, is running on a workstation (e.g. Windows NT PC) communicating with Coot-Boot via TCP/IP. The idea behind Baltazar is to implement a user-friendly interface making it easy to operate the test bench after a short introduction. The software automatically generates the history report files and makes them accessible from WWW.

The GUI is coded in JAVA to achieve platform independence. JAVA is also easily available and well

documented on the web. Baltazar has also been used as reference software in TileCal test-beam. The data analysis is made by Baltazar requiring all data (~900kByte/run) to be transferred from Coot-Boot. This takes only a few seconds. The JAVA code makes the analysis sufficiently fast.

III. Conclusions

The TilCal digitizer is soon ready for full production. In order to assure fully tested boards and a high production yield many test procedures have been developed and inserted in different places along the production chain. This has required the development of different hardware and software test benches.

However there are still a few tests that must be improved. This will be done before the final production.

IV. Acknowledgements

We would like to thank J. Molnar and A. Fenyvesi from Atomki in Debrecen for their help making the neutron irradiation of our components.

V. References

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