

# DeltaStream : A 36 channel low noise, large dynamic range silicon detector readout ASIC optimised for large detector capacitance.

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## Abstract

DeltaStream is a 36 channel pre-amplifier and shaper ASIC that provides low noise, charge to voltage readout for capacitive sensors over a large dynamic range. The chip has been designed in the DMILL BiCMOS radiation tolerant technology for the CMS Preshower project. Two gain settings are possible. High gain (HG), has gain  $\sim 30$  mV/MIP (7.5 mV/fC) for a dynamic range of 0.1 to 50 MIPS (0.4 fC – 200 fC) and low gain (LG), has gain  $\sim 4$  mV/MIP (1 mV/fC) for a dynamic range of 1 to 400 MIPS (4 fC – 1600 fC). The peaking time is  $\sim 25$  ns and the noise has been measured at  $\sim \text{ENC} = 680 e + 28 e/\text{pF}$ . Each channel contains a track & hold circuit to sample the peak voltage followed by an analog multiplexer operating up to 20 MHz. The response of the signal is linear throughout the system. The design and measured results for an input capacitance  $< 52$  pF are presented.

## I. INTRODUCTION

DeltaStream has been developed within the framework of the CMS Preshower development [ 1 ]. It provides a simple analog signal processor, which can be used for the multi-channel readout of silicon sensors with strip/pad capacitances up to 55 pF per channel. The prime motivation for the development was to provide the signal processing necessary for the production testing of the CMS Preshower silicon

sensors. DeltaStream incorporates the same analog design specifications as needed for the CMS Preshower front-end electronics foreseen for LHC (PACE) but avoids its complexity.

The main features of DeltaStream are dc coupling to the sensors, sensor leakage current compensation, two dynamic range settings with linear response over the ranges 0.1-50 MIPs and 1-400 MIPs,  $S/N > 10$  (for 1 MIP in the 0.1-50 MIP range), single channel or multiplexed analog readout with multiplexing frequency up to 20 MHz, radiation tolerance up to 10 Mrads(Si) of ionising radiation and  $4 \times 10^{13} \text{ ncm}^{-2}$ .

## II. DELTASTREAM DESIGN

The DeltaStream channel architecture is shown in Figure 1. The architecture is similar to that of the AMPLEX family of ASICs [ 2 ] but differs in its analog properties and speed of multiplexed readout.

Each of 36 identical channels include a charge sensitive pre-amplifier (Delta) with leakage current compensation (LCC) [ 3 ] followed by a CR-RC<sup>2</sup> shaper and a track & hold circuit. The outputs from the 36 channels feed into an analog multiplexer. The multiplexer serialises the sampled analog voltage from each channel into a stream of analog values. The analog stream is then buffered to the outside world through a single analog output.

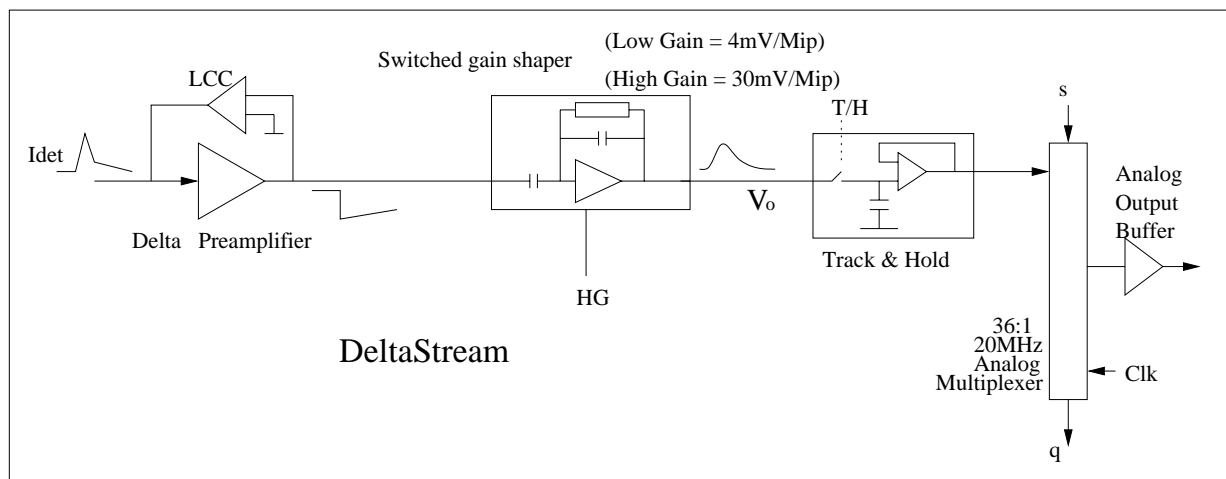


Figure 1 : The DeltaStream channel architecture.

The Delta pre-amplifier provides charge to voltage conversion producing a “step like” function with a fast initial response and a slow tail back to the operating point. Delta has a bipolar input device with optimised emitter area with respect to noise for highly capacitive sensors (~55 pF) and expected radiation levels of 10 Mrads(Si) of ionising radiation and  $4 \times 10^{13} \text{ ncm}^{-2}$ .

The LCC enables dc coupling to the sensor and virtual insensitivity to sensor leakage current up to 150  $\mu\text{A}$  (well beyond the requirements of most modern day silicon sensors).

A switched gain shaper provides noise filtering and offers the possibility of two gain settings and hence two dynamic ranges. These are:

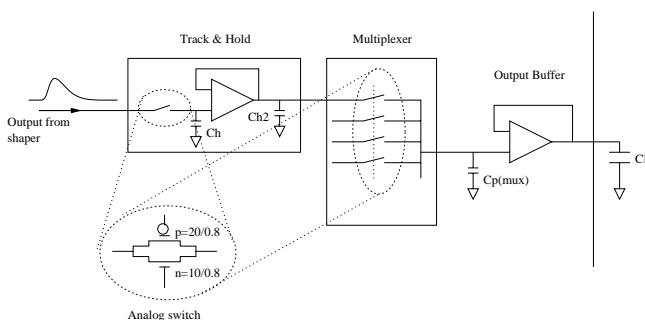
- High gain (HG) ~30 mV/MIP, dynamic range 0.1-50 MIPs
- Low gain (LG) ~4 mV/MIP, dynamic range 1-400 MIPs

The peaking times in the two gains have been matched to 25 ns.

The Delta pre-amplifier, LCC circuit and switched gain shaper were first developed on a demonstrator chip. Details of the design, optimisation for noise with respect to input capacitance and irradiation and the demonstrator chip results before and after irradiation can be found in [ 3 ].

In DeltaStream a track & hold circuit (shown in Figure 2) is implemented after the shaper which comprises a switch, storage capacitor (Ch) and an amplifier implemented as a unity gain buffer. The switch has been designed as a complementary CMOS switch with W/L values chosen to have an almost constant “on” resistance with respect to signal value in order to maintain dynamic range and linearity. The time constant of the switch plus Ch is 620 ps allowing the voltage on Ch to track effectively the output from the shaper.

Also shown in Figure 2 is the multiplexer which is designed to run a 20 MHz. A static shift register is used to sequentially turn on and off switches connecting each channel output to the output buffer. The same complementary switch design as used in the track and hold circuit is used to maintain linearity.

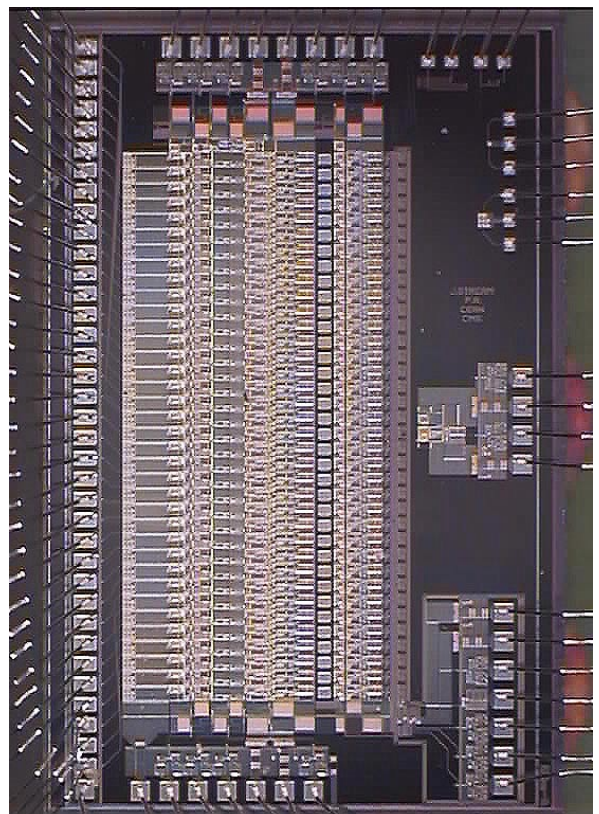


**Figure 2 : The track & hold plus multiplexer circuit.**

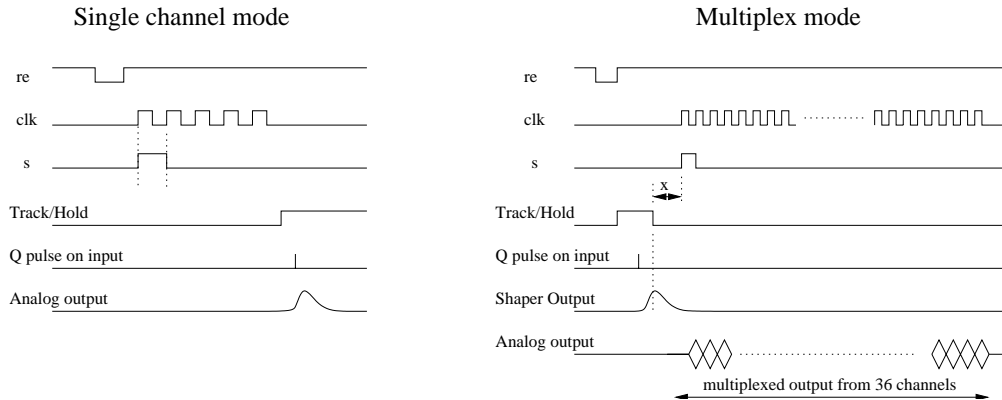
The drain capacitance of one analog switch is 42fF. The output node of the multiplexer is connected to each channel by a metal line, which has a calculated capacitance of 462 fF.

The total parasitic capacitance of the multiplexer output node including the metal interconnect (462 fF) and drain capacitance of each analog switch (42 fF each) is ~ 2 pF . This is represented in Figure 2 by  $C_{p(mux)}$  and is naturally much larger than the parasitic capacitance associated with each multiplexer input. Since the signal voltage difference from one channel to the next may be as large as 1.6V, it is possible that charge stored on Ch couples back to the multiplexer input of the next selected channel causing distortion when multiplexing at high speed. This problem can be reduced by increasing the drive capability of the track & hold unity gain buffer but this increases power consumption. Another option (used in this design) is to deliberately load the track & hold output with a capacitance matched with  $C_{p(mux)}$  therefore eliminating the capacitive imbalance. Ch2 in Figure 2 represents the additional capacitor.

Figure 3 shows a photograph of a bonded DeltaStream chip. The 36 channel inputs are located on the left and the analog readout buffer is the central block on the right. The power supply is delivered to the top and bottom as well as bias currents and voltages. Digital signals for the control of the multiplexer enter DeltaStream in the lower right hand section. The digital circuits have their own power supply and guard-ring. The overall dimensions of the chip are  $3.115 \text{ mm} \times 5.106 \text{ mm} = 15.9 \text{ mm}^2$ .



**Figure 3 : Photograph of DeltaStream.**



**Figure 4 : Timing diagrams for operating DeltaStream in "single channel mode" and "multiplex mode."**

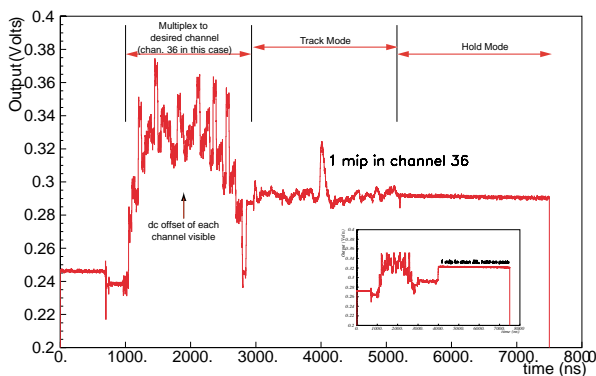
### III. MEASURED RESULTS

All measurements have been made using electrical test pulses to stimulate the input. An input charge of 4 fC is used to represent the 25000 e rms produced by 1 MIP traversing a 300  $\mu\text{m}$  thick fully depleted silicon sensor. The inherent parasitic capacitance of the measurement board has been measured to be  $C_i = 13.2 \text{ pF}$  (+- 0.8 pF). Additional capacitance ( $C_{\text{Add}}$ ) was introduced to the inputs (up to 39 pF) to achieve a total input loading capacitance of  $\sim 52.2 \text{ pF}$ .

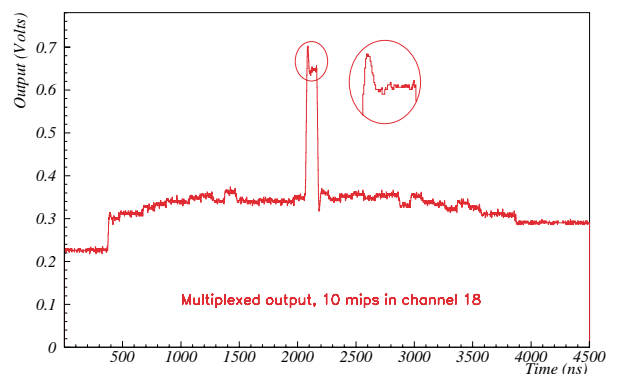
DeltaStream can be operated in two modes with respect to the multiplexer. These two modes are **Single channel mode** and **Multiplex mode**.

Figure 4 shows a timing diagram for the control signals in both modes of operation. Figure 5 shows the analog output in single channel mode. In this case the last channel (36) was selected and hence the dc values of channels 1-35 are evident during the channel selection. Channel 36 then remains connected and a 1 MIP signal is clearly seen during "track mode". The insert shows the track & hold circuit maintaining the peak of the signal response.

Figure 6 shows the analog output in multiplex mode. A signal of 10 MIPs was injected onto channel 18 and sampled on the peak before multiplexing at 20 MHz. A zoom of the channel containing the signal shows an initial overshoot of the signal value by the output buffer. The signal settles within the first half period of multiplexing, external sampling of the signal value should therefore be done towards the end of the second half period when the output has settled.



**Figure 5 : The DeltaStream analog output in single channel mode.**

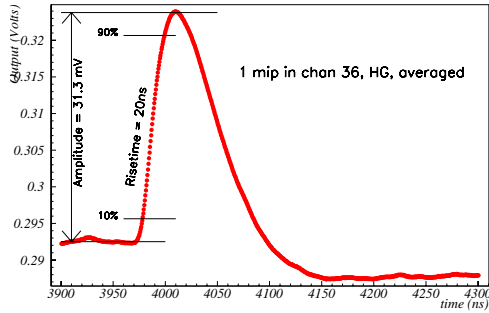


**Figure 6 : The DeltaStream analog output in multiplex mode.**

In single channel mode, the multiplexer can be used to switch through to one particular channel and stay there indefinitely. Keeping the track & hold circuit in "track" mode enables the full pulse shape from the shaper to be observed.

Multiplex mode samples first the signal on the peak and then multiplexes through all 36 channels.

The channel to channel spread in dc values was measured as 91 mV peak to peak with a standard deviation around the mean of  $\sigma = 21 \text{ mV}$ .

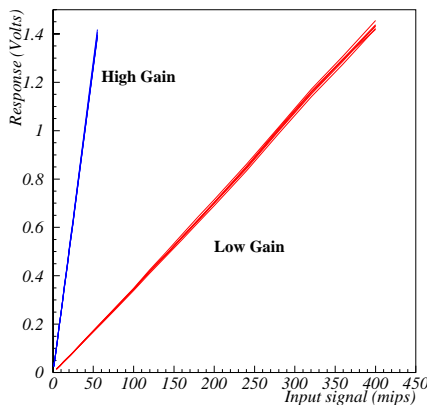


**Figure 7 : The signal response for 1 MIP in high gain.**

The signal response is best seen in Figure 7. The rise time (as measured from 10% to 90%) of the signal amplitude was independent of signal size within the dynamic range. Measurements showed mean rise times in LG of 14.5 ns with  $C_{Add} = 0$  pF and 17.5 ns with  $C_{Add} = 39$  pF. In HG the mean rise times were 18.9 ns with  $C_{Add} = 0$  pF and 21.8 ns with  $C_{Add} = 39$  pF. The channel-to-channel variation was  $\sim 1.5\%$ .

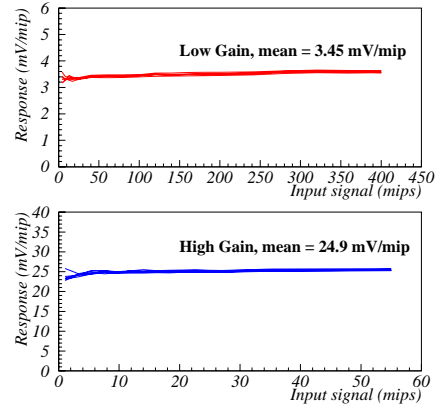
The dynamic range for  $C_{Add} = 39$  pF is 50 MIPs in HG and 400 MIPs in LG as shown in Figure 8. The gain (measured by the mean of straight line fits) was 4.62 mV/MIP in LG with  $C_{Add} = 0$  pF reducing to 3.45 mV/MIP with  $C_{Add} = 39$  pF. In HG the mean gain was 33.12 mV/MIP with  $C_{Add} = 0$  pF reducing to 24.9 mV/MIP with  $C_{Add} = 39$  pF. The channel to channel variation of the gain calculated as the standard deviation ( $\sigma$ ) around the mean was  $\sim 3.5\%$  (exact values given in Table 2).

The linearity in both LG and HG is shown in Figure 9 which plots the peak amplitude divided by the input signal in MIPs against the input signal in MIPs. A straight horizontal line would show perfect linearity. The integral non-linearity (INL) (measured as the standard deviation from a straight line fit of the data in Figure 8 and expressed as a percentage of the operating range) is 0.42% for LG and 0.21% for HG measured over the specified ranges of 400 MIPs (LG) and 50 MIPs (HG).

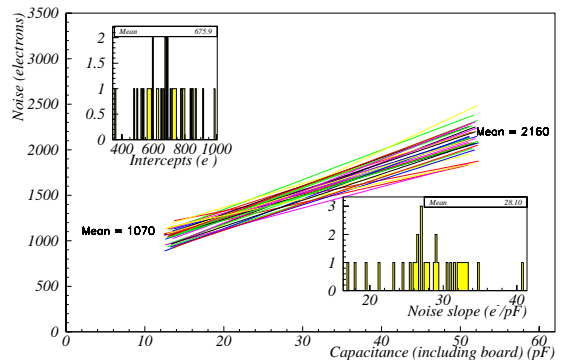


**Figure 8 : The measured peak amplitude for 6 channels in LG and HG for input signals up to 400 MIPs.**

Figure 10 shows the noise measured against total input capacitance for each channel in HG and the corresponding straight line fit. The mean fit for all 36 channels showed an ENC of  $676 e + 28 e/pF$ .



**Figure 9 : The peak amplitude against peak amplitude divided by input charge in MIPs .**



**Figure 10 : Measured noise as a function of the total input capacitance for all 36 channels.**

The power consumption for each module and the entire chip is given in Table 1. The gain-bandwidth required by the track & hold op-amp. is less in multiplex mode compared to single channel mode. Increasing the distance in time marked "X" in Figure 4 allows the track & hold power consumption to be reduced in multiplex mode.

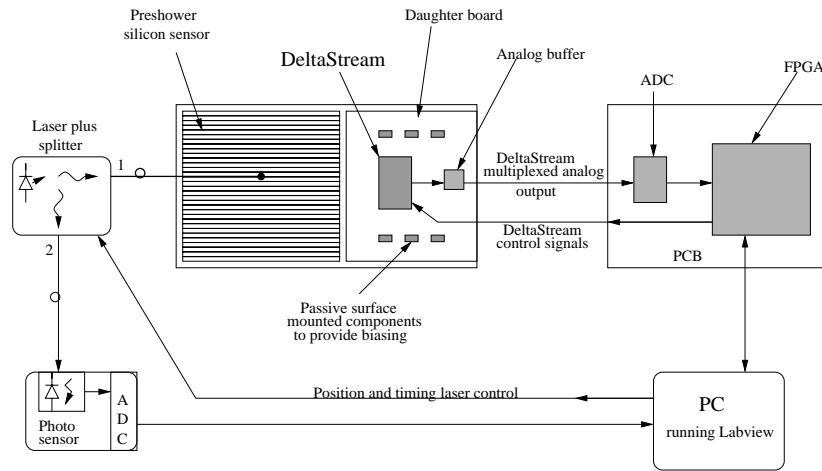
Delta pre-amp + LCC	5.12 mV / ch.
Shaper	5.6 mV / ch.
Track & hold (single chan. mode) <sup>a</sup>	8 mW/ ch
Track & hold (multiplex mode) <sup>b</sup>	950 $\mu$ W / ch
Output Buffer	10 mW
Total Power consumption	684 mW <sup>a</sup> 430 mW <sup>b</sup>

**Table 1 : The DeltaStream power consumption.**

A summary of the principle results from the DeltaStream measurements is contained within Table 2 .

Measurement type & additional Capacitance	Low Gain			High Gain		
	pp	mean	$\sigma$	pp	mean	$\sigma$
Rise time (0 pF)		14.5 ns	0.21 ns		18.9 ns	0.27 ns
Rise time (39 pF)		17.5 ns	0.23 ns		21.8 ns	0.38 ns
Gain (0 pF)		4.62 mV	159 $\mu$ V		33.12 mV	1.16 mV
Gain (39 pF)		3.45 mV	112 $\mu$ V		24.90 mV	925 $\mu$ V
DC Baseline (0 pF) (Channel to channel)	91 mV		21 mV	69 mV		18mV
Linear range & INL (39 pF)	400 MIPs (1600 fC) with INL = 0.42%			50 MIPs (200 fC) with INL = 0.21 %		
Noise (HG)	ENC = 676 e + 28 e/pF					

**Table 2 : Summary of DC levels, gain over the full dynamic range, rise time and noise. The results of all 36 channels are included.**



**Figure 11 : Preshower silicon sensor laser measurement system using DeltaStream.**

#### IV. APPLICATION EXAMPLE

DeltaStream can be used for the analog signal processing of silicon strip/pad sensors that require low noise and large dynamic range. The application foreseen within the CMS Preshower development is a silicon sensor measurement system. The Preshower sensors are to be produced in a number of regional centres around the world. In order to maintain consistency between test methods and results during the production phase a common measurement system is required. Figure 11 shows a block diagram of the system. A laser is used to generate pulses of light with wavelength 1060 nm. A passive “splitter” is used to divide the light into two parts and fibre optic cables direct the light to well focused regions on the sensor strips and to a photo sensor. The charge from the strips are readout by DeltaStream and digitised by an ADC. The signal from the photo sensor is also digitised and the two results compared on a PC.

#### V. CONCLUSIONS

The design and results of DeltaStream have been presented. DeltaStream contains 36 identical channels of pre-amplifier, 25 ns peaking time shaper and a track & hold circuit. The analog signal from each channel is multiplexed to a single analog output at frequencies up to 20 MHz. DeltaStream has a selectable gain (LG and HG) offering a

linear response over 2 dynamic range settings of 0.1-50 MIPs (HG) and 1-400 MIPs (LG). DeltaStream has been designed to readout large silicon strip/pad sensors imposing up to 55 pF of input capacitance per channel. The chip can be dc connected to the sensor and is unaffected by sensor leakage current up to 150  $\mu$ A per channel.

#### VI. REFERENCES

- [ 1 ] The CMS collaboration *The Calorimeter Project Technical Proposal* (CERN/LHCC 94-43 LHCC/P2, 1994)
- [ 2 ] E.Beuville, K.Borer, E.Chesi, E.Heijne, P.Jarron, B.Lisowski, S.Singh *AMPLEX, A low noise, low power analog CMOS signal processor for multi-element particle detectors*. Nuclear Instruments & Methods in Physics Research A 288 (1990) 157 North Holland
- [ 3 ] P. Aspell, D.Barney, P.Bloch, P.Jarron, B.Lofstedt, S.Reynaud, P.Tabbers *Delta: A charge sensitive front-end amplifier with switched gain for low-noise, large dynamic range silicon detector readout*. Nuclear Instruments & Methods in Physics Research A 461 (2001) 449-455
- [ 4 ] A.Go, A.Peisert *The Preshower gain pre-calibration using infrared light* (CERN CMS internal note 2001)

