One Size Fits All: Multiple Uses of Common Modules in the ATLAS Level-1 Calorimeter Trigger

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Abstract

The architecture of the ATLAS Level-1 Calorimeter Trigger has been improved and simplified by using a common module to perform different functions that originally required three separate modules. The key is the use of FPGAs with multiple configurations, and the adoption by different subsystems of a common high-density custom crate backplane that takes care to make data paths equal widths and includes minimal VMEbus. One module design can now be configured to count electron/photon and tau/hadron clusters, or count jets, or form missing and total transverse-energy sums and compare them to thresholds. In addition, operations are carried out at both crate and system levels by the same module design.

I. Introduction

The ATLAS Level-1 Calorimeter Trigger (figure 1) [1] uses reduced-granularity data from ~7200 'trigger towers', 0.1×0.1 in η–ϕ, covering all of the ATLAS electromagnetic and hadronic calorimeters. After digitisation and assignment of each pulse to the correct 25-ns bunch crossing in the Preprocessor subsystem, the trigger algorithms (figure 2) are executed in two parallel subsystems. The Cluster Processor (CP) finds and counts isolated electron/photon and tau/hadron clusters, while the Jet/Energy-sum Processor (JEP) finds and counts jets, as well as adding the total and missing transverse energy (E_T). The JEP also has logic to trigger on jets in the forward calorimetry, and on approximate total E_T in jets.

Cluster Processor Modules (CPMs), each covering an area of $\Delta\phi=90^\circ \times \Delta\eta\sim0.4$, send the number of e/γ and tau/hadron clusters they have found, up to a maximum of seven (three bits), to two merger modules that sum cluster multiplicities. One merger module handles 8 electron/photon threshold sets (each set being a combination of cluster, e.m. isolation, and hadronic isolation E_T), and the other handles 8 threshold sets that can each be programmed to be e/γ or tau/hadron. The maximum multiplicity for each threshold set is also seven. The multiplicity summing is in two stages: first for the 14 CPMs in each CP crate, and then for the four-crate CP subsystem. In the original design [2] these were Cluster Merger Modules, fed by cables from the CPMs to a separate crate. The final 'hit' multiplicity results are sent to the Central Trigger Processor (CTP).

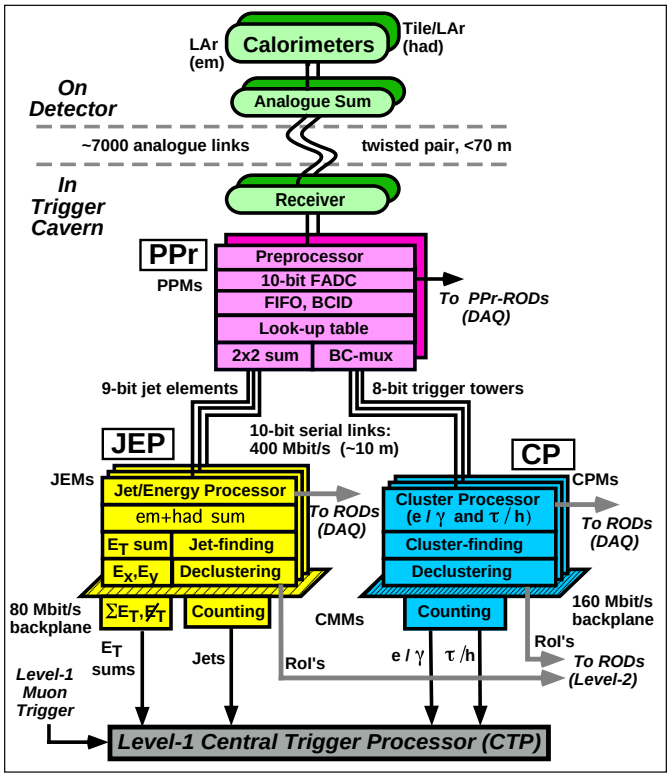

Figure 1: Overall architecture of the ATLAS Calorimeter Trigger.

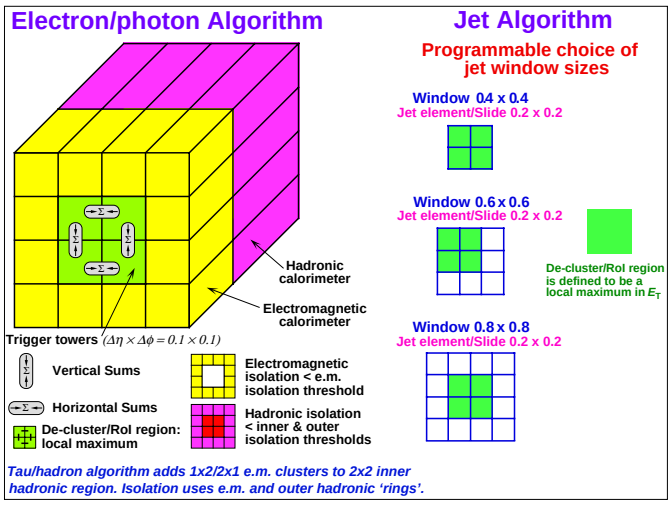

Figure 2: Calorimeter trigger algorithms.

Jet/Energy Modules (JEMs), each covering an area of $\Delta\phi=90^\circ \times \Delta\eta\sim0.8$, send the number of jets they have found, up to a maximum of seven, to a merger module that sums jet multiplicities. One merger module handles 8 jet thresholds. The maximum multiplicity for each threshold is also seven. The multiplicity summing is again in two stages: first for the 16 JEMs contained in each JEP crate, and then for the two-crate JEP subsystem before transmission to the CTP. In the original design the crate-level summing was done by Jet Merger Modules, fed by parallel signals on the backplane in the same crate as the JEMs.

Note that summing of the 'hit' multiplicities in both the CP and the JEP is essentially identical, except that the JEP has two more modules per crate with results to be counted.

The Jet/Energy Modules also sum E_T, as well as its x and y components needed for missing-E_T triggers, over the region that they cover. Further summing is again done in separate crate and subsystem stages. In the original design there were Sum Merger Modules in each crate, also fed via the backplane, followed by subsystem summing and comparison of total and missing transverse energy with sets of thresholds before transmission of the results to the CTP.

II. Common Merger Module Evolution

The functionality of the Cluster and Jet Merger Modules was very similar, so first those two designs were unified. A Cadence simulation showed that data signals could be transmitted over the full-crate width of the backplane at 40 MHz single-ended (mandatory due to pin-count limitations), so the same in-crate layout could be adopted for both the CP and the JEP [3]. This eliminated a crate needed for CP cluster counting, along with a large number of cable links from all of the CPMs, as well as reducing the design effort by eliminating one type of module. There are two hit-counting merger modules in each CP crate (8 threshold sets each) and one hit-counting module in each JEP crate. The slightly different requirements of the CP and JEP could be met by the use of programmable FPGA logic.

After some discussion of possible options for how and where to do the subsystem-level counting, it was decided to simplify further by putting hardware to do this on *all* modules. For the CP, the modules in three of the four crates do not use this logic, and only the two hit-counting modules in one crate actually do the subsystem-level counting. For the JEP, the module in one crate does the subsystem-level counts for both crates.

Thus we now have all cluster and jet hit-counting, at both crate and subsystem levels, done by one type of module. The inputs for the subsystem-level counting are supplied by cable(s) from the other crate(s), and by internal on-board links for the crate-level counts done by that module itself.

However, the E_T summing seemed to be a different problem for two reasons. First, the internal logic needed is different: there are four total-E_T thresholds and eight missing-E_T thresholds, and forming missing-E_T as well as its threshold comparisons is to be done using look-up tables. Second, more input bits needed to be handled. For the hit-counting, 16 modules each produce 8 3-bit numbers to be summed making a total of 384 bits, while for E_T there were 16 modules each producing 12-bit sums for E_T, E_x and E_y for a total of 576 bits.

It was then shown that the energy summation could be done by the *same* Common Merger Module (CMM) as the hit-counting since each of the 12-bit wide JEM E_T, E_x and E_y sums could be compressed to 8 bits without significant effect on trigger performance. A physics simulation was done using ATLFAST to process QCD 2-jet events from PYTHIA (method of study as in [4]). This showed that encoding the energy sums as 6 data bits and 2 scale bits did not produce any significant degradation of either energy resolution or trigger

performance, either on the individual JEM sums in each crate or on the inter-crate sums. The optimal scaling was to use the two scale bits to multiply by 1, 4, 16 or 64. At the same time, it was shown that FPGA code for summing the hit multiplicities, or for computing total and missing transverse energy, could be run in the same type of FPGAs. The multiplication needed for the energy scaling can be done by bit-shifting to keep the latency low. The JEP then has two CMMs in each crate: one for counting jet multiplicities, and one for summing transverse energy.

We thus end up with just one type of merger module, for both CP and JEP subsystems, and for both hit-counting and transverse-energy summing. Furthermore, this one module design contains both the crate-level and system-level logic. Which operations they carry out will be determined automatically by the crate and slot that they occupy.

III. Common Merger Module Design

A block diagram of the CMM is shown in figure 3. At the core of the design are the two blocks labeled Crate Merging Logic and System Merging Logic. These blocks contain all of the logic that is specific to one or more versions of the CMM. All of the other logic shown is common to all versions. The data widths shown are the maximum needed to implement all of the required versions of CMM.

Each CMM receives data from the local crate via a maximum of 400 backplane links. These data are re-timed to the system clock and sent to the Crate Merging Logic. The data output from the Crate Merging Logic are sent to System Merging Logic, either on the same CMM (in the case of system-level CMMs) or on a remote CMM (in the case of crate-level CMMs). The transmission of these data between CMMs is performed using parallel LVDS cable links.

On system-level CMMs, the System Merging Logic receives a maximum of 50 bits of data from the local Crate Merging Logic, and up to 75 bits of data from up to three remote crate-level CMMs. Data received from remote CMMs are re-timed to the board clock and data from the local crate merging logic are fed through a pipeline delay to compensate for any difference in the latency of the local and remote data paths. The results from the System Merging Logic are fed to the CTP via LVDS cable links. The System Merging logic on crate-level CMMs is redundant.

The core of the CMM logic is implemented in two large FPGAs, labeled Crate FPGA and System FPGA. These implement the following logic:

- Crate FPGA: Crate Merging Logic, Backplane Receiving Logic, Event Data Readout, Readout Control.
- System FPGA: System Merging Logic, Cable Receiving Logic, Event Data Readout, RoI Data Readout.

The main motivation for using FPGAs on the CMM is the flexibility they introduce into the design. By choosing two large devices rather than several smaller ones this flexibility is increased, as the number of hard-wired interconnections at board level is reduced. Both the Crate and System FPGAs are implemented with Xilinx XCV1000E devices. This device was chosen to meet the I/O requirement of the Crate FPGA and the RAM requirement of the System FPGA. It contains approximately 1.5 million gates including 96 blocks of 4kbit RAM. It is a fine-pitch ball-grid array package, with 660 pins of user-I/O.

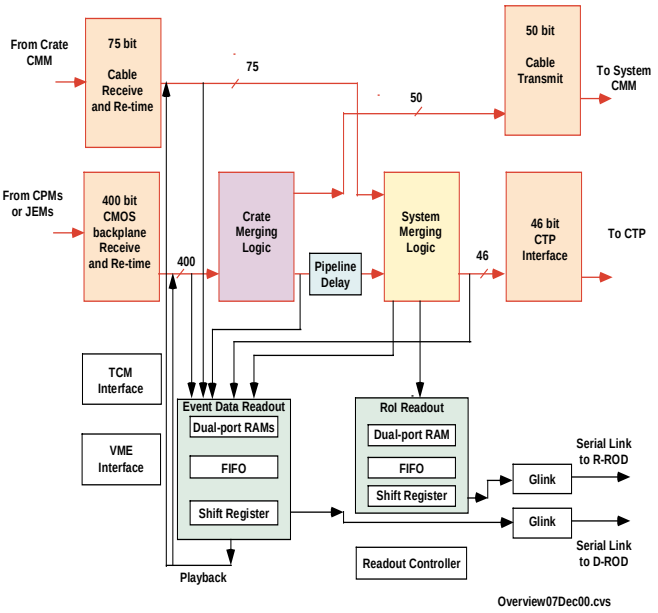

Figure 3: A block diagram of the Common Merger Module.

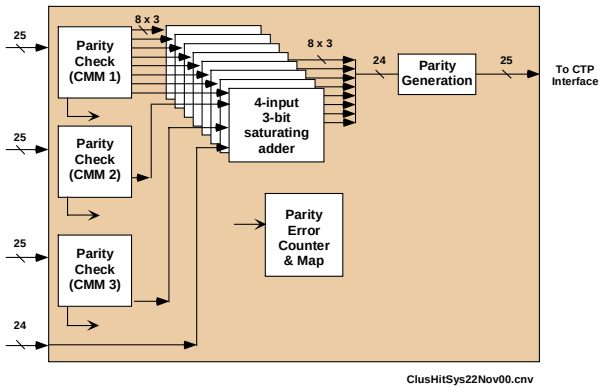

Figure 4: The system-merging logic of the e/γ System-level CMM.

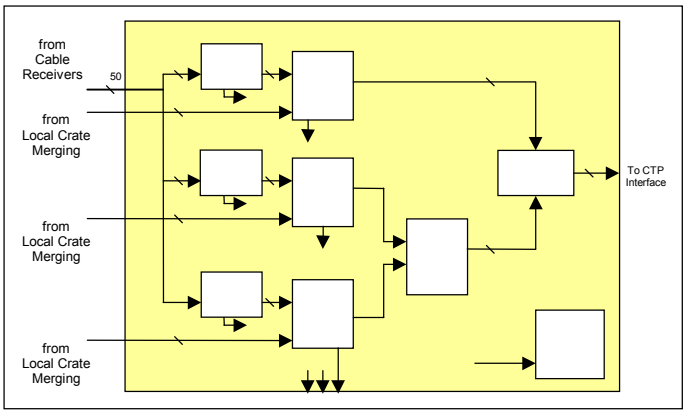

Figure5: The system-merging logic of the Energy System-level CMM.

The ATLAS level-1 calorimeter trigger requires the CMM to perform a number of different functions (see table 1). For a CMM to implement a function the specific configuration files for that function must be loaded into the Crate and System FPGAs. On board every CMM are flash memories that house all configuration files, so that every CMM has the potential to perform any of the functions listed in table 1. On power up, the CMM automatically configures itself to perform one of these functions, determined by the geographical address of the module.

CMM Module Types
e/γ Crate-level CMM
e/γ System-level CMM
τ/hadron Crate-level CMM
τ/hadron System-level CMM
Jet Crate-level CMM
Jet System-level CMM
Energy Crate-level CMM
Energy System-level CMM

Table 1: CMM module types.

Figures 4 and 5 show two examples of different logic designs that can be implemented in the System FPGA. Figure 4 shows the System Merging Logic required by the e/γ subsystem. This consists mainly of 7-bit adder trees which sum the e/γ multiplicities over all crates for each of 8 thresholds. Figure 5, on the other hand, shows the system-merging logic required to perform energy summation. Here the total E_T, E_x and E_y values are formed by summation. A bank of look-up tables (LUTs) is then used to apply thresholds to these values to produce the number of total-E_T and missing-E_T hits. In all cases, the output from the System Merging logic is sent to the CTP.

IV. Common Backplane

The use of the CMM in both the CP and JEP subsystems means that these subsystems require very similar backplanes. It can be seen from table 2 that, with the exception of speed, the requirements of the CP subsystem are a subset of those of the JEP subsystem. A backplane capable of hosting the JEP subsystem can therefore also be used to host the CP subsystem, provided the fan-in/out links between modules are capable of operating at 160 MHz. To take advantage of this, and rationalise the design of the Level-1 Calorimeter Trigger further, a common backplane has been designed for these two subsystems.

The common backplane is 9U high (400.05 mm) and 84 HP wide (426.72 mm). It can accommodate up to 21 modules, comprised of the following: 16 JEMs or 14 CPMs, 2 CMMs, 1 Timing Control Module (TCM) and 2 VME controllers. Most of the tracks on the backplane carry data fanned between neighbouring CPMs/JEMs, or data transferred from these modules to CMMs. There are also timing signals and a CANbus that is used to monitor temperatures and voltages within the crate.

Due to the large number of signal tracks on the backplane it is not possible to accommodate a full VMEbus. Instead a custom VME bus is used, called *VME – –*. This allows only A24 D16 VME cycles using a minimal set of VME lines: SYSRESET, A[23:1], D[15:0], DS0*, WRITE* and DTACK*. A custom adapter card is needed to provide the interface between the crate and a standard VME64 controller.

CP subsystem crate	**JEP subsystem crate**
14 CPMs	16 JEMs
CPM input from pre-processor = 80 serial links via 20 cable assemblies	JEM input from pre-processor = 88 serial links via 24 cable assemblies
CPM–CPM fan-in/out = 320 single-ended point-to-point links @ 160 MHz	JEM–JEM fan-in/out = 330 single-ended point-to-point links @ 80 MHz
Data input to each CMM from CPMs = 350 single-ended point-to-point links @ 40 MHz	Data input to each CMM from JEMs = 400 single-ended point-to-point links @ 40 MHz
TTC, CPU, DCS (CANbus) required	TTC, CPU, DCS (CANbus) required

Table 2: Comparison of the JEP and CP subsystem crate backplane requirements.

In addition to the signal tracks across the backplane, the backplane must also accommodate the serial links that bring data from the Preprocessor system to the CPMs/JEMs. These are brought to the back side of the backplane via untwisted shielded pair cable assemblies. These assemblies are mated to long through-pins on the rear of the backplane, and passed directly through the backplane to the processor modules on the other side. The same system of through pins is used on the CMM connectors to receive 84 twisted-pair cables carrying data from CMMs in remote crates.

The connections between the backplane and the modules are implemented using AMP Z-pack (Compact PCI) connectors. These feature 5 rows of pins at a 2 mm pitch, allowing a total of 820 pins to be connected to each module. A signal to ground ratio of 4:3 is used on these pins to minimise interference between the signals.

V. Example of Flexibility: New Algorithms

This backplane just described, combined with the use of FPGAs in both the CMM and JEM designs, allows us to add some new trigger algorithms that have been requested by ATLAS but were not foreseen in the original design. No doubt other variations will appear in the future.

- The forward calorimetry, covering rapidities from 3.2 to 4.9, was originally included in the trigger only because it was needed to improve the missing-E_T resolution. However, in addition to allowing extension of the normal jet trigger into this range, it has recently been proposed that certain Higgs decays via Ws (i.e., the 'invisible Higgs' channel) might be picked up by a trigger on jets in the FCAL in conjunction with missing-E_T. The flexibility of the FPGA logic in the JEMs allows forward jets to be found on their own, and the logic in the CMM can be altered to count them separately.
- A trigger on approximate total E_T in jets was going to be done in the CTP. This multiplies the number of jets exceeding each jet threshold by the value of the threshold, and compares the estimated total jet E_T obtained with some

total jet-E_T thresholds. This can now be done in the final subsystem-level jet-counting FPGA, which is more logical and appropriate.

- Triggers on total E_T can be spoiled by noise, particularly if it is coherent. Simulation indicates that matters might be improved by requiring local regions to exceed a low threshold value if they are to be added to the total. This could, of course, be done in the JEMs and simply replace the normal total-E_T trigger. However, if it is desired to use this trigger in *parallel* with the normal total-E_T trigger, the use of FPGA logic in both the JEMs and CMMs allows this to be done by using some of the jet logic.

VI. Other Common Modules: TCM and ROD

In addition to the hardware described above, two other modules in the ATLAS Level-1 Calorimeter Trigger perform multiple roles. A common Readout Driver handles both readout data and level-1 trigger regions-of-interest in both CP and JEP. This module is described in an accompanying paper.

A common Timing Control Module has also been designed for use in the CP, JEP, and Preprocessor subsystems. It provides the interface between the crates in these subsystems and the ATLAS TTC and DCS networks. One difficulty in the design of the TCM is that the Preprocessor and CP/JEP crates use different formats and connectors to implement their VME buses. To overcome this problem the TCM uses and an Adapter Link Card (ALC) to house the VME interface. The ALC is essentially a daughter card for the TCM. It differs from normal daughter cards, however, in that it fits into a cut-out section at the rear of the TCM and lies flush with that card. Two ALCs have been designed, to implement the VME interfaces for the Preprocessor and CP/JEP systems.

VII. Status and Testing

Prototype versions of the CMM and the common backplane have been designed, and will shortly be sent out for manufacture. A prototype TCM has been manufactured and is currently undergoing stand-alone tests, and a prototype common ROD module exists and its interfaces with other ATLAS subsystems have been tested at CERN.

In March 2002, a complete vertical 'slice' of the ATLAS Level-1 Calorimeter Trigger will be built and tested. This will include prototype versions of all of the hardware elements in the system, including all of the common hardware described above.

VIII. Conclusions

We have shown how the use of programmable FPGA logic has allowed us to implement what were originally three separate kinds of merger modules as a single design. Although two of the three were fairly similar, the energy summation is quite a different task from hit counting, but by making the number of input and output signals the same and by using versatile and powerful FPGAs it could still be accommodated. This reduction in the number of different module types saves on design effort and on non-recurrent engineering costs, and reduces the number of spare modules required.

Although the use of a common custom backplane in the CP and JEP subsystems was mandated by the use of the Common Merger Module, the gains just mentioned make it too a useful simplification to the trigger system.

The use of a common Readout Driver Module for the two subsystems, again made possible by the use of programmable logic, and the use of a common Timing Control Module throughout all three calorimeter trigger subsystems, also carries the same advantages.

References

[1] ATLAS Level-1 Calorimeter Trigger home page: http://hepwww.pp.rl.ac.uk/Atlas-L1

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[4] R. Dubitzky and K. Jakobs, *Study of the performance of the Level-1 P_t^{miss} Trigger*, ATL-DAQ-99-010