"The MAD", a Full Custom ASIC for the CMS Barrel Muon Chambers Front End Electronics

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Abstract

To meet frontend electronics needs of CMS barrel muon chambers a full custom ASIC, named "The MAD", has been first developed by INFN of Padova and then produced in 80.000 pieces to equip the 180.000 drift tubes[1].

The task of this IC is to amplify signals picked up by chamber wires, compare them against an external threshold and transmit the results to the acquisition electronics.

The chip, built using 0.8 µm BiCMOS technology, provides 4 identical chains of amplification, discrimination and cable driving circuitry. It integrates a flexible channel enabling/disabling feature and a temperature probe for monitoring purposes.

The working conditions of the detector set requirements for high sensitivity and speed combined with low noise and little power consumption. Moreover, as the basic requirement for the frontend is the ability to work at very low threshold to improve efficiency and time resolution, a good uniformity of amplification between channels of different chips and very low offset for the whole chain are needed.

The ASIC has been extensively and deeply tested resulting in good performances; particularly, big effort was put in testing radiation (neutron, gamma rays and ions) tolerance and ageing effects to check behaviour and reliability in LHC environment.

I. ASIC DESCRIPTION

A. General

The analog frontend electronics for the muon chambers of CMS barrel has been integrated in a full custom ASIC, named "The MAD", developed by INFN of Padova using 0.8 µm BiCMOS technology from Austria Mikro Systeme. Each chip provides the signal processing for 4 drift tubes in a 2.5x2.5 mm^2 die, housed in a TQFP44 package.

Figure 1 shows the block diagram of the ASIC: the 4 identical analog chains are made of a charge preamplifier followed by a simple shaper with baseline restorer, whose output is compared against an external threshold by a latched discriminator; the output pulses are then stretched by a programmable one-shot and sent to an output stage able to drive long twisted pair cables with LVDS compatible levels.

Control and monitoring features have been included in the chip: to mask noisy wires each channel can be disabled at the shaper input resulting in little crosstalk to neighbours. A fast disable/enable feature, controlled via LVDS levels acting on the output driver of left and right channel pairs, allows the simulation of tracks perpendicular to the detector. An absolute temperature probe has been integrated in order to detect electronics failures and monitor environmental changes.

Two separate power supplies (5 V and 2.5 V) are used in order to reduce power drain and minimize interference between input and output sections. The layout and routing have been particularly cured and many pins have been reserved for power, input ground and analog ground.

To prevent latch-up events and improve crosstalk performances guard ring structures have been largely used to isolate sensitive stages like the charge preamplifier or complementary MOS devices.

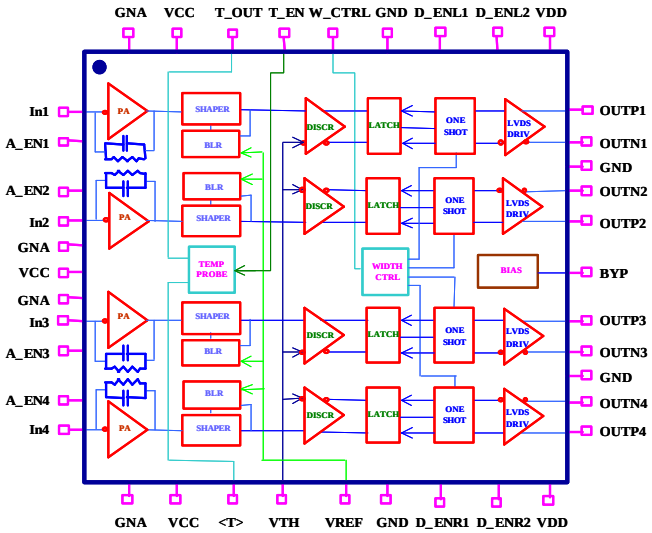

Figure 1: Block diagram of the ASIC.

B. Analog section

The preamplifier uses a single gain stage with a GBW product in excess of 1 GHz (from simulation) and a feedback time constant of 33 ns. Input pads, derived from standard ones, were modified to enhance ESD protection by integrating series resistor and large diodes connected to analog ground. Power dissipation for this stage is about 2.5 mW.

The shaper is a low gain integrator with a small time constant: the noninverting input is connected to the preamplifier while the inverting one allows to put this stage inside the feedback loop of a low offset OTA; this combination implements a time invariant baseline restorer

acting as a high pass filter for the signal path. Tests performed on this circuit show that the quiescent level of the shaper output can be set anywhere between 1.0 and 3.5 V even in the presence of worst-case parameters for fabrication process and operating conditions of the IC. The pin VREF, common to the four OTAs, is used to control the quiescent level from outside.

The output of the shaper is directly connected to the noninverting input of a fully differential discriminator with 2 gain stages. The other input of the comparator is connected to the external threshold pin VTH, common to all channels. The input section uses no special technique, except a careful layout, to obtain low offset with high speed; a hysteresis of about ±1 mV helps in avoiding autoscillation and in speeding up commutation with slow input signals. Common mode input voltage ranges from 1.2 to 3.8 V. Finally, a buffer prevents switching noise from the following sections to propagate backwards to sensitive paths.

All previously described blocks share a single +5 V supply for about 12 mW power drain.

C. *Output section*

The buffered output of the discriminator is capacitively coupled to a one-shot that is very similar to a classical astable multivibrator; its differential output, when active, stores the status of comparator in the latch so producing a non retriggerable pulse whose width is inversely proportional to the current sunk from W_CTRL pin, again shared by all channels. Critical parameters of this section are propagation delay, which sets the ability to catch narrow pulses produced by signals just over threshold, and the time it takes to fully recover after the falling edge of a pulse.

The same lines that activate the latch are used to feed the output driver, again a differential one capable of driving a 100 Ω load at voltage levels compatible with LVDS standard. Voltage driving has been chosen because NPN bipolar transistors are faster than PNP and PMOS devices and also because this turns out to be a power convenient choice when the load is a cable terminated at both ends. The working conditions of the driver are a compromise between speed and power drain: rise and fall time are below 2.5 ns and, to reduce external components, terminating resistors are integrated in the pads. To reduce consumption, the supply voltage is the lowest possible, 2.5 V, yielding power dissipation, including the one-shot, of about 12 mW.

D. *Temperature sensor, channels masking and biasing*

Temperature sensing is based on the voltage difference between base emitter junctions operated at different current densities. Voltage output is 7.5 mV/°K and power drain about 1 mW from 5 V. The output is always available at pin <T> while at pin T_OUT a unity gain buffer, enabled by a TTL high level (pin T_EN), allows the multiplexing of more chips on the same net.

Each frontend channel can be masked by a TTL high level applied to pins A_EN(1-4), in this case recovery to normal operation requires about 10 μs. Channels 1 & 2 (left channels) can be enabled or disabled in about 30 ns by a differential signal, LVDS or 3.3 V PECL, applied to pins D_ENL(1-2); the same for right channels 3 & 4 via pins D_ENR(1-2).

A bias circuit controls the current generators of the whole chip and supplies voltage for one-shot sections. Its output is connected to pin BYP for bypassing with a capacitor to GNA.

II. ASIC PERFORMANCES

We have verified ASIC performances on bare chips using a specific test board with minimal stray capacitance to reduce measurements errors. The same measurements have been carried out on chips mounted on FEB, the final boards in which the frontend electronics of the CMS barrel muon chambers is organized.

First of all power dissipation is very low, about 25 mW/ch with little variation with temperature and input signal rate.

A. *General tests*

Since no test pads were foreseen in the chip, tests on the analog section are based on the statistics of output response to δ–like charge pulses, injected by a voltage pulse generator via a series capacitor of about 1pF.

In order to measure the gain, two different values of charge, 3 and 9 fC, have been injected: the resulting threshold distributions for the bare chip have mean values of 10.7 and 33.6 mV, respectively, with r.m.s. of 0.34 and 0.42 mV (see figure 2). This little spread is due to gain variations among chips, caused by the tolerance of feedback capacitor in charge preamplifier, and by the discriminator and baseline restorer offset.

Resulting gain is 3.8 mV/fC in average, about 10% higher than simulated because of a process parameter (capacitor oxide thickness) out of specification in the preserie wafer (results shown are from preserie devices). Sensitivity is constant up to 500 fC input with less than 1% integral nonlinearity and saturation occurs at about 800 fC. Uniformity is very good, r.m.s. about 0.01 mV as chips belong to the same wafer.

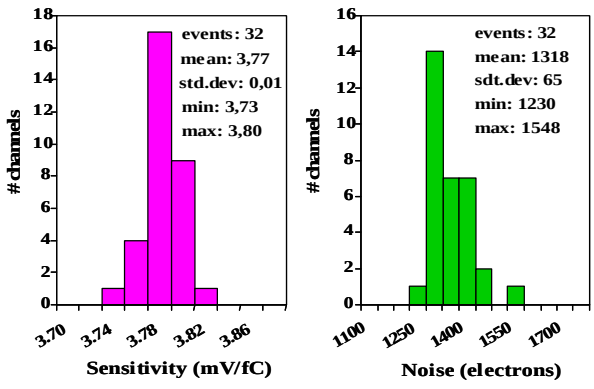

Figure 2: Sensitivity and noise of bare ASIC.

Other key characteristics for low threshold operation are noise and crosstalk: bare chips exhibit ENC 1320 electrons

(slope of 45 e/pF) and a value below 0.1% for the latter. Once mounted on the PCB these two figures increase to 1900 electrons (slope of 60 e-/pF) and 0.2% because of the external protection network mounted on FEBs in order to withstand a full discharge of one drift tube.

Figure 3 shows the time walk characteristics versus the input charge overdrive (amount of charge over the threshold) for the bare ASIC in two different configurations. In the first case the input pins are directly connected to the charge generator, while in the second one a 40 pF capacitor is added to simulate the detector capacitance (about 10 pF/m, so this value represents the worst case). Since the estimated average charge is about 50÷100 fC, the deterioration on time walk performances is acceptable.

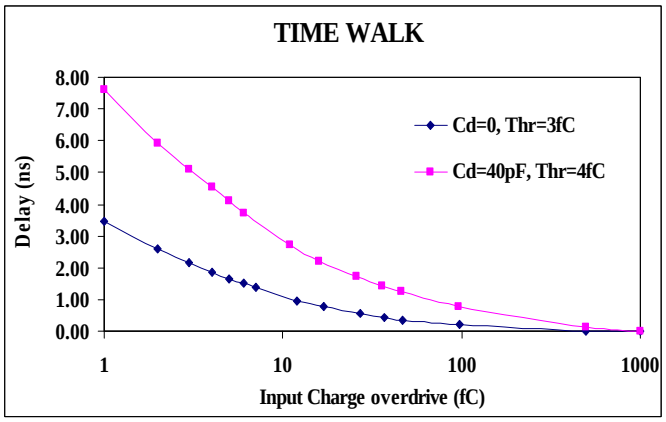

Figure 3: Time walk of the bare chip with 2 input configurations.

Temperature sensors integrated in the ASIC were also tested for chips mounted on the FEBs: at an ambient temperature of 23±1 °C, we obtain an average value of 27 °C, with a maximum error of ±3 °C and a heating of 4 °C respect to ambient.

The conversion factor of 7.5 mV/°K has been measured for few ASICs in a climatic chamber in the range 0÷100 °C. In the same chamber we have verified specifications as a function of temperature. All performances, except for output width, exhibit little variations against temperature and the output levels comply with LVDS standard in the 0÷100 °C range and for supply voltage tolerances of ±10%.

B. July 1999 and 2000 Test Beam results

A prototype chamber with a final design of the cells and equipped with MAD chips, was installed inside the M1 magnet of the CERN H2 zone and exposed to high-energy muon beams in July 1999[4] and in the same period of 2000[6].

The results obtained were very satisfactory: efficiency higher than 95.5% and resolution of 200 μm were reached in all operating conditions with safety values of drift tubes voltages.

In detail figure 4 shows the meantimer resolution for different beam positions along the wires[5] and different wire amplification: degradation of signals coming from the opposite end of the wire (respect to FEB) account for a resolution worsening limited to 0.5 ns in real conditions.

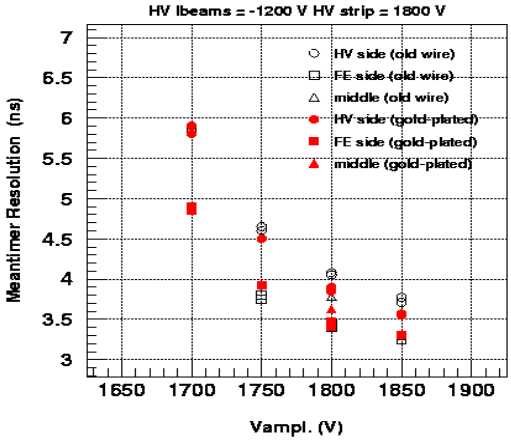

Figure 4: Meantimer resolution for different beam positions along the wires and different amplification.

III. ASIC RELIABILITY

About 45000 ASICs are located inside the gas volume of the CMS detector in a hardly accessible environment and must operate for a long time (at least 10 years) with no or minimal maintenance.

Electronics reliability is therefore a crucial point and specific tests were performed to check the ASIC against radiations, ageing and HV discharges.

A. Radiation tests

Besides usual considerations about wear out of electronics, big concern must be devoted to radiation tolerance: in the barrel muon stations only the neutron flux (5 10^{10} n/cm^2 for 10 years of LHC activity, 10% thermal), can generate problems (the iron yoke is a shield against other radiation type) mainly due to SEU and SEL (Single Events Upsets and Latch-up). The first item accounts for trigger and readout noise while the second one can cause device burn out.

The spectrum of neutron flux in CMS ranges from thermal up to high-energy. To meet these specifications, we have performed tests at INFN Legnaro National Laboratory (for thermal and fast neutrons up to 10 MEV) and at the Universitè Catholique of Louvain-la-Neuve laboratory (for fast neutrons up to 60 MeV)[2].

Low energy neutrons were produced using a graphite moderator with a deuterium beam accelerated up to 7 MeV by the Van de Graaff accelerator of LNL while fast neutrons up to 10 MeV were obtained from the same beam on a thick beryllium target. In a same way, the Louvain facility provides a wide neutron spectrum, roughly flat in the range 20-60 MeV, using a protons beam of energy up to 65 MeV.

For all radiation tests a suitable acquisition system was implemented in order to monitor supply currents and temperature of the ASIC to detect latch-up events; SEU events at different threshold levels have been acquired to

verify the dependence using counters on single channels. Also, at the end of exposure, all devices were deeply re-tested to verify changes in static and dynamic characteristics.

Being basically a charge sensitive device, this ASIC is naturally affected by SEU: we are interested in checking if the associated rate is compatible with detector efficiency.

The neutron cross-section per readout channel is plotted in Figure 5 showing a roughly exponential dependence on the threshold. We can see the not-negligible contribution of slow neutrons to cross-section (only one measure at 20 fC threshold). From these results we can estimate few thousands spurious counts for the whole detector activity: a very safe value.

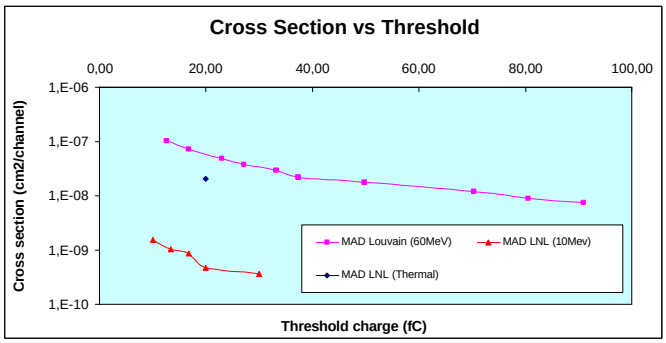

Figure 5: Fast and slow neutrons cross-section versus threshold.

In all tests performed with neutrons no LATCH-UP events were detected. Also performances tests done after irradiation have shown no significant changes.

For better SEL characterization of the chip, we decided for a test with heavy ions, as the energy deposition is quite larger[3]. Measurements have been performed in April 2000 at the Tandem accelerator of INFN LNL. The ion beams were set to obtain fluxes (monitored on line with silicon diodes) of 10^4-10^5 ions/cm^{2}s^{-1} in order to achieve an integrated fluence of some units/μm^2 in the die. Table 1 shows the ions used, selected to cover a useful range of LET values.

Table 1: LET (MeVcm/mg) and energy (MeV) of ions beams used.

Ion	Energy	LET
^{79}Br	242	39,4
^{79}Ag	267	54,7
^{127}I	277	61,8

The irradiated ASIC was a sample of the final production, housed in a ceramic package without cover in order to expose directly the silicon die.

Figure 6 shows SEU cross-section versus threshold measured in 2 different condition: the largest figures have been obtained enabling the amplifying section of all channels, while in the second case only the output circuits were enabled resulting in much lower values, independent on threshold.

We found little difference in cross-sections ranging from $4{\cdot}10^{-4}$ to $7{\cdot}10^{-4}$ cm^2/ch with ions type. Also in this case no latch-up event was detected.

Hence results from irradiation with heavy ions show little ASIC sensitivity to SEU and immunity to LATCH-UP, in agreement with previous neutron tests.

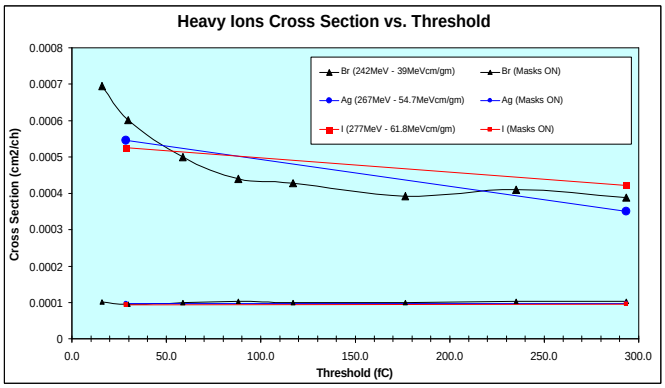

Figure 6: Heavy ions cross-section versus threshold.

Last check was performed with gamma rays: few prototypes have been exposed to a Cobalt source up to 80 Krad dose in Bologna facility: static and dynamic characteristics measured before and after irradiation have not shown any significant change.

B. *HV discharges test*

Whenever a spark occurs in a drift tube a very large charge, stored in the 470 pF decoupling capacitor, moves into the sensitive input pins of the chip. To preserve the ASIC from this potentially destructive event a protection circuit was added on FEB: a 39 Ω series resistor and a double diode to ground, all in parallel with 100 μm gap limiting voltage to about 500 V. Tests have shown that with this configuration the ASIC inputs can withstand more than 10^5 sparks at full wire potential (~3.6 KV) and still work.

C. *Ageing test*

Another important parameter concurring to system reliability is MTBF (mean time before failure). The practical method to measure it, is to let electronics operate in stress conditions (high temperature and supply values) for a long time, resulting in accelerated ageing, and detect failures versus time.

A test was performed on 10 prototypes, keeping them into an oven at 125 °C for 2000 hours in order to simulate 10 years of CMS activity. Test ended with no faults; extensive tests on whole frontend electronics, FEBs and service boards, are now in progress having simulated several years of activity with no faults.

IV. CONCLUSIONS

The MAD ASIC, now produced in about 80.000 tested pieces, shows very good performances at low power consumption as summarized in the table below. Also temperature probe and masking features work properly.

The chip was extensively and successfully tested with muon beam at H2 CERN facility.

COMPASS, a HEP experiment under construction at the Super Proton Synchrotron (SPS), has used some thousands MAD chips for its multiwires proportional chambers and preliminary results confirm good performances.

The ASIC shows good MTBF characteristics, low SEU rate and immunity to latch-up events in spite of using a standard and not too expensive technology. Safe and reliable operation in CMS environment can be assumed with a reasonably low rate of background events and failures.

V. REFERENCES

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[2] S. Agosteo et al., *First evaluation of neutron induced Single Event Effects on the CMS barrel muon electronics*, CMS Note 2000/024.

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[4] M. Aguilar-Benítez et al., *Construction and Test of the final CMS Barrel Drift Tube Muon Chamber Prototype*, accepted for publication in Nucl. Instr. And Meth. A (2001).

[5] S. Paoletti, *A study of the CMS Q4 prototype chamber for different beam positions along the wires*, CMS IN 2000/021.

[6] M. Cerrada et al., *Results from the Analysis of the Test Beam Data taken with the Barrel Muon DT Prototype Q4*, CMS Note 2001/041.

Table 2: Summary of ASIC performances (preserie).

power ≅ 25 mW/channel @ +5 V & +2.5 V	**threshold range** 0÷500 fC with < 1% nonlinearity
Zin ≅ 100 Ω (5÷200 MHz)	**crosstalk** < 0.1%
noise ≅ 1300 e^- ± 5% @ C_D = 0; slope ≅ 45 e^-/pF	**propagation delay** ≅ 4 ns
sensitivity ≅ 3.77 mV/fC ± 0.5%	**time walk** ≅ 3.5 ns @ C_D = 0
BLR + discriminator offset < 0.13 fC r.m.s.	**output pulse width** 20÷200 ns (5% r.m.s. @ 50 ns)
max input signal before saturation ≅ 800 fC	**one shot dead time** ≅ 9 ns
input rate without loss of accuracy > 2 MHz @ 800 fC	**output t_r & t_f** < 2.5 ns
No latch up events detected for neutrons up to 60 MeV	

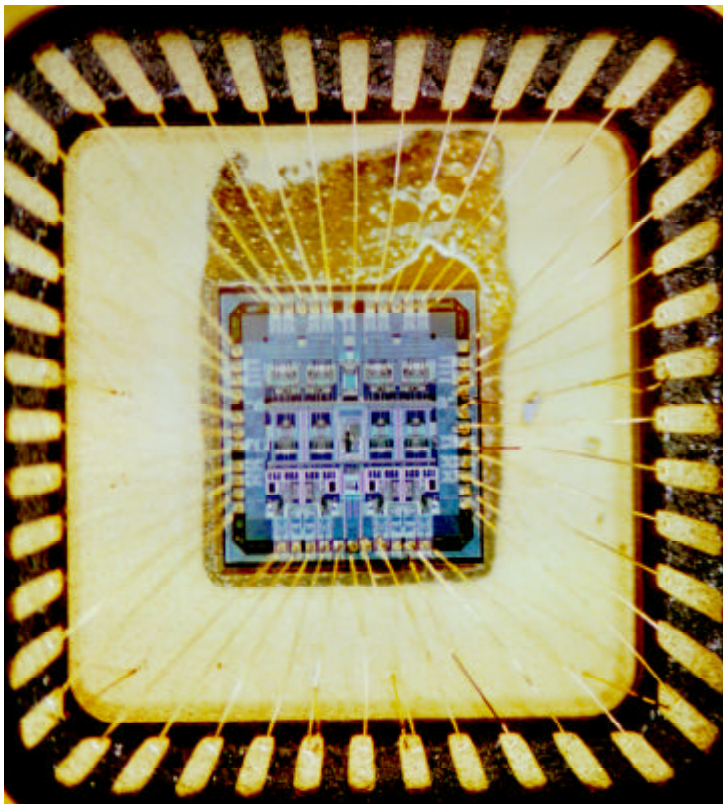

Figure 7: Microphoto of the definitive die bonded to a ceramic case.