A Radiation Tolerant Laser Driver Array for Optical Transmission in the LHC Experiments

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Abstract

A 3-way Laser Driver ASIC has been implemented in deep-submicron CMOS technology, according to the CMS Tracker performance and rad-tolerance requirements. While being optimised for analogue operation, the full-custom IC is also compatible with LVDS digital signalling. It will be deployed for analogue and digital transmission in the 50.000 fibre link of the Tracker. A combination of linearization methods allows achieving good analogue performance (8-bit equivalent dynamic range, with 250 MHz bandwidth), while maintaining wide input common-mode range (±350 mV) and power dissipation of 10 mW/channel. The linearly amplified signals are superposed to a DC-current, programmable over a wide range (0-55 mA). The latter capability allows tracking of changes in laser threshold due to ageing or radiation damage. The driver gain and laser bias-current are programmable via a SEU-robust serial interface. The results of ASIC qualification are discussed in the paper.

I. Introduction

Data connection to the CMS Tracker Front-Ends is provided by a large number of optical fibre links: 50.000 analogue for readout and 3.000 digital for trigger, timing, and control signals distribution [1]. The Front-End components must withstand the harsh radiation environment of the Tracker, over the planned detector lifetime of 10 years (total ionising dose and hadron fluence exceeding 10 MRads and 10^{14} neutron-equivalent/cm^2 respectively) [2]. The baseline technology for ASIC developments in the Tracker is a 0.25 µm CMOS, 3-metals, commercial technology (5 nm oxide thickness) [3, 4, 5]. The intrinsic radiation tolerance of this technology is increased to the required levels, by using appropriately extended design-rules and self-correcting logic. The use of this technology for analogue applications was carefully evaluated before employing it for the design of the Front End chips.

A Linear Laser Driver (LLD) array for the CMS Tracker links had been already developed and implemented in a non-radiation tolerant BiCMOS technology [6]. The design was then translated in the 0.25 µm CMOS technology at an earlier stage of the Tracker design [7]. A new LLD has now been implemented in the same technology, appropriately matching the Tracker modularity and functionality requirements for both analogue and digital links.

Section II explains the device functionality and major specifications. Section III describes the electrical circuit and layout. Section IV reports on the measurement results and device qualification.

II. Functionality

Figure 1 shows the block diagram of the new LLD chip. The laser driver converts a differential input voltage into a single ended output current added to a pre-set DC current. The DC current allows correct biasing of the laser diode above threshold in the linear region of its characteristic. The absolute value of the bias current can be varied over a wide range (0 to 55 mA), in order to maintain the correct functionality of laser diodes with very high threshold currents as a consequence of radiation damage. The laser diode-biasing scheme (current sink) is compatible with the use of common-anode laser diode arrays.

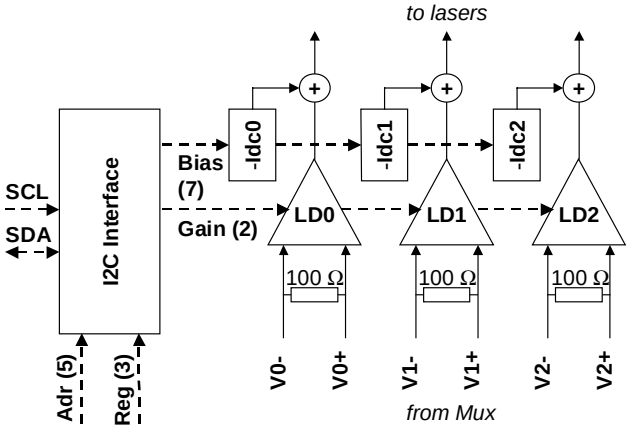

Figure 1: Block diagram.

Input signals are transmitted to the laser driver using some 0-30 cm of 100 Ω matched transmission lines. The driver is optimised for analogue operation in terms of exhibiting good linearity and low noise. However, input voltage levels are compatible with the digital LVDS standard (±400 mV into 100 Ω). The gain can be chosen from 4 pre-set values. Gain control provides an extra degree of freedom for optimally equalising the CMS Tracker readout chain. A system-level simulation of the fibre link performance achievable with a four-gain equalisation is presented in [8].

The IC modularity is 3 channels per chip. About 20 thousand 3-way laser drivers will be used for the CMS Tracker readout and control links. The total power dissipation of individual chips must remain constant regardless of the modulation signal to minimise cross-talk and noise injection in the common power supplies.

The channels can be individually addressed via a serial digital interface (Philips Semiconductors I2C standard), which allows individual power down, gain control, and pre-bias control. Robustness to Single Event Upsets is achieved by tripling the digital logic in the interface and by using a majority voting decision scheme. The power-up I2C register configuration is read from a set of hard-wired inputs. Thus it is possible to insure that the optical links are correctly biased at power-up.

III. CIRCUIT AND LAYOUT

The Linear Laser Driver consists of a Linear Driver and a laser-diode bias generator (Figure 2).

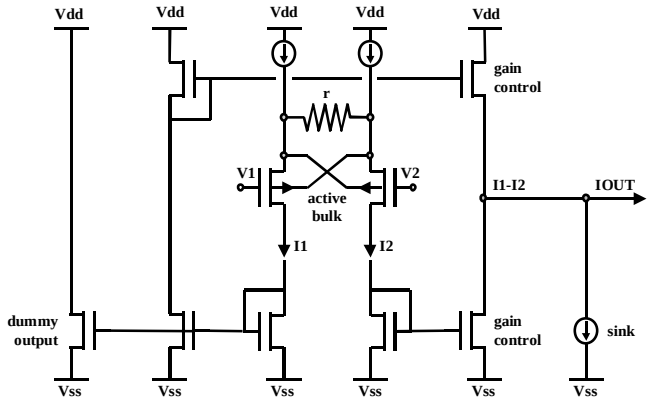

Figure 2: Circuit diagram.

The Linear Driver consists of a degenerated PMOS differential pair and a push-pull output stage. The degenerated differential pair, in comparison to alternative solutions, is conceptually simple and offers good dynamic and noise performance with limited power dissipation. The PMOS version is bulk-effect-free, thus allowing a larger input common-mode range. The required linearity is obtained by combining two source-degeneration methods: a parallel source-degeneration resistor, and a source-bulk cross-connection between the transistors of the differential pair. The use of both methods allows keeping the degeneration resistor to a value compatible with the required input common-mode range. The push-pull output stage mirrors the currents in the differential pair branches and subtract them at the output node. Three switched output stages can be activated in parallel, to provide four different selectable gains. In order to keep the power supply current constant, a dummy output stage dumps the complement of the modulation current directly into the power supplies.

The laser-diode bias generator circuit consists of an array of current sources and sinks. The enabling logic allows them to be switched on and off as appropriate in order to generate a current linearly variable between 0 and 55 mA. A regulated cascode scheme [9] has been used to keep the output impedance high and the compliance voltage low (<500 mV) in all possible operating conditions. To minimise the cross talk within a given chip, each individual channel contains its own independent bias circuit and power-down logic.

The circuit has been laid-out taking particular care of matching the differential pairs, the current mirrors, and the elementary current sources and sinks. All the NMOS transistors have enclosed geometry and isolation guard-rings to prevent the formation of radiation-induced leakage channels between source and drain in a same transistor or between adjacent transistors. These layout practices, together with the intrinsic good quality of the gate oxide of the technology being used, offer proven radiation tolerance up to levels compatible with the most stringent requirements of HEP experiments. The Linear Laser Driver layout and pin-out are shown in Figure 3.

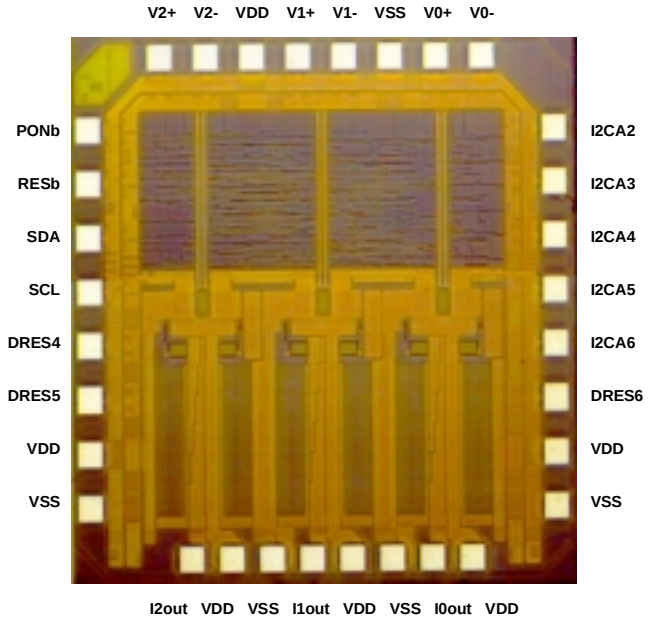

Figure 3: Device layout (die size: 2 mm x 2 mm).

IV. DEVICE QUALIFICATION

The LLD static and dynamic performance has been tested extensively, for different chips and various settings of their configuration registers (different gains and bias currents). Moreover, the foundry provided us with prototype chips corresponding to 5 different process corners. This practice is used to evaluate the deviation between the expected and actual performance in the final production lot due to statistical process variations. Twelve chips corresponding to 5 different process corners have been mounted and tested and shown to be fully functional. Channel-to-channel as well as chip-to-chip variation appears to be very limited (regardless of the different processing). One chip (nominal process) has been tested for tolerance to total-dose radiation and accelerated ageing. The set of qualification results is presented in the following sub-sections.

A. Static performance

Figure 4 shows the pre-bias current for 5 chips differently processed (different σs). The measured LSB is 0.45 mA and the highest current that can be generated on-chip is 57 mA. The transfer characteristics (differential and common-mode) and output characteristic of the LLD have been measured with a Semiconductor Parameter Analyser. Figure 5 shows the differential transfer characteristics of the LLD, for four different gains (and different σs). The measured (transconductance) gain values are 5.3 mS, 7.7 mS, 10.6 mS, and 13.2 mS (5% above their nominal design values).

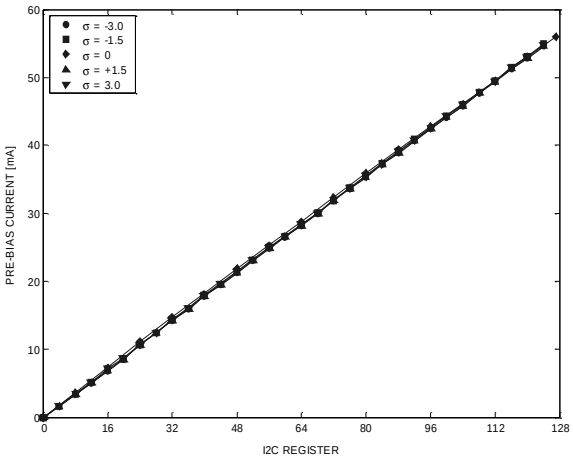

Figure 4: Pre-bias current.

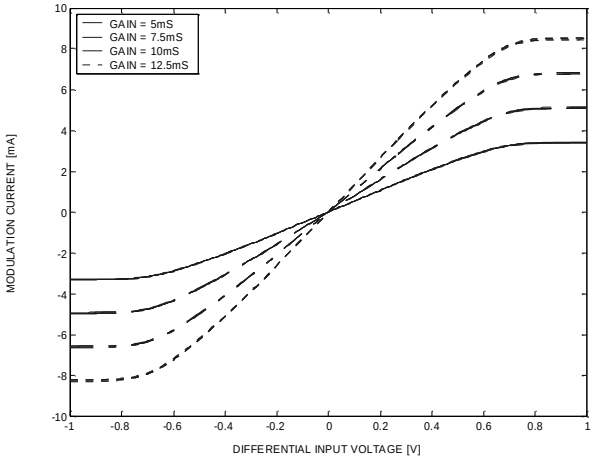

Figure 5: Differential transfer characteristic.

Figure 6 shows the linearity error, for different input common mode voltages (V_{cm} = 0 and V_{cm} = ±625 mV). The linearity error is calculated as the absolute difference between the real output current and its (least-square) linear fit, and is expressed as a percentage of the specified operating range (integral linearity deviation). In absence of common mode, the error is less than 0.5% over the whole linear operating range (±300 mV). The common-mode has an impact on linearity. However, performance degradation is negligible for an input common mode between ±350 mV. Figure 7 shows the integral linearity deviation as a function of the input common mode.

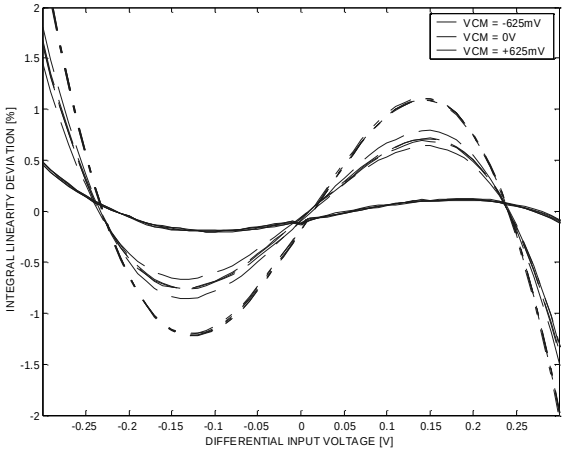

Figure 6: Linearity error.

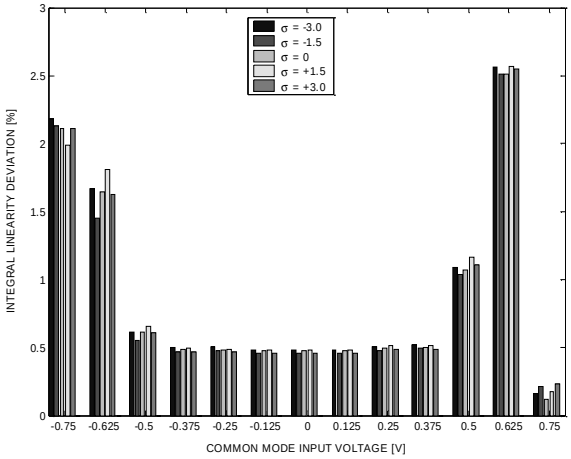

Figure 7: Common-mode impact on linearity error.

The Common Mode Rejection Ratio at DC is inferred from the common-mode transfer characteristic. The DC-CMRR is 40 dB in the worst case (maximum laser-bias) and becomes as high as 70 dB at low biases. The output impedance (inferred from the output characteristic) of the LLD varies between 3 kΩ and 10 kΩ, depending on the pre-bias, and is in all cases much higher than the typical dynamic impedance of the laser diode (<10 Ω).

The minimum power consumption is 10mW per channel at minimum bias and minimum gain. The power consumption increases proportionally to the bias current and it is also to some extent dependent on the gain. The maximum power consumption is below 110 mW/channel.

B. Dynamic performance

The dynamic performance of the LLD has been evaluated with laser emitters, which are representative of the ones to be used in the final application. A wide-bandwidth optical head is used for receiving the optical signal and converting it back to electrical for compatibility with standard instrumentation. The pulse response of different chips and for different gains is shown in Figure 8. The response exhibits little overshoot and ringing. The measured rise and fall times are below 2.5 ns. The measured settling times (to within 1% of the final value) are of 10-12 ns, which leaves (for a 40 MHz sampled system) 13-15 ns for correctly sampling the output signal.

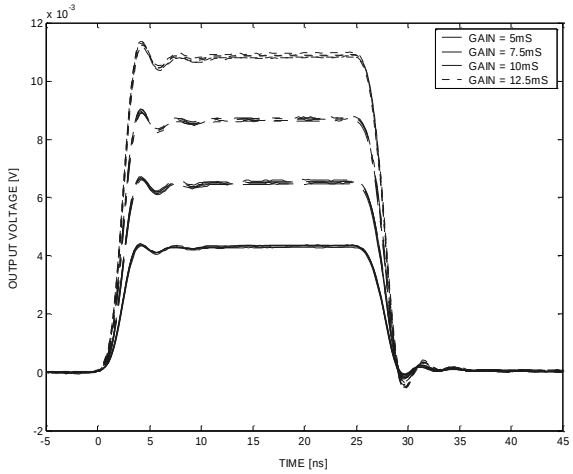

Figure 8: Pulse response.

The frequency responses (differential and common-mode) are shown in Figure 9. The analogue bandwidth has been measured with a network analyser and was found to be 250 MHz. The equivalent input noise into this bandwidth is gain and laser bias dependent. The measured noise is in all cases below 1 mVrms. The CMRR is shown in Figure 10 as a function of frequency (15 mA bias current). Cross-talk between channels has been also measured and is below – 60 dB.

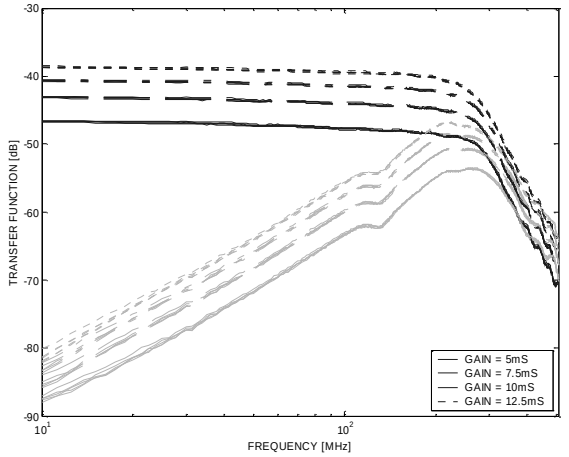

Figure 9: Frequency response.

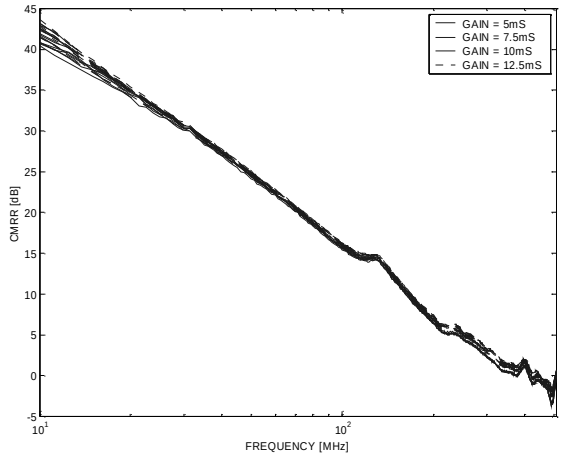

Figure 10: Common Mode Rejection Ratio.

C. Radiation hardness

The circuit has been tested for total ionising dose effects using an X-ray source, to investigate possible performance degradation related to ionising effects (charge trapping in oxide interface states). The experiment has been carried out according to ESA/SCC recommendation for IC qualification with respect to total dose effects [10]. The chip has been irradiated in three steps to 1 Mrad, 10 Mrad and 20 MRad (SiO_2), at a constant dose rate of 21.2 Krad/min. After irradiation the chip was annealed for 24 hours at room temperature, followed by 168 hours at 100°C (accelerated life). The full set of static measurements was carried out after each step in order to assess any change in performance. The chip was under nominal bias during irradiation with the three channels switched on at maximum pre-bias.

The results of radiation and accelerated life testing show that the LLD will operate within specifications all during the experiment lifetime (10 years). The overall radiation effects are negligible or acceptable. The laser-bias current shows an increase of 5%, 10% and 15% for three different channels in the same chip (see Figure 11).

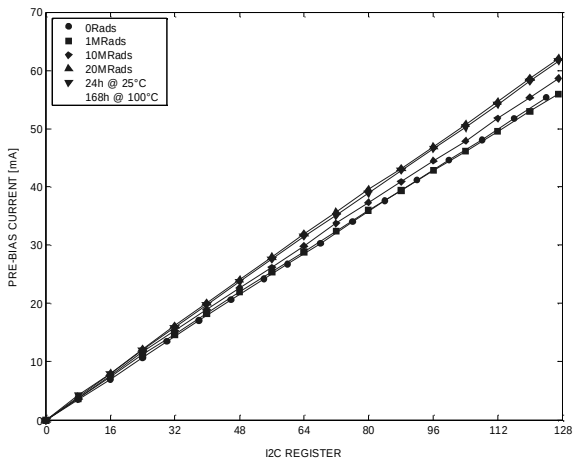

Figure 11: Pre-bias during irradiation.

This is attributed to the NMOS type V_T-referred current reference and is compatible with the previously measured threshold variations in NMOS devices. There is no significant change in the LLD differential or common-mode transfer characteristics nor in the output characteristics.

The LLD robustness to SEU needs to be tested and an experiment is being planned before the end of the year.

V. CONCLUSIONS

A Linear Laser Driver array has been developed and implemented in a commercially available 0.25 µm CMOS technology. The device has been designed to comply with the stringent CMS requirements for analogue optical transmission in the Tracker readout. It is however also compatible with digital optical transmission modes in the Tracker slow control system. Sample devices have been tested and shown to be fully functional. The switched gains can be used to equalise the significant insertion loss spread expected from the 50.000 analogue optical links. The pre-bias current is programmable over a wide range, with 7-bit resolution, allowing tracking of optical source degradation during detector lifetime. The LLD array has a modularity of three channels. However, since the channels can be individually disabled any modularity below that can also be chosen without a power penalty. The extensive set of measurements showed that the device matches or exceeds the required analogue performance. Integral linearity deviation is better than 0.5% over an input common mode range of ±350 mV. Input referred noise is less than 1 mV in an analogue bandwidth of 250 MHz. Power dissipation at maximum pre-bias is below 110 mW per channel. The radiation testing of one device showed that the analogue performance would also be maintained after a total ionising dose comparable with the one expected during the experiment lifetime. The parameters spread and yield for the tested devices are very good. Twelve devices have been tested and shown to be fully functional. The new chips will be packaged in a 5 mm x 5 mm LPCC case for ease of testing and installation in the Tracker readout and control hybrids.

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

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