

# Development of an Optical Front-end Readout System for the LHCb RICH Detectors.

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## Abstract

The development of a front-end readout system for the LHCb Ring Imaging Cherenkov (RICH) detectors is in progress. The baseline choice for the RICH photon detector front-end electronics is a binary readout ASIC for an encapsulated silicon pixel detector. This paper describes a system to transmit the binary data with address ID and error codes, from a radiation harsh environment while keeping synchronisation. The total data read out for the fixed Level-0 readout period of 900ns is 32x36x440 non-zero-suppressed bits per Level-0 trigger, with a sustained Level-0 trigger rate of 1MHz. Multimode fibres driven by VCSEL devices are used to transmit data to the off-detector Level-1 electronics located in a non-radiation environment. The data are stored in 512Kbit deep QDR buffers.

## I. INTRODUCTION

The baseline photon detector for the LHCb RICH [1] detector is the CERN/DEP Hybrid Photon pixel detector (HPD) [1] whose active elements comprise a photo-cathode, electrostatic imaging system, encapsulated pixellated silicon detector and binary readout ASIC [2]. There are 440 HPDs to be read out in 900ns, each HPD has 32x32 pixel channels. Beam Count ID, error information and parity checking information are added to the data bringing the total transmission to 32x36x440 bits per Level-0 trigger.

The intention is to use a fibre-optic data transmission scheme to export the data from the detector electronics located in a radiation environment to the Level-1 electronics, located in a non-radiation environment, the control room. A reliable and cost effective solution, that allows a reasonable tolerance on the available bandwidth is to use two fibres per HPD, each operating at a data bandwidth 640Mbits/s.

Data from the binary readout chip are interfaced to the fibre-optic link using a custom interface ASIC, the PInt chip. These data are serialised, multiplexed and driven into fibres using radiation hard Gigabit Optical Link (GOL) [3] and VCSEL [4] chips. A fibre receiver converts the incoming serial data stream to parallel data. The receivers, which are currently being investigated, will be commercial off the shelf (COTS) components. A FPGA controller checks the incoming parallel data and stores them to quad data rate (QDR) Level-1 buffers [5]. Control and synchronisation of this system is achieved by using the TTCrx [6] and LHCb Experiment Control System (ECS) [7] systems. Fig 1 illustrates the read-out chain to the Level-1 buffer for one HPD. Component availability, radiation hardness, ease of replacement, accessibility, synchronicity and cost effectiveness all need to be considered and demonstrated during the prototyping stages.

## II. ENVIRONMENT

The Level-0 electronics will be situated in the ~30 Gauss magnetic fringe field of the spectrometer magnet and will experience radiation doses of 3Krad/year [8]. A shell of ferromagnetic material provides shielding for the Level-0 electronics reducing the fields to less than 10 Gauss [9]. All Level-0 electronics will be fabricated in a 0.25µm process using radiation tolerant layout techniques to protect against the radiation dose. The radiation tolerant layout employed uses guardrings and enclosed MOS transistors that prevent leakage currents in thick field oxides and reduces the probability of single event latch up (SEL). However this does not protect against a change in bit state or transient caused by an ionising particle depositing energy in the gate region, single event upset (SEU). To minimise the effects of SEU, redundancy and error correction have been added to the control logic. Protecting data against SEU effects is thought not to be necessary if the SEU rate can be considered small. The Level-1 electronics are situated in the counting room ~100m away from the Level-0 area in a non-radiation and non-magnetic field region. The counting room can be

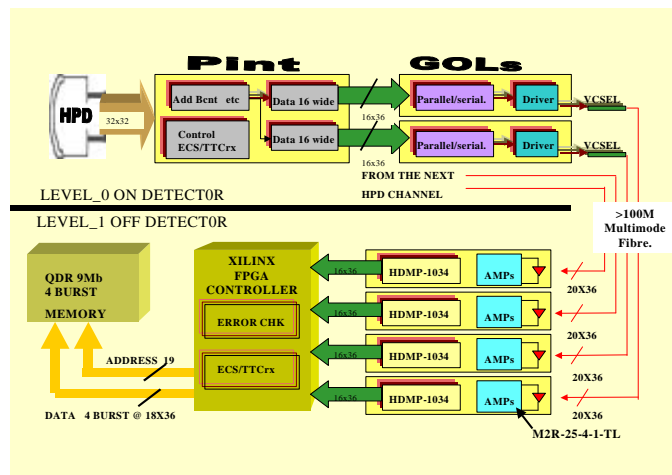


Figure 1: Illustrates the read-out chain for one HPD.

considered as an electronic friendly environment and therefore standard COTS components can be used. This has the advantage of availability, maintenance, and cost effectiveness, with a broad range of products and allows the use of FPGA devices. Error checking, error correction and self test algorithms will be built into the Level-1 electronics for ensuring that synchronisation is not lost and corrupt data are not being transmitted either to or from the Level-1 region.

### III. THE PIXEL INTERFACE (PInt) Chip

The HPD Binary Pixel chip requires an interface chip (PInt) that generates chip biasing and calibration test levels, handles the ECS (Experiment Control System) and TTC (Timing and Trigger Control). The PInt chip adds error codes, addresses, parity and bunch crossing ID to the data. The data are synchronised into two Gigabit Optical Links (GOL). The PInt is being developed using a Spartan II FPGA, and finally ported into a 0.25 $\mu$ m CMOS radiation-hard ASIC. The PInt chip controls a second level of multiplexing and serialisation of the Level-0 data before fibre transmission, see sections IV and V. Fig 2 shows the block diagram of the PInt and its supporting blocks.

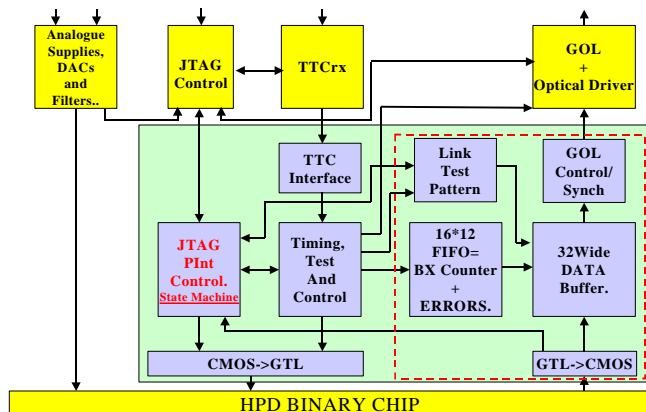


Figure 2: PInt block diagram.

#### A. Pixel Chip Configuration

The 44 internal 8 bit DACs of the Pixel Chip needed for setting the bias voltages and currents are configured using a JTAG interface. The PInt interfaces the ECS to the test access port (TAP) through a standard TAP state controller. The TAP controller is a 16 state FSM that responds to the control sequences supplied from the ECS.

#### B. Data Handling

The PInt translates all incoming signals to the Pixel chip I/O standard of GTL and outgoing signals to CMOS. The TTCrx bunch-crossing clock of 40.08MHz is used to synchronise the PInt with the Pixel, GOL chip and the LHCb system. Data coming from the HPD binary chip are of a binary format i.e. a binary '1' for a hit pixel. On a trigger Level-0 accept (average trigger rate of 1MHz) 32x32 pixels are read out to the PInt chip. A 12-bit bunch crossing ID, which is reset to zero every 3563 crossings, is taken from channel A of the TTCrx and

added as a header to the data. The bunch crossing ID is taken over preference of the event ID because of the problem of consecutive Level-0 triggers in LHCb [10]. Any error conditions that the PInt chip may have identified are then flagged in a 32bit error word. The ECS is also informed of certain error conditions to enable a decision on what action to take. Finally, the data, parity and trailer bits are added. The parity check is a generated 32-bit number consisting of the parity of each of the 32 bit wide data set.

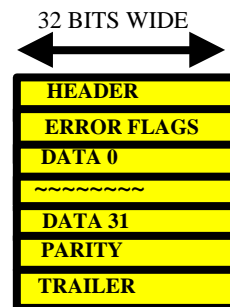


Figure 3: Event-building scheme.

The trailer is expected to use cyclic redundancy checking (CRC) which is an error detection scheme in which the block check character is the remainder after dividing all the serialised bits in a transmission by a predetermined block number. Simulations will be performed to find the most efficient block size and predetermined binary number. Parity and CRC together will show bit error location and in which way the bit has changed allowing for correction at a later stage. The PInt event-building scheme is shown in fig 3.

### IV. PARALLEL TO SERIAL Data Transmission

The (GOL) [3] chip is a multi-protocol high-speed transmitter. It is an ASIC fabricated in the 0.25 $\mu$ m process and is able to withstand high doses of radiation. The chip is to be run in the G-Link mode at 800Mbits/s and is required to transmit 20 bits of data in 25nS, 16 of which are data and the remaining 4 are overhead bits for encoding. The CIMT (Conditional Invert Master Transition) encoding scheme is employed. Before being serialised the 20-bit encoded words are time-division multiplexed into two 10-bit words. The two 10-bit words are serialised and transmitted via a VCSEL (Vertical Cavity Surface Emitting Laser) and multimode fibre. For this mode two GOLs per Pixel chip will be required. The threshold of the laser driver can be adjusted during the lifetime of the experiment with the GOL chip.

### V. FIBRE OPTIC DRIVERS

VCSELs emit light perpendicularly to their p-n junctions. High output luminosity, focussing and large spectral width allows for easy coupling with multimode fibres. Wavelengths are generally in the (650-850-1300) nm ranges [11] and output power is typically 5mW for a multimode fibre. VCSEL arrays can be easily incorporated into single ICs, which allow for a much better multiple fibre package. The VCSELs have

been proven to be very robust in terms of radiation and magnetic fields. The proposal is to use two VCSELs per pixel chip and drive 800Mb/s of data through 100 metres of multimode fibre to the LHCb counting room located in a low radiation region.

## VI. THE FIBRE OPTIC RECEIVER AND SERIAL TO PARALLEL CONVERTER

The intention is to use COTS items in the counting room region. The data are to be received by a pin diode receiver and amplifier array package and de-serialised using a Hewlett Packard HDMP1034 for the 16-bit data word. Fig 4 shows the general scheme.

Evaluation of such a scheme, in the simplex transmission mode, is currently under way using the ODIN S-Link package [12]. In this mode studies on checking synchronisation, identifying lost data etc. are being done.

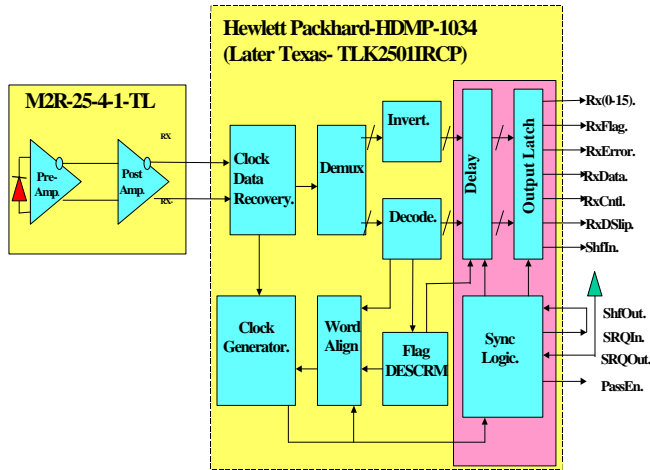


Figure 4: Fibre Optic Receiver

The S-Link is a CERN specification for an easy-to-use FIFO-like data link that can be used to connect front-end to read-out at any stage in a data flow environment [13].

If the GOL functions reliably with 32 bit data words at 40 MHz the Texas Instruments TLK2501IRCP will be considered as the receiver package. This will reduce the number of required fibres by a factor of 2.

## VII. LEVEL\_1 BUFFER

Data arriving from each of the serial/parallel converters are in a 16-bit wide, 36 word format, received at a rate of 640Mbits/s. The data contain header and error codes as illustrated in fig 3. The data, event ID and error codes are proposed to be time multiplexed and stored in the Level-1 buffer. The bunch ID is checked against the expected ID, generated at the Level-1 region using another TTCrx, and the resulting error condition carried with the event

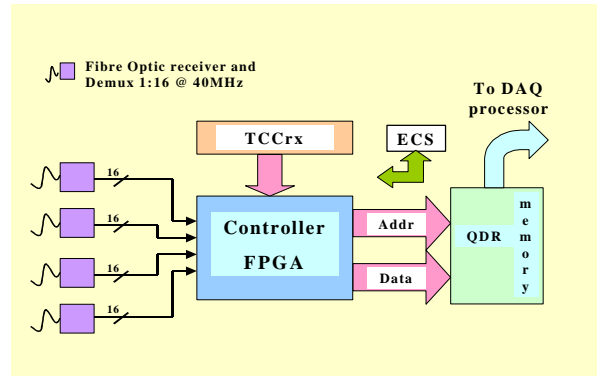


Figure 5: Level\_1 Buffer scheme

The Level-1 buffer is implemented with a commercially available QDR SRAM (Quad Data Rate SRAM) and is controlled by the FPGA QDR controller. Fig 6 shows the general scheme with the support blocks.

### A. QDR SRAM

The QDR SRAM is a memory bank of 9Mbits and can store up to 3.5K events from two HPDs pending the Level-1 trigger decision. The LHCb trigger architecture presently requires a buffer of at least 2K events. One QDR will store the data from four fibres or two HPD Pixel chips. Data can be read in and read out on the same clock edge at a rate of 333Mbits/sec. The QDR architecture is shown in Fig 6 and the key points of this device are:

- 9-Mbit Quad Data Rate Static RAM. (migration to 64Mb).
- Manufacturers: Cypress, IDT, Micron and NEC.
- Separate independent read and write data ports support concurrent transactions.
- 4-word burst for reducing address bus frequency.
- 167MHz clock frequency (333MHz data rate).  
Migration to 250MHz (500MHz data rate).

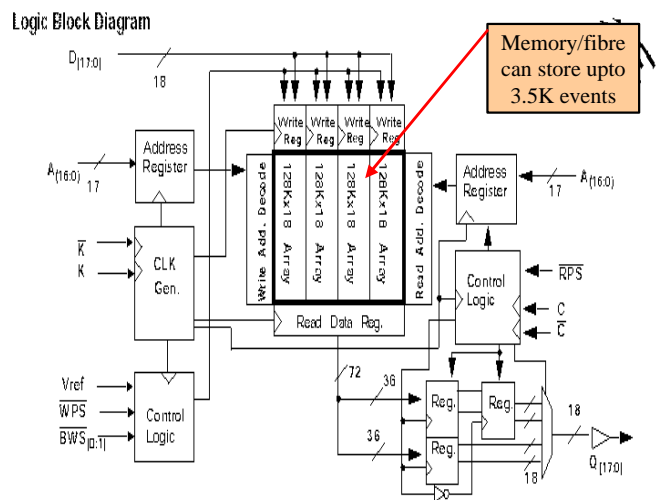


Figure 6: QDR SRAM Architecture

The QDR is a four-burst device and requires only one write address to be generated to store four 18-bit words. This therefore means that addresses are generated at a rate of 40MHz while the data are being transferred at 160MHz. This allows a data word from each of the four receivers to be

stored in one bunch crossing. Reading of the data is a similar process but the read address has to be on an alternative K clock edge to the write address, where the K clock is the QDR clock (80MHz).

More detail on the timing is given in section B below. As the data from the receivers are in 16 bit words and the QDR accepts 18-bit words, the remaining 2x36 bits of the memory can be used for error flagging and data validation in the following processing stages. The transmission check will consist of a coded 1x36 bit word that is stamped onto the side of an event.

### B. QDR Controller

A Xilinx Spartan-II XC2S200 FPGA is used as the controller chip. The device offers 284 I/Os with access times of 200MHz, internal clock speeds of 333MHz, 1176 control logic blocks and 5292 logic cells and is a low cost item. Internal Delay Lock Loops (DLL) are used for clock multiplication. The Spartan-II is programmable directly by JTAG or PROM.

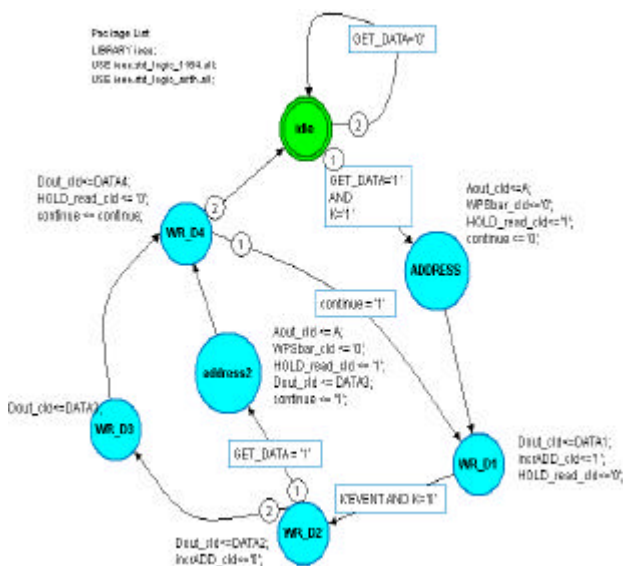


Figure 7: Write state machine.

The Level-1 buffer logic is built around two state machines: a write machine shown in fig 7; and a read machine, which is very similar in operation but receives different control signals. The “One Hot” state machines ensure the correct timing of the QDR read/write signals by forcing a read/write on a rising edge of the QDR K clock (80MHz) and then passing data from/to the QDR on every edge of the K clock for four edges. The state machine operates at 160MHz.

The write machine is activated on the 40MHz clock and the RXREADY flag when data are ready to be stored. Every time the write machine is activated a wrap around counter is incremented by 1. This counter is used for the QDR write address. Two counters generate the read address. The “offset counter” counts in multiples of 36 on every Level-1 trigger to ensure that the read pointer starts at the beginning of an event. On receipt of a Level-1 trigger accept the read machine is activated and cycles 36 times consecutively, incrementing the

“sub counter” each time. The “sub counter” is reset after reading out one complete event. Logic has been incorporated into the design to ensure the read and write pointer cannot overtake each other.

The Level-0 trigger has a 1MHz sustainable rate whereas the level-1 trigger is a variable ~40KHz rate. For this reason the write machine always has the priority over the read machine. To allow for this, Level-1 triggers and decisions are buffered. Fig 8 shows a simulation of data flow to and from the QDR for a condition where continuous write and read signals are requested. After an initial one K clock delay for both read and write the four 18-bit data words are read in and out of the device in one bunch crossing. The cursor is at the beginning of a write sequence. With the rising edge of K and “NOT wpsbar” the write address is taken from the input port “sa”. On the following rising edge of K and for three consecutive edges thereafter, data are stored to the QDR. Data read from the device use the same principle as the write procedure but “rpsbar” is the control signal. The “wpsbar” and “rpsbar” signals should not appear on the same rising edge of the K clock. The data in this simulation are arbitrary.

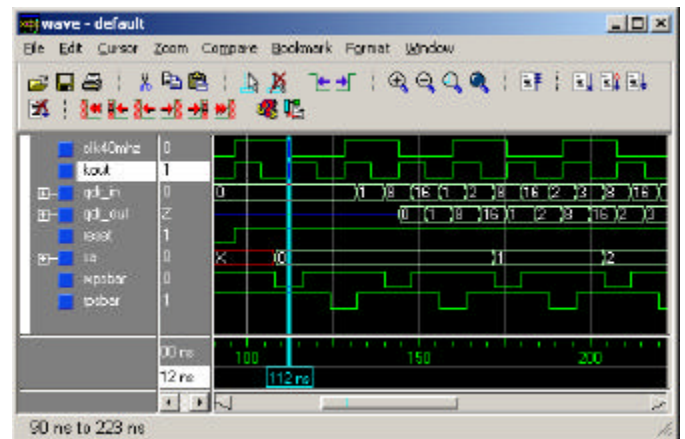


Figure 8: QDR wave-from

### C. TTCrx and ECS

Both the QDR and Spartan-II have boundary scanning facilities that will be used in production tests. The Spartan is also programmable via a JTAG interface. The ECS will be used to deliver the configuration signals.

The controller chip requires a bunch-crossing clock, reset, bunch ID and Level-0 and Level-1 trigger information from the TTCrx. For the Level-0 information the TTCrx is used in the same way as for the Level-0 board (see Section III) but instead of the local bunch ID being added as a header it is compared against the header on the incoming Level-0 event for transmission checks. The local Level-0 bunch ID will be stored in 16 deep derandomiser buffers to track the on detector Level-0 process. The resulting bunch ID header check is stored as part of the 1x36 bit error word (see Section VII-A).

The short broadcast port of the TTCrx will be used for trigger information, reset and event ID. This has a limited number of bits (~8) that can be sent but does support the necessary bandwidth (~2MHz). Six bits of the eight are user configurable and are being defined by the LHCb collaboration according to the experiment requirements. Two bits have been allocated for event ID so that they can be compared with the two LSBs of a locally generated event ID to ensure that the Level-1 buffers have not lost any fragments or synchronisation.

### VIII. TEST BED

Test boards have been built to check timing, chip programming, TTCrx compatibility and QDR functionality.

The test bed has been made in a modular fashion, utilising a Spartan-II demonstration board [14] and two PCB's. One PCB is for interfacing to the TTCrx test board and the other for the QDR.

The demonstration board is equipped with a Spartan-II XC2S100 in a PQ208 package. The speed performance does not differ from the proposed final chip, XC2S200, but the packaging limits the amount of I/Os that can be made available to the user, in this case 196. For this reason only the essential ports of the TTCrx have been utilised and the number of data-in ports have been limited. To emulate the event data coming from the receivers a pattern generator is used for one of the 16-bit wide ports, the other three ports have fixed binary numbers set internally on the chip.

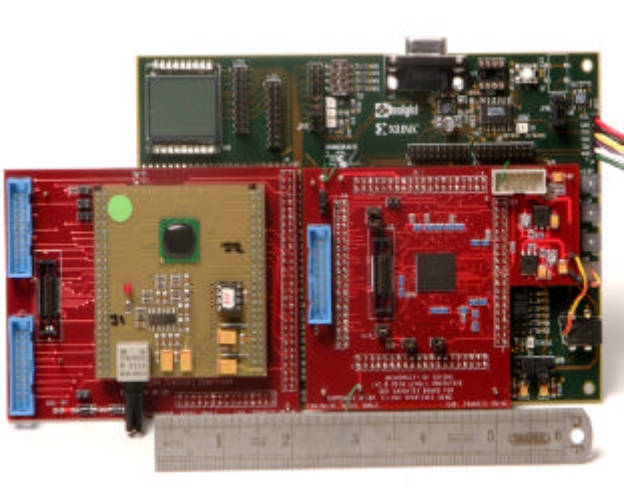


Figure 9: Spartan/QDR/TTCrx test board

A mezzanine board has been produced and locates on top of the FPGA I/O connector. This board has a QDR on it along with all the necessary power supplies and termination required for running the QDR chip. The QDR controller FPGA has its I/O configured as HSTL to suit the I/O voltage level of the QDR device.

The TTCrx used at this design stage was delivered pre-mounted to a test board [15]. The test board contains the TTCrx IC, an integrated detector and preamplifier, a serial configuration PROM (XC1736D) and a fibre optic post-amplifier. Unfortunately the test board is not compatible with the Spartan-II demonstration board user area that route 30 of the FPGAs I/O to a breadboard area. Therefore a TTCrx test board fan out PCB has been produced to translate to the Spartan-II demonstration board.

Fig 9 shows the assembled modules. Testing these boards is now in progress.

### IX. FUTURE PLANS

A complete prototype HPD to Level-1 readout system for one HPD will be constructed over the next year. The prototype will, as closely as possible, match the specifications of the final design. This will allow full testing of a complete unit and show compatibility of the selected components.

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