

Design and Test of a DMILL Module Controller Chip for the ATLAS Pixel Detector.

R. Beccherle

INFN Genova, Via Dodecaneso 33, Italy
Roberto.Beccherle@ge.infn.it
on behalf of the
Atlas Pixel Collaboration [1]

Abstract

The main building block of the Atlas Pixel Detector is a module made by a Silicon Detector bump bonded to 16 analog Front-End chips. All FE's are connected by a star topology to the Module Controller Chip (MCC) with data push architecture. MCC does system configuration, event building, control and timing distribution. The electronics has to tolerate radiation fluences up to 10^{15} cm^{-2} 1 MeV in equivalent neutrons during the first three years of operation.

The talk describes the first implementations of the MCC in DMILL (a $0.8 \mu\text{m}$ Rad-Hard technology). Results on tested dices and irradiation results of these devices at the CERN PS, up to 30 Mrad, will be presented. 8 chips were operating during irradiation and allowed to measure SEU effects.

I. INTRODUCTION

The ATLAS pixel detector [2] is constituted of 3-barrel layers and of 3 forward and backward disks. The barrels are at 5.05, 8.85 and 12.25 cm from the beam, with a tilt angle of 20° and a total dose of 30 Mrad for the innermost layer (B-Layer) is expected after 3 years of operation. Each barrel is organized into staves and each disk into sectors; both of them are in turn composed of modules. 1744 identical modules will be used in the whole detector.

The Module Controller Chip (MCC) is an ASIC, which provides complete control of the Atlas Pixel Detector module. Besides the MCC the module hosts 16 FE chips bump-bonded to a silicon detector [3].

The talk is divided in three sections. In the first section we describe the requirements that the MCC has to fulfil. Main features of this device are the ability to perform event building which provides some data compression on data coming from 16 Front-End chips read out in parallel. Output data stream is transmitted on one or two serial streams allowing a data transfer up to 160 Mbit/s. The system clock frequency is 40 MHz. First a prototype and then a full version of the chip were designed and tested. The second section describes the test set-up developed in Genova, which allows a comparison between the actual chip, hosted in a VME board,

and a C++ model simulating the chip. Test results of both chips will be presented in the third section. We focus on the irradiation tests, which allowed us to operate the chip while irradiating it, and this allowed performing detailed SEU studies.

II. SYSTEM DESCRIPTION

16 analog FE chips and a digital Module Controller Chip make the electronics part of the Atlas Pixel Detector. The interconnections have been kept very simple, and all connections that are active during data-takings use low voltage differential signalling (LVDS) standards to reduce EMI and balance current flows. The data link topology from the 16 FE's to the MCC in a module is a star topology using unidirectional serial links. This topology has been chosen to improve the tolerance of the whole system to individual FE failure, as well as to improve the bandwidth by operating the serial links in parallel.

FE chips electronics is organized in 18 columns and 160 rows of $50 \times 400 \mu\text{m}^2$ pixel cells. These chips provide 7-bit charge information using a time-over-threshold front-end design. Time over threshold information is digitised using the 40 MHz beam crossing rate. Event data coming from the FE chips are already formatted and are provided as soon as possible using data push architecture. This is done by the digital End of Column logic built-in in each chip. MCC has to perform event building collecting events from all 16 FE chips. In order to be able to perform this task, data from each link are buffered into a 21×32 bit deep FIFO. All FIFO's are full custom blocks, while the remaining part of the chip was built using the DMILL standard cell library. As soon as one complete event has been received from the FE chips and stored in the FIFO's, the MCC starts event building. Formatted data are sent to the output using one or two serial streams that can provide a total data transfer up to 160 Mbit/s.

Besides event building the MCC has also to perform system configuration, by a serial protocol, being the only electronics part of the module able to communicate with the Read Out Driver (ROD). In order to perform this task a serial command decoder has been implemented. This is a crucial part of the chip and particular effort has been put into its

realization in order to ensure a high tolerance to single bit flips in the data being received. The protocol is divided in two main classes, Data Taking mode and Configuration mode and it is not possible to mix these two states, by construction, even with single bit flip. This is especially important in case of a noisy environment and for the B-layer, where high SEU induced effects are expected. Another feature of the command decoder block is the ability to reset its circuitry without the need of a power up reset or a hard reset pin. Each FE chip is independently accessible in order to be able to configure it through a set of dedicated commands. MCC configuration information is stored in a Register Bank.

The chip has also to ensure synchronization between all events and to distribute Trigger commands to all FE's. Trigger and Timing Circuitry block (TTC) performs this task. In case of any error in event reconstruction, due, for example, to a data overflow in the internal FIFO's, synchronization is guaranteed and error words are added to the data stream in order to correctly flag the failure.

In addition to the main functions also a self-testing capability of all internal structures has been added to the chip. This test capability is a key feature in order to be able to build, test and operate with reliability a complex system such as the ATLAS Pixel Detector module. As an example, implemented test structures allow for testing the correctness of event builder, writing FE events into the internal storage structures as if they would come directly from the FE chips. This is done using the serial data protocol. In order to verify the correctness of event building, simulated events can be downloaded to the MCC first and are then reconstructed and formatted by the event builder and transmitted back to the off detector electronics (ROD).

After a first chip, built using AMS 0.8 μm technology, which was successfully used to build complete modules and used in test beam, we decided to implement a rad-hard version of the MCC [4]. The chosen technology was DMILL, a 0.8 μm rad-hard technology, for its similarities, in terms of design rules, with the AMS one.

We developed two successive versions of the MCC called MCC-D0 and MCC-D2. The first chip is a simple test chip containing only one full custom FIFO, the complete command decoder and the register bank. The main goal of this chip was to understand eventual technology issues and to perform an irradiation at the CERN PS proton irradiation facility. As described later in the paper the chip was successfully irradiated up to 30 Mrad. The second chip developed using this technology (MCC-D2) is a full version of the module controller chip and is therefore suited to build complete rad-hard modules.

III. TEST SETUP

The main difficulties in testing a chip like the MCC is by far the ability to fully debug, during the chip design phase, and then to test the correctness of the event building algorithm and all its possible exceptions. Also the verification of the correctness of the Trigger distribution to the FE chips without

loss of synchronization presents many challenges. The MCC has to distribute LEV1 triggers to the FE's. Up to 16 Trigger commands can be received by the MCC. Each time the MCC receives a Trigger command a counter is incremented. As soon as all FE's have sent a complete event the counter keeping track of the received triggers is decremented. If more than 16 triggers have to be processed the trigger command is dropped and an empty event is generated by the MCC in order to keep up with event synchronization. Therefore the overflow mechanism strongly depends on all 16 concurrent FE data streams and is therefore very hard to recreate both in the laboratory and in the Verilog simulation used to validate the chip. In order to overcome these challenges we decided to develop a VME based test board (MCC exerciser) that allows us to completely simulate MCC input data. A C++, timing oriented, simulation package that is part of a larger simulation environment, developed in Genova, and called SimPix, controls the board.



Figure 1: MCC exerciser board with two mounted memory cards.

The MCC exerciser board, see Figure 1, is a standard VME board that can host a packaged version of the chip. On the motherboard we can plug-in 10 smaller "memory cards". Each of them is equipped with two 8 Mbit deep memory banks and can either store data to be transmitted to the MCC or can sample data lines coming from the MCC. In a typical laboratory test we use 16 channels to simulate FE data, one channel to simulate data commands coming from the ROD, and the last channel is used to sample one MCC output data line. Two other channels are used to sample, for example, other MCC I/O's. The whole board is synchronous with a system clock of 40 MHz. Up to 200 ms of operation can be simulated with this set-up. SimPix provides input data to the memory cards using a 32 bit wide VME bus interface.

SimPix is a modular simulation program, written in C++, which allows us to simulate the whole ATLAS Pixel Detector starting from physics data. A block diagram describing its main features is presented in Figure 2. The input data to the simulation can be provided both by random selected data and by means of a GEANT simulation of the whole detector. LEV1 triggers can be generated both randomly and according to the ATLAS trigger specifications. Data produced by this first step are then sent to 16 FE models which in turn produce

the correct inputs for the MCC. Data processed by the MCC are then analysed by an automatic analysis tool that flags possible mismatches. The peculiar aspect of this simulation environment is the modular approach that allows one to replace each component, FE or MCC model, with a similar description that can be at a different level of accuracy. This is very useful for example if one wants to simulate different versions of the FE chip. Therefore different models are provided in order to be able to simulate an ideal FE or a model that follows, as closely as possible, the real hardware implementation. Being the simulation time oriented, one can simulate the input/output of each electronics component down to the single clock cycle. In the case of the MCC this approach is pushed forward and besides an ideal model and a full C++ simulation of the chip one can actually replace the MCC module with a Verilog simulation of the chip running on a remote workstation. This is accomplished by some routines that use TCP/IP to interface two different machines on a network. This approach, in which one runs at the same time the Verilog and the C++ model of the chip, allows to quickly comparing results as the chip is being developed. Another option is to directly interface the simulation software to the MCC exerciser board previously described. In this case the software interfaces to the VME crate hosting the actual hardware. Using the same approach one can also interface directly to a logic state analyser. This approach has been proven very useful in order to perform both development and test of the whole chip.

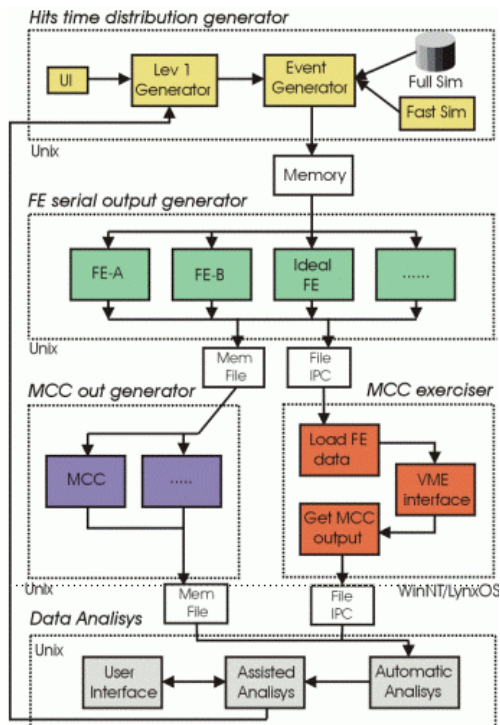


Figure 2: SimPix block diagram.

IV. TEST RESULTS

In this section we present the results of the tests performed on both chips designed in Genova using the DMILL 0.8 μm

rad-hard technology. The design of both chips was done starting with a Verilog behavioural model and using Synopsys as synthesis tool to map the design to the standard cell library provided by the foundry. Layout was performed using Cadence Cell Ensemble. DRC and LVS were performed on a completely flat design. The only step of the standard design flow that was not performed was a simulation of the circuit using extracted values for capacitance after the layout was completed due to some problems in the provided design kit. On both chips all the full custom blocks were hand placed and the clock tree was done using a distributed buffer as a clock tree generation tool was not provided.

Both chips were tested in the laboratory, after packaging them, using the MCC exerciser board and a logic state analyser. The MCC-D0 chip was also tested at the CERN PS proton beam and irradiated up to 30 Mrad.

A. Tests of the MCC-D0

The first chip, MCC-D0, is a test chip developed in order to test the new technology. This chip contains a 21 bit wide and 32 words deep full custom FIFO designed using a conservative 12 transistors layout. In addition to the FIFO a command decoder and a register bank were implemented. Up to 40 configuration bits can be stored in the register bank. The main goal of this version of the chip was to irradiate it at the CERN proton irradiation facility in order to be able to perform SEU studies.

For this purpose some special functions were added to the chip in order to maximize the test that could be performed during irradiation. For example, the information of a detected bad command is stored inside an error register during irradiation. By reading such register we have been able to quantify the effect of induced errors.

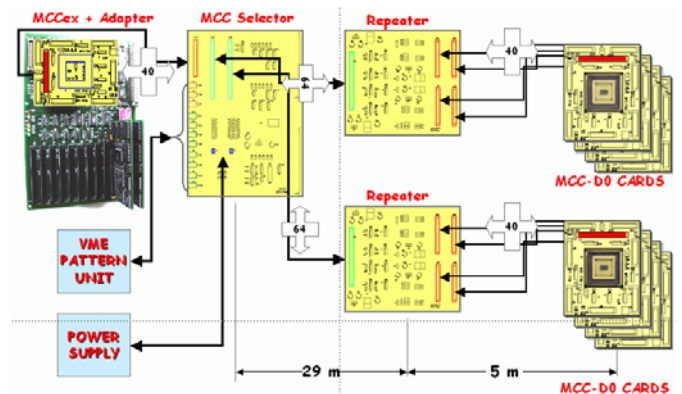


Figure 3: MCC-D0 test beam set-up. Data taking was active during irradiation and this allowed for SEU studies.

In order to perform the irradiation test a dedicated test system was built. This test set-up is shown in Figure 3. Up to 8 chips can be irradiated at the same time in the set-up. All chips are mounted on support cards, which only have passive components. These boards are connected to repeater cards, located 5 m away from the beam. The repeater cards are connected, by a 29 m long flat cable to the selector card that essentially implements a multiplexer allowing selecting one of the 8 support cards as being active. The selector board is

controlled by means of a standard VME bus by the MCC exerciser that is in turn controlled by SimPix. This set-up therefore allows addressing all 8 chips, only one being active at a time.

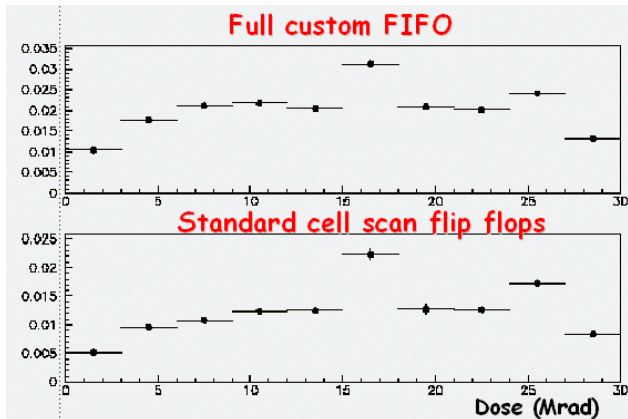


Figure 4: The upper plot shows results for a 12 transistor based memory cell, while the second one is for standard cell memory cells.

The CERN PS proton irradiation facility has a bunched beam, with one or two 200 ms bursts every two seconds.

We synchronised our data taking with the start of burst in order to be able to operate the chips during irradiation. We performed two different tests, a dynamic one on the actual active chip and a static one on the remaining 7 chips. After each bunch the active chip was changed. The dynamic test consists in continuously write, read and compare data in the FIFO and configuration registers. After that we read out data from the chip checking that all commands were correctly recognized by the MCC and if some bit flipped inside the data structures. Each read operation was performed three times, in order to ensure that no transmission error occurred during the readout phase. The static tests instead, consisted in writing a known data configuration pattern in the MCC data structures before each beam spill and in reading out data after the spill in order to evaluate the bit flip probability. To select the 8 good chips we performed a test in the laboratory on packaged chips, because they were not tested at the production site. We tested 14 chips and 11 turned out to be working perfectly. During this test we measured power consumption, maximum clock frequency and checked that all writ able structures were correctly addressable. Maximum working clock frequency turned out to be ~ 90 MHz. All working chips were in perfect agreement with synthesis and simulation results.

All chips were successfully irradiated up to 30 Mrad. After irradiation all chips were perfectly working but after some days of cooling down four of them stopped to respond to any command. We also tried to anneal them in an oven at 100 C° for one week without being able to make them working again. We suppose that this problem is related to our full custom LVDS I/O pads design that in fact showed no activity on the non-working chips. We performed the same measurements done before irradiating the chips on the four remaining chips and compared the results. The only measured difference was a reduction of the maximum clock frequency of about 40%.

Anyway, even after this frequency reduction, the chips were still functional at the LHC working frequency of 40 MHz.

SEU measurements, presented in Figure 4, show almost no errors in the dynamic test and a pure static bit flip probability per burst of 1.2% for data stored inside a standard cell scan flip-flop and a probability of 2% for the full custom, twelve transistor design, FIFO memory cell.

B. Tests of the MCC-D2

The second chip developed by our group is a complete version of the MCC that is compliant with the ATLAS Pixel specifications. The goal of this second chip was to be able to implement, together with a DMILL version of the Front End chips, a rad-hard version of the ATLAS Pixel Detector module. The foundry did not test these chips and therefore we packaged 19 of them in order to be able to test them with our test set-up. We performed three different types of tests on the chips: first a DC test to measure static power consumption, then a test with the logic state analyser in order to test some simple patterns on the FIFO's and on the Register Bank at different clock speeds, and finally a functional test with the MCC exerciser, in order to fully debug the event building circuitry of the chip. Results of these tests are shown in Table 1.

Table 1: Test results of MCC-D2: in the first column of the table DC current measurements are shown while in the second one the maximum working clock frequency is reported. The last two columns show how many chips passed the logic state analyser and/or the MCC exerciser test. Finally in the last row the total chip yield after each test is shown. Both fully working chips passed all test only operating them at a frequency of 33 MHz.

Chip #	DC test	Max ck	LSA test	MCC ex test
1	24 mA	74 MHz	OK	Failed
2	22 mA	72 MHz	OK	Failed
3	34 mA	73 MHz	OK	Failed
4	Failed	-	-	-
5	21 mA	74 MHz	OK	Failed
6	21 mA	73 MHz	Failed	-
7	20 mA	72 MHz	OK	Failed
8	Failed	-	-	-
9	20 mA	73 MHz	OK	Failed
10	Failed	-	-	-
11	18 mA	73 MHz	OK	OK @ 33 MHz
12	30 mA	72 MHz	OK	Failed
13	22 mA	75 MHz	Failed	-
14	19 mA	74 MHz	OK	Failed
15	41 mA	73 MHz	Failed	-
16	21 mA	74 MHz	OK	Failed
17	18 mA	75 MHz	Failed	-
18	Failed	-	-	-
19	21 mA	74 MHz	OK	OK @ 33 MHz
Yield		84%	58%	11%

DC measurements showed a power consumption of 20 to 40 mA, in agreement with expectations. The maximum working clock frequency turned out to be in a range between 70 and 75 MHz that is in quite good agreement with synthesis

results that predicted 78 MHz. One has to remember though, that we did not perform a simulation of the chip after extracting parasitic capacitor values from the layout and that therefore we rely entirely on wire load models. It is worth to remember that the test done with the logic state analyser did not cover all possible timing paths in the chip; we expect it covers ~10%. This test also allowed a detailed study of the Command Decoder built in the chip that performed very well, meeting all specifications. Also, by design, the Command Decoder should be able to initialise itself into a well-known state in order to be able to operate the chip without a hard reset pin or a power-up reset, but only issuing a global reset command. This feature worked flawlessly.

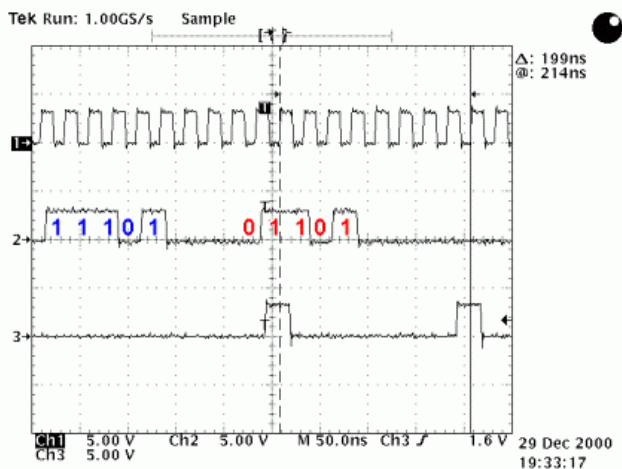


Figure 5: Trigger commands without and with bit flip. In the graph we can see the 40 MHz system clock, the serial input line with of the MCC the two Trigger commands. The last line shows the MCC output line and one can see that the timing information between commands is preserved.

Another implemented and tested feature was the ability to distinguish between two consecutive Trigger commands and to correctly detect correct timing information even in case of a single bit flip in the input data line during the Trigger command. This can be seen in Figure 5.

11 out of 19 chips passed these first two tests. The last test, for which we calculated a system coverage of ~70% was performed doing real event building using the MCC exerciser. Results of these tests are also presented in Table 1 and one can see that only 11% of the chips turned out to be fully functional after these tests. One thing to note though is that both working chips had to be operated at only 33 MHz in order to get correct results. This discrepancy with synthesis results can both be due to the lack of simulation of a netlist that included parasitic capacitor extracted from the actual layout or to an incorrect timing in the synthesis models.

As we can see the results of these test show an unacceptable low yield and some problems in the design

technology and/or it's modelling. Some rough calculations made taking also in account DMILL forecasts for a digital chip of this size should have provided a yield of 20, 30%. Much more detailed studies on these results should have been performed in order to accept this technology for our needs.

In our collaboration also two distinct versions of the analogue Front End chip, also developed in DMILL, were submitted within the same reticule and these chips turned out to have a yield that was lower than 1%.

V. CONCLUSIONS

In this paper we presented test results of two chips that were submitted by the Genova group of the ATLAS Pixel Collaboration to DMILL, a 0.8 μm rad-hard technology. One test chip was tested and successfully irradiated up to 30 Mrad at the CERN PS proton beam facility. SEU studies have been performed on this chip operating the chip while irradiating it. Results showed that this technology, from the radiation tolerance point of view, is suitable for the ATLAS Pixel Detector even for the innermost layer. In addition we presented test results of a full version of the ATLAS Module Controller Chip. These results show some severe yield problems (11% on 19 tested dices) and problems in the timing models of the libraries that produced a chip working only at 33 MHz, despite of the synthesis results that showed 78 MHz.

This, connected to the fact that also the FE chip of our collaboration, submitted on the same reticule of the MCC, showed a very poor yield result (less than 1%) made our collaboration decide to temporarily drop this technology in order to explore the 0.25 μm technology, with rad-tolerant layout techniques, developed at CERN. Therefore the collaboration will submit a new version of both the FE and the MCC in this technology in October this year.

VI. REFERENCES

- [1] ATLAS Collaboration, Pixel Detector TDR, CERN/LHCC/98-13, 1998
- [2] G. Darbo, The ATLAS Pixel Detector System Architecture, Proceedings of the "Third Workshop on Electronics for LHC Experiments", London, CERN/LHCC/97-60 (1997), pp. 196-201.
- [3] R. Beccherle, The Module Controller Chip (MCC) of the ATLAS Pixel Detector, Proceedings of the "Nuclear Science Symposium", Montreal, Canada, (1998).
- [4] P. Natchaeva et al., Results on 0.7% X0 thick pixel modules for the ATLAS detector, Proceedings of "Pixel 2000", Genova, Nuclear Instruments and methods in Physics Research A 465 (2001), pp. 204-210.