

The ALICE on-detector pixel PILOT system - OPS

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Abstract

The on-detector electronics of the ALICE silicon pixel detector (nearly 10 million pixels) consists of 1,200 readout chips, bump-bonded to silicon sensors and mounted on the front-end bus, and of 120 control (PILOT) chips, mounted on a multi chip module (MCM) together with opto-electronic transceivers. The environment of the pixel detector is such that radiation tolerant components are required. The front-end chips are all ASICs designed in a commercial 0.25-micron CMOS technology using radiation hardening layout techniques. An 800 Mbit/s Glink-compatible serializer and laser diode driver, also designed in the same 0.25 micron process, is used to transmit data over an optical fibre to the control room where the actual data processing and event building are performed. We describe the system and report on the status of the PILOT system.

I. INTRODUCTION

A. Detector

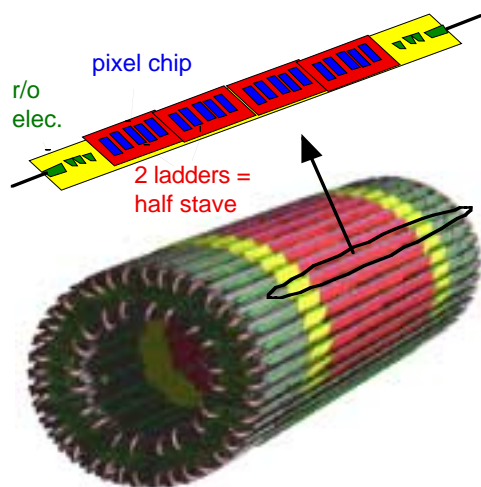


Figure 1: ALICE Silicon Pixel Detector

Two ladders (5 pixel chips each), mounted on a front-end bus, constitute a half-stave. The complete detector consists of 120 half-staves on two layers, 40 half staves in the inner layer, 80 in the outer layer. The detector is divided into 10 sectors (in ϕ -direction). Each sector comprises two staves in the inner layer and four staves outer layer. Thus one detector sector contains six staves. Fig. 1 illustrates the ALICE silicon pixel detector. [1, 2]

B. Design considerations

Table 1 summarizes the main design parameters of the readout system.

Table 1: System parameters

L1 latency	5.5 μ s
L2 latency	100 μ s
Max. L1 rate	1 kHz
Max. L2 rate	800 Hz
Radiation dose in 10 years	< 500 krad
Neutron flux in 10 years	$3 \times 10^{11} \text{cm}^{-2}$
Total number of pixels	9.8184×10^6
Occupancy	< 2%

Although the L1 trigger rate and the L2 trigger rate are low compared to other LHC experiments, the raw data flow yields almost 1 GB/s.

The expected radiation dose and the neutron flux are at least one magnitude of order lower compared to the ATLAS or CMS experiments. However, commercial off-the-shelf components can still not be used. Therefore, the ASICs have been developed in a commercial 0.25-micron CMOS technology using radiation hardening layout techniques [3]. Precautions have been undertaken to reduce malfunction due to single event upset. A minimum of data processing is performed on the detector, which subsequently simplifies ASIC developments.

II. SYSTEM ARCHITECTURE

A. System overview

Fig. 2 shows a block diagram of the system electronics. The 10 pixel chips of one half stave are controlled and read

out by one PILOT multi chip module (MCM). The PILOT MCM transfers the data to the control room. In the control room 20 9U-VME-based router cards, two for each detector sector, receive the data. One router card contains six data converter daughter boards, one for each half stave. The data converters process the data and store the information in an event memory. The router merges the hit data from 6 half staves into one data block, processes the data and stores them into a memory where the data wait to be transferred to the ALICE data acquisition (DAQ) over the detector data link DDL [4].

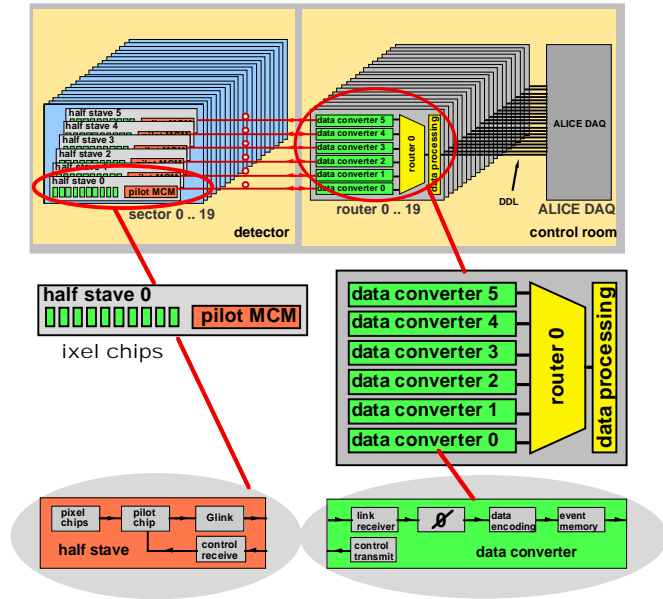


Figure 2: System block diagram

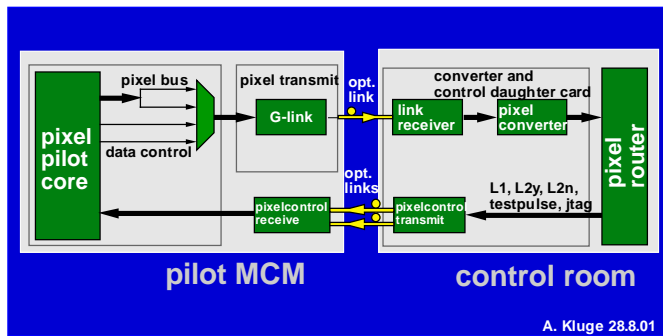


Figure 3: Read-out chain

B. PILOT logic and optical pixel transmitter

Fig. 3 illustrates a block diagram of the read-out chain. When the ALICE DAQ issues a L1 trigger signal, the pixel router forwards the signal via the pixel control transmitter and the pixel control receiver to the PILOT logic. The PILOT chip asserts a strobe signal to all pixel chips [5], which stores the delayed hit information into multi event buffers in the pixel chips. Once a L2 accept signal (L2y) is asserted and transmitted to the detector, the PILOT chip initiates the readout procedure of the 10 pixel chips one after the other. The 256 rows of 32 pixels of a pixel chip are presented

sequentially on a 32-bit bus. The read-out clock frequency is 10 MHz. As a result, the read-out of 10 chips takes about 256 μ s.

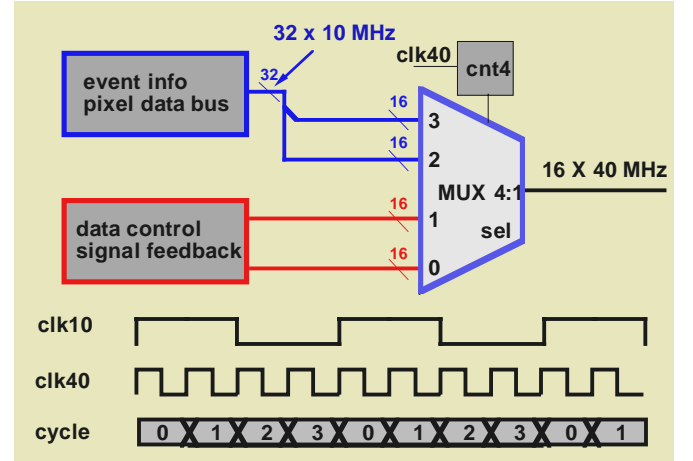


Figure 4: Transmission principle

The PILOT logic performs no data processing but directly transmits data to the control room. This approach has several advantages. The first is, that the on detector PILOT-ASIC architecture is simple. Secondly, the system becomes more reliable as the complex data processing units are accessible during operation in the control room. Finally, if the detector hit occupancy increases in the future, data compression schemes can be adapted in the FPGA based control room located electronics.

For the optical transmission of the data to the control room the encoder-serializer gigabit optical link chip GOL [6] is used. The GOL allows the transmission of 16 bit data words every 25 ns resulting in an 800 Mbit/s data stream. The data are encoded using the Glink [7] protocol. This chip has already been developed at CERN.

The pixel data stream arrives from the pixel chips at the PILOT chip on a 32-bit bus in 100 ns cycles. That means that the transfer bandwidth of the GOL is twice as high as required. The 100 ns pixel data cycle is split up into four 25 ns GOL transmission cycles. Fig. 4 shows the transmission principle. In two consecutive GOL cycles, 16 bits of pixel data are transmitted. The remaining two transmission cycles are used to transmit data control and signal feedback signal blocks. The control block contains information directly related to the pixel hit data transmission, such as start and end of transmission, error codes, but also event numbers. In the signal feedback block, all trigger and configuration data sent from the control room to the detector are sent back to the router for error detection.

Upon receipt of a L2 reject (L2n) signal the corresponding location in the multi event buffer in the pixel chips are cleared and the PILOT initiates a short transmission sequence to acknowledge the reception of the L2n signal.

C. Data converter

The serial-parallel converter receives the Glink data stream and recovers the 40 MHz transmission clock using a commercial component [8]. The implementation of the link receiver is based on a commercial FPGA and storage devices. Fig. 5 shows a block diagram of the data converter. The received data is checked for format errors and zero suppression is conducted before the data are loaded into a FIFO. The expected occupancy of the detector will not exceed 2%. As a result, it is economic to encode the raw data format. In the raw data format the position of a hit within a pixel row is given by the position of logic '1' within a 32-bit word. The encoder transforms the hit position into a 5-bit word giving the position as a binary number for each single hit and attaches chip and row number to the data entry [9]. The output data from the FIFO are encoded and stored in an event memory in a data format complying with the ALICE DAQ format [10]. There it waits until merged with the data from the remaining five staves by the router electronics.



Figure 5: Link receiver data converter

D. Pixel control transmitter and receiver

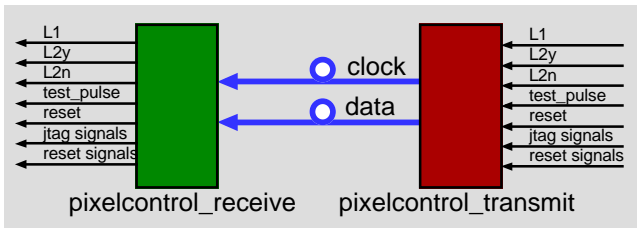


Figure 6: Pixel control block diagram

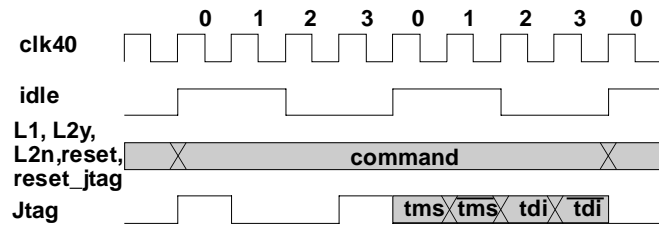


Figure 7: Pixel control data format

The pixel control transmitter and receivers are responsible for the transmission of the trigger and configuration signals from the control room to the detector. This includes the following signals: L1, L2y, L2n trigger signals, reset signals, a test pulse signal and JTAG signals.

The data must arrive at the detector in a 10 MHz binning, since the on detector PILOT system clock frequency is 10 MHz. During data read-out of the detector the JTAG access functionality is not required and vice versa. The link is unidirectional since the return path for the JTAG system (TDO) uses the Glink data link. The data protocol must be simple in order to avoid complex recovery circuitry on the detector in the PILOT chip. As a result, all commands must be

DC balanced. (The number of '1's and '0's in the command code must be equal.)

The data transmission is performed using two optical fibres, one carrying the 40 MHz clock and the other the actual data.

The pixel control transmitter (see fig. 6) translates the commands into a serial bit stream. A priority encoder selects the transmitted signal in case two commands are active at the same time. L1 is the only signal where the transmission latency must be kept constant. Therefore, a L1 trigger transmission must immediately be accepted by the pixel control transmitter and, thus, has highest priority. A conflict would arise if the transmitter were in the process of sending a command at the same time as a L1 transmission request arrives. In order to avoid this situation the L1 trigger signal will always be delayed by the time duration, it takes to serialize a command (200 ns). During this delay time, all command transmissions are postponed to after the L1 signal transmission. Thus, when the delayed L1 trigger signal arrives at the transmitter, no other command can be in the transmission pipeline.

Fig. 7 illustrates the data protocol. Four 40 MHz clock cycles form a command cycle. At start-up 64 idle patterns are sent to the receiver. The receiver synchronizes to this idle pattern. Commands are always two transmit cycles (or eight 40 MHz cycles) long. The number of different commands requires a two transmit cycle command length. After each transmission of an idle word, a transmission command can follow. Since the idle word is only 100 ns long, the transmission of a command can be started in a 100 ns binning. However, the duration of a command transmission is 200 ns long [11].

E. Fast multiplicity

The pixel chips provide an analog fast multiplicity current signal. This signal is proportional to the number of pixels being hit. As it is a current signal, the sum of all 10 chips on a half stave can be obtained by connecting the 10 fast multiplicity outputs together. The use of this signal to generate a multiplicity and vertex trigger for the ALICE trigger system is currently under investigation [12].

For the read-out of this signal, two options exist. One option is to use an A/D-converter and transmit the signal using the PILOT system and the Glink interface. The other option is to use an analog optical link [13] to transmit the information independently from the digital data stream. The draw back of the first option is the additional time delay when inserting the signal into the Glink data stream, which prohibits the use of the trigger signal in the L0 application in ALICE. The disadvantage of the second option is the need of an additional optical package. The available space for components is very restricted, as described below.

III. PHYSICAL IMPLEMENTATION

A. Pixel bus and pixel extender

Fig. 8 shows the view from the side of the mechanical assembly, fig. 9 from the top. On the bottom of fig. 8, a fibre carbon structure and the cooling tube can be seen which holds the detector components. The pixel chips and the sensor ladders are bump-bonded and directly glued on top of the fibre carbon structure. On top of the assembly the pixel bus is glued. The pixel bus is an aluminium-based multi layer bus structure, which provides both power and data to the chips. The connections between the pixel bus and the ladder assembly are made by wire bonds. Passive components are soldered on top of the pixel bus. The PILOT MCM is attached to the structure in a similar way. Two copper bus structures, known as the pixel extenders, supply the pixel bus and the PILOT MCM with power.

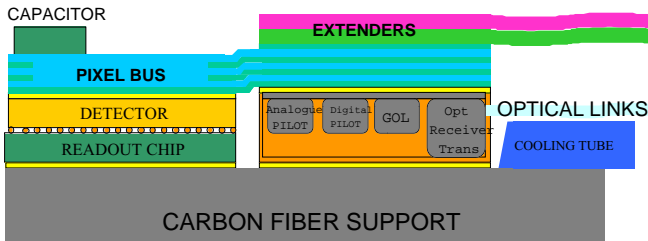


Figure 8: Pixel bus and extender

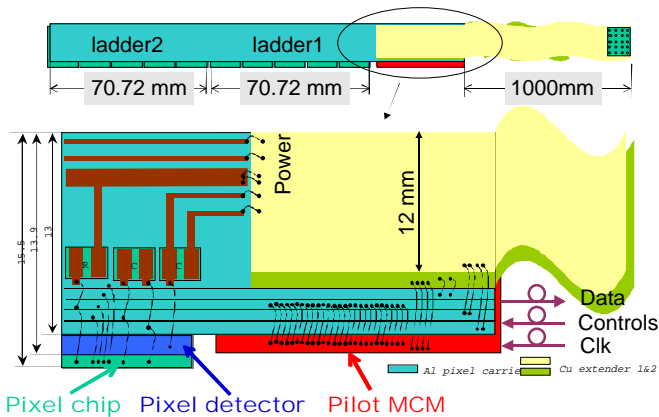


Figure 9: Pixel bus and extender (top view)

B. PILOT MCM

Fig. 10 shows a diagram of the PILOT MCM. Due to mechanical constraints, the MCM must not exceed 50 mm in length and 12 mm in width. Components can only be placed in a 5 mm-wide corridor in the middle of the MCM. A special optical package is being developed, which is less than 1.4 mm in height and houses two pin diodes and a laser diode [14].

Due to the height constraints for components, all chips will be directly glued and bonded onto the MCM without a package. Fig. 10 shows the GOL, which must be in close vicinity to the optical package in order to keep the 800 Mbit/s transmission line short. The distance from the connector to the GOL is less critical, as only 40 Mbit/s signals are connected

to the optical package. On the very left, the analog PILOT chip is shown. It is an auxiliary chip for the pixel chips and provides bias voltages.

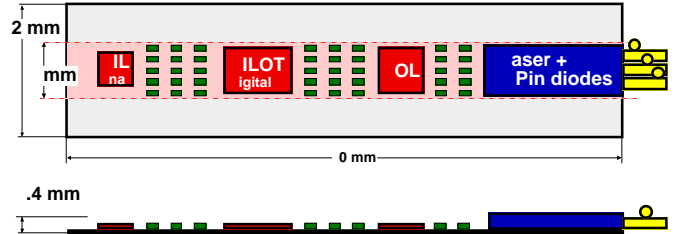


Figure 10: PILOT MCM

C. PILOT chip

The PILOT chip layout can be seen in fig. 11. The chip size of 4 x 6 mm is determined by the number of I/O pins. The chip has been produced in a 0.25 micron CMOS technology using special layout techniques to enhance radiation tolerance [3]. A comprehensive description of the PILOT chip can be found in [11, 15].

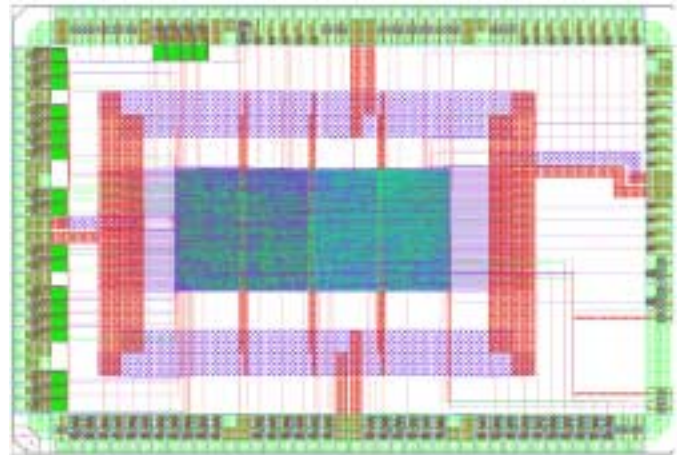


Figure 11: PILOT layout

D. GOL chip

The GOL chip has already been tested and its performance is described in [6].

E. Single event upset

Although the expected neutron fluence is comparatively low, design precautions have been undertaken to prevent single event upsets from causing malfunctions. In both the PILOT chip and the GOL chip, all digital logic has been triplicated and all outputs are the result of majority voting. Internal state machines are made in a self-recovering manner. Fig. 12 shows the principle. In case a flip-flop in a state machine changes its state due to a single event upset, the correct state will be recovered using the state of the remaining two state machines.

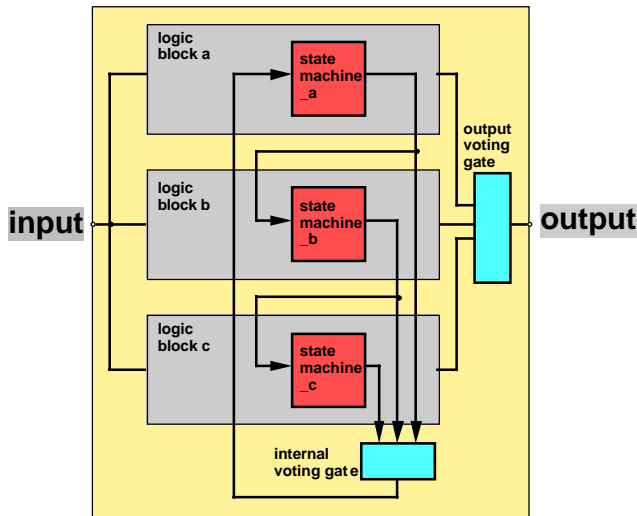


Figure 12: SEU recovery architecture

F. PILOT system test board

A PILOT system test board has been developed. The board is used to test the functionality of the PILOT chip. The PILOT chip is directly glued and bonded onto the board. An FPGA [16] provides the test patterns to the PILOT. The FPGA contains functional models of the pixel control transmitter, the ten pixel chips and the link receiver. The outputs of the PILOT chip are stored in a 128k x 48 static memory bank and can also be read back by the FPGA for comparison with the model. Access to the board, the FPGA and the RAM bank is via a JTAG port. Fig. 13 shows the block diagram of the board. In a second phase, the test will include the PILOT chip, the GOL transmitter chip and the commercial Glink receiver chip [8]. Again, the output of the data chain can be read into the FPGA and the memory bank. In a third phase the pixel bus and its 10 pixel chips will be connected to the board. This feature will allow qualification of the entire data read-out chain.

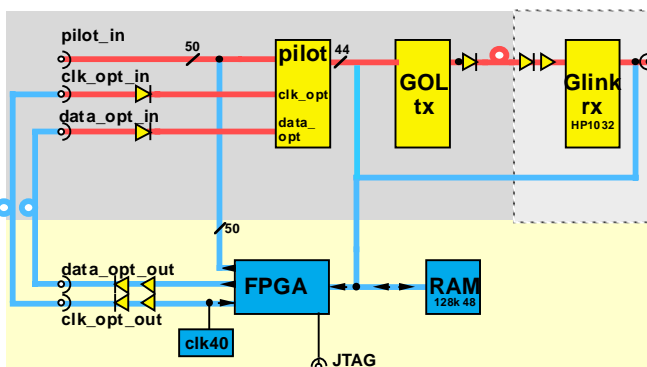


Figure 13: PILOT system test board

IV. STATUS

The GOL chip has already been tested and its performance met the specifications. Another prototype run was launched in order to enhance functionality for another application [6].

The PILOT chip has been received from the foundry [11, 15].

Tests of a prototype pixel bus have been started [17].

The link receiver [10, 11] and the router designs are in progress.

V. CONCLUSION

All chip developments have been conducted using a 0.25-micron CMOS technology and layout techniques in order to cope with the radiation dose. The on detector PILOT system performs no data processing nor requires on-chip memory. The entire data stream can be moved off the detector using the encoder and serializer chip GOL. This has the advantage that the on-detector electronics is independent from the detector occupancy and future upgrades can be performed on the FPGA based electronics located in the control room. The transmission of data is performed using optical links. The number of electrical read-out components is minimized, as the available space for physical implementation is very limited.

VI. REFERENCES

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