Progress in Development of the Analogue Read-Out Chip for Silicon Strip Detector Modules for LHC Experiments.

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Abstract

We present a new version of the 128-channel analogue front-end chip SCTA128VG for readout of silicon strip detectors. Following the early prototype developed in DMILL technology we have elaborated a design with the main goal of improving its robustness and radiation hardness. The improvements implemented in the new design are based on experience gained in DMILL technology while developing the binary readout chip for the ATLAS Semiconductor Tracker.

The architecture of the chip and critical design issues are discussed. The analogue performance of the chip before and after the gamma irradiation is presented. The performance of modules built of ATLAS baseline detectors read out by six SCTA chips is briefly demonstrated. The performance of a test system for wafer screening of the SCTA chips is presented including some preliminary results.

I. Introduction

The SCTA chip has been developed from the beginning as a backup option to the binary read-out chip ABCD [1] for the ATLAS SCT, using the DMILL technology. Currently, SCTA chips have found the following applications:

- Read-out of silicon strip detectors for the NA60 experiment.
- Production quality assurance testing of silicon strip detectors for ATLAS SCT.
- Fast read-out chip for diamond strip detectors.
- Read-out of silicon pad detectors for HPD applications.

A first prototype of the SCTA chip [2] was designed and manufactured in the early stages of stabilisation of the DMILL process. In the meantime the DMILL process has been improved and stabilised. The development of the ABCD binary readout chip helped us to understand better and quantify various aspects of the process like matching, parasitic couplings through the substrate and radiation effects. The conclusions from the work on the ABCD chip have been implemented in the new design of the SCTA128VG chip with the main goal of improving robustness and radiation hardness of the new chip.

II. Chip Architecture

Figure 1 shows the block diagram of the SCTA128VG chip. The SCTA128VG chip is designed to meet all basic requirements of a silicon strip tracker for LHC experiments. It comprises five basic blocks: front-end amplifiers, analogue pipeline (ADB), control logic including derandomizing FIFO, command decoder and output multiplexer. The detailed architecture of the front-end amplifier based on a bipolar input device has been discussed already in [3]. An advantage of this solution, compared to a pure CMOS version being developed for the CMS tracker [4], is significantly lower current in the input transistors required for achieving comparable noise levels.

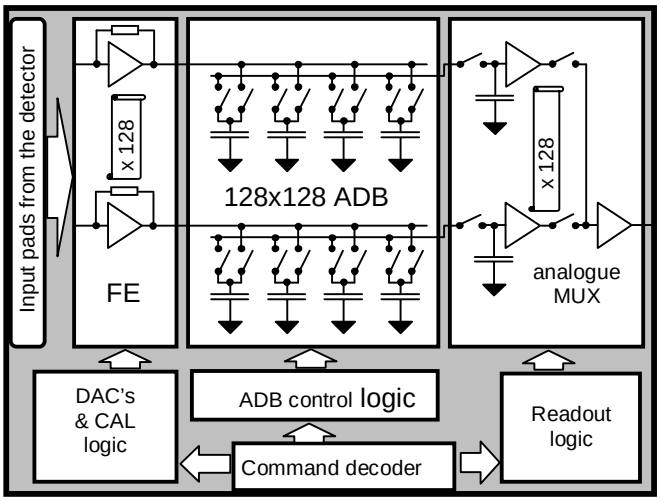

Figure 1: Block diagram of the SCTA128VG chip.

The front-end circuit is a fast transimpedance amplifier followed by an integrator, providing semi-gaussian shaping with a peaking time of 16 to 24ns. This dispersion of peaking times is for the full range of expected process variations. The design peaking time for nominal values of resistors and capacitors is 20ns. The peak values are sampled at 40 MHz rate and stored in the 128-cell deep analogue pipeline (ADB). Upon arrival of the trigger the analogue data from the corresponding time slot in the ADB are sampled in the buffer and sent out through the analogue multiplexer. The gain of the front-end amplifier is about 50mV/fC. The gain of the output

buffer of the analogue multiplexer is in the range of 0.8[V/V]. Therefore the final gain of the whole read-out chain is roughly 40mV/fC. All figures in the paper showing the gain and linearity refer to the full processing chain (front-end amplifier, ADB and output multiplexer). The front-end circuit is designed in such a way that it can be used with either polarity of the input signal, however the full read-out chain (NMOS switches in the analogue pipeline, output multiplexer) is optimised for p-side strips. The dynamic range of the amplifier is designed for 12fC input, which together with the gain of 40mV/fC gives a full swing at the output of the chip in the range of 500mV. The current in the input transistor is controlled by an internal DAC and can be set within the range 0 to 320uA. This allows one to optimise the noise according to the actual detector capacitance.

III. RESULTS FROM THE EVALUATION OF A SINGLE CHIP

The basic parameters of the chip have been evaluated using internal calibration circuitry. The internal calibration circuitry provides a well-defined voltage step at the input of the calibration capacitors connected to every channel. Since the characteristic of the calibration DAC can be measured, the inaccuracy of the electronic calibration is related only to the deviation of calibration capacitors from the nominal value and the mismatch of the resistors used for scaling of the calibration voltage. For comparison with the results obtained with the electronic calibration, the absolute calibration of the chip in the set-up with a silicon pad detector and beta source is also presented.

A. Basic parameters of the Front-End amplifier.

The basic parameters of the amplifier are speed, gain, linearity and noise performance. The pulse shape at the output of the front-end amplifier has been evaluated by scanning the delay of the calibration signal with respect to the 40MHz-sampling clock for the analogue pipeline. In order to normalise the results to the absolute time scale the measurement has been repeated for two consecutive values of the trigger delay.

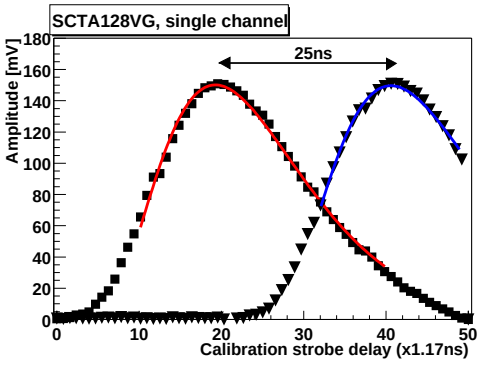

Figure 2: Pulse shapes at the output of the multiplexer obtained from the delay scan for two consecutive trigger delays.

Figure 2 shows the example of the measurement done for one typical channel of the SCTA128VG chip. The injected charge was 3.5fC. The obtained 18ns peaking time is in the expected range given by the technology process variation. The distribution of the peaking times in one SCTA128VG chip is shown in Figure 3. The RMS spread of the peaking times is in the range of 0.6%.

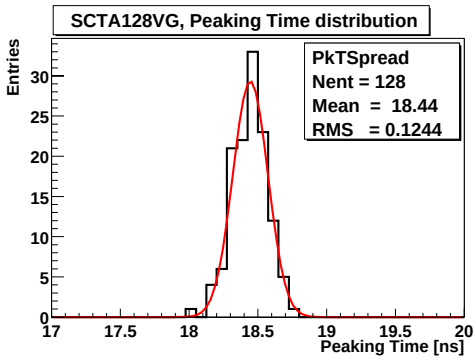

Figure 3: Distribution of the channel peaking times in one SCTA128VG chip. The RMS spread is about 0.6%.

Figure 4 shows the gain linearity for one channel in the chip. The gain is 43mV/fC and a good linearity is kept up to 16fC, which is the maximum range of the calibration DAC. The overall distribution of the gain in one SCTA128VG chip is presented in Figure 5. The RMS spread of the gains is about 2%, which is very good for tracking applications.

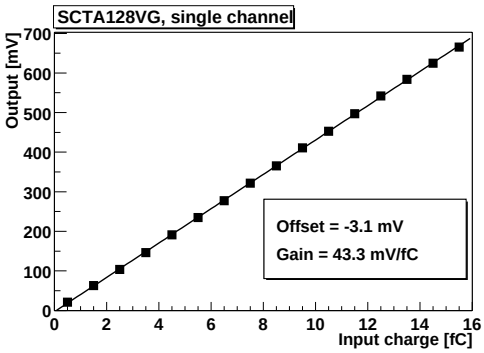

Figure 4: Gain linearity for one channel of the SCTA128VG chip.

The noise measurements have been done for the whole chip working with a 40MHz clock sampling data to analogue memory and for random readout of ADB cells. In this way any pedestal variation between ADB cells will contribute to the overall noise performance of the chip. The distributions of the ENC in one particular SCTA128VG chip for various input transistor biases are shown in Figure 6. For input transistor current ranging from 120µA up to 300µA the equivalent noise charge varies between 480 and 630e-. The RMS spreads of the ENC are in the range of 2 to 2.5%.

In order to verify the measurements with the internal calibration signal a set-up with a detector and beta source has been built. The SCTA128VG chip was connected to a SINTEF Silicon pad detector of thickness of 530µm. The detector bias voltage was set to 400V, 265V above the depletion voltage, providing sufficiently fast charge collection from the pads. The SCTA128VG chip was operating under nominal bias condition with input transistor current set to 200µA. Figure 7 shows the signal distribution from the detector exposed to beta particles. The gain extracted from

this signal distribution, assuming the Landau peak corresponding to a charge of 5.7fC, is in the order of 44.2mV/fC. This has to be compared with the gain of 45.6mV/fC measured with internal calibration circuitry for the channel connected to a detector pad. A minor difference of 3% between the results of two measurements could be explained not only by the tolerance of the calibration capacitors and inaccuracy of the band-gap reference but also by a ballistic deficit for charge collected from the detector. The difference between charge collection time from the detector and charge injected from the calibration circuitry is in the range of 5ns, which is not negligible for a front-end amplifier with 18ns peaking time.

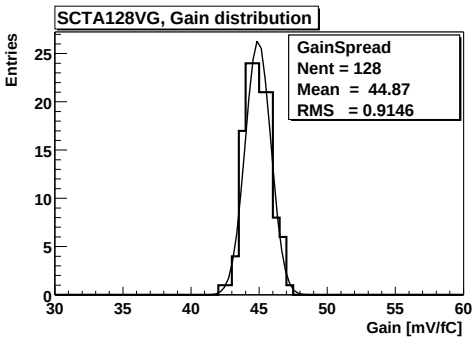

Figure 5: Distribution of channel gains in one SCTA128VG chip. The RMS spread is in the range of 2%.

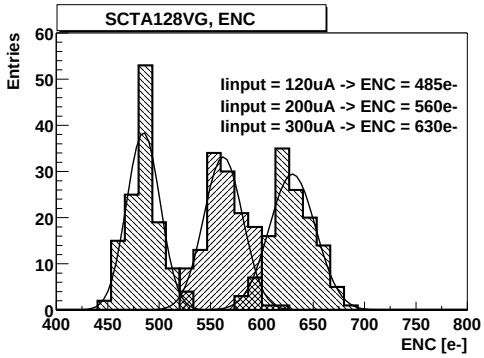

Figure 6: Distribution of ENC in a single SCTA128VG chip for different bias of the input transistor. The spread of the equivalent noise charge is in the range of 2 to 2.5%.

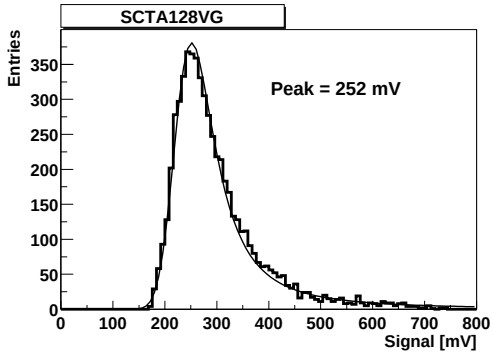

Figure 7: Histogram of data taken with silicon pad detector and a ^{106}Ru beta source showing Landau peak at 252mV.

B. *Performance of the analogue memory (ADB).*

One of the most important parameters of the analogue memory, which will define its contribution to the overall noise performance of the chip, is the uniformity of the DC offsets (pedestals) between ADB cells.

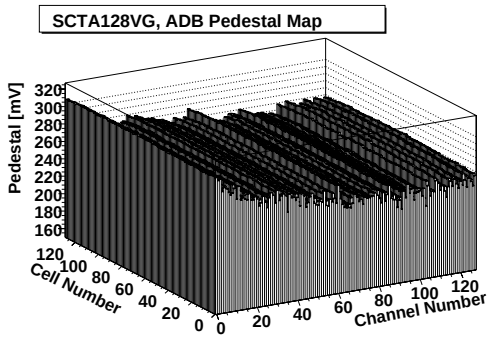

Figure 8: ADB pedestal map in one SCTA128VG chip.

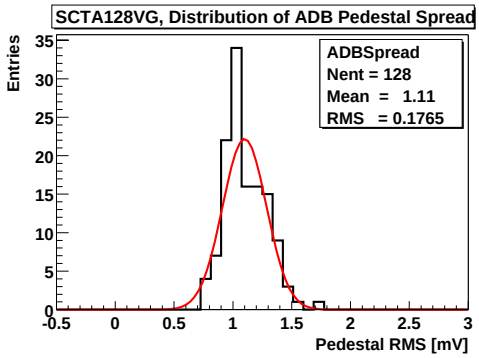

Figure 9: Distribution of ADB pedestal spread in each channel, in one SCTA128VG chip. The 1.1mV mean value of the distribution is equivalent to 150e- ENC.

Figure 8 shows the pedestal map of 128x128 ADB cells in one chip. From the presented figure one can extract the ADB cell-to-cell variation for all channels of the chip. The distribution of the ADB pedestal spreads for all channels in one particular chip is shown in Figure 9. The 1.1mV mean value of the distribution is equivalent to 150e- ENC of extra, non-correlated contribution to the noise generated by the front-end. For a low value of the input current and a low detector capacitance the additional contribution is about 4%. For higher detector capacitance this contribution becomes negligible. One can notice the high channel-to-channel uniformity of the analogue memory confirmed by a narrow (RMS ~ 10%) distribution of the pedestal spreads (Figure 9).

IV. PERFORMANCE OF THE SCTA128VG CHIP CONNECTED TO A SILICON STRIP DETECTOR.

To demonstrate the performance of the SCTA128VG chip reading out long silicon strip detectors, several modules equipped with 12.8cm ATLAS SCT type sensors have been built. A 6 chip ceramic hybrid holding two silicon detectors of size 6.3 x 6.4cm is shown in Figure 10.

The noise performance of the SCTA128VG chip may be optimised according to the detector capacitance by adjustment of the current in the input transistor. Figure 11 shows the results of noise measurements of one module with SCTA chips connected to 6.4 and 12.8cm long silicon strip detectors.

Figure 10: Photograph of 6chip, 12.8cm strip silicon detector (ATLAS type) module.

The measurement has been done for various bias conditions of the input transistor. It should be noted that the noise performance of the chip connected to 12.8cm strips could be improved by increasing the bias current of the input transistor. The reduction of ENC is relatively smaller for high current since the noise of the base spread resistance and the noise of the strip resistance become limiting factors.

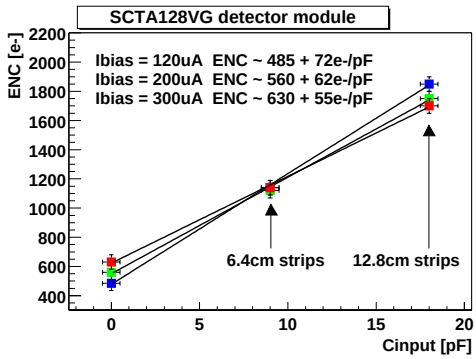

Figure 11: ENC for SCTA128VG chips connected to various length silicon strip detectors.

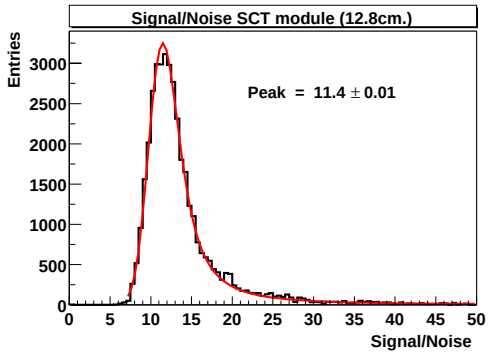

Figure 12: Signal over Noise histogram of data taken with 100GeV pion beam for the 12.8cm detector module. Measurement done for 200µA input transistor current.

Figure 12 shows a Signal-over-Noise distribution of data taken with 100GeV pion beam for the SCTA chip connected to a 12.8cm long and 280µm thick silicon strip detector. The SCTA128VG chip was operated under nominal bias conditions with input transistor current set to 200µA. The ENC of 1850e- extracted from Figure 12 has to be compared with an ENC of 1700e- measured with the internal calibration circuit. The difference may be explained by the ballistic deficit and charge loss due to the inter-strip capacitances of the detector.

V. Results of the X-Ray Irradiation

Although the SCTA128VG chip is realised in DMILL radiation hard technology the radiation effects in the devices cannot be ignored. The critical issue is the noise in the front-end amplifier. A second order effect is possible degradation of matching which may affect the uniformity of the channels in terms of gain, speed and the ADB performance.

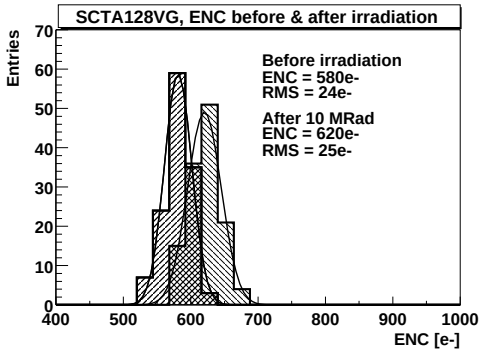

Figure 13: Distribution of ENC before and after 10Mrad. After irradiation the ENC increases by about 6%. The measurement are performed for 200µA input bias current.

The irradiations have been performed at CERN using a facility providing 10keV energy X-Rays at two dose rates: 8 and 33kRad/min. No annealing has been applied. During the irradiation we have evaluated the analogue parameters such as gain, noise, peaking time, and ADB uniformity as well as power consumption in the analogue and digital parts of the circuit.

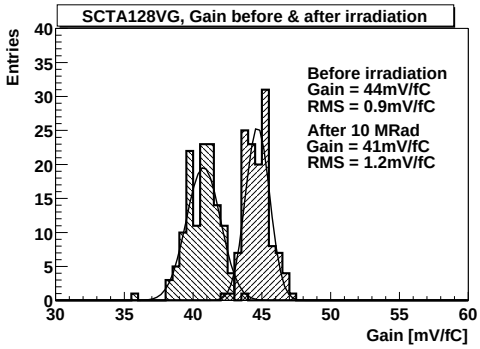

Figure 14: Distribution of channel gains before and after 10Mrad. After irradiation there is a noticeable drop of gain in the order of 7%, and an increase of gain spread from 2 to 3%.

Figure 13 shows the distribution of ENC in one SCTA chip before and after irradiation. The increase of parallel noise due to the BJT beta degradation is as expected and could be neglected in the case of a chip working on a detector module when the serial noise due to the capacitive load is dominant. Figure 14 shows the distribution of channel gains in the

SCTA128VG chip before and after irradiation. After irradiation one can observe a 7% decrease of gain and an increase of gain spread from 2 to 3%. The evolution of power consumption during the irradiation is shown in Figure 15.

The small (8%) decrease in analogue power consumption is due to the drift of the resistors in the internal band-gap reference and could be compensated by a change of the bias DAC setting. The peaking time and the uniformity of the ADB pedestals were unaffected by the X-Ray irradiation.

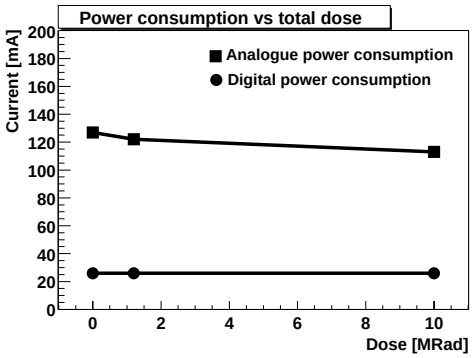

Figure 15: Evolution of analogue and digital power consumption of SCTA128VG chip during the X-Ray irradiation.

VI. WAFER SCREENING SYSTEM FOR SCTA128VG CHIP.

In order to be able to qualify good dies a wafer screening system has been developed. The system is based on an automatic probe station with all movements programmed. Using a standard probe card it was possible to test the SCTA chips under nominal bias conditions and at full, 40MHz read-out speed. Results of all tests together with chip coordinates are saved to file for off-line analysis. The presented system provides the capability of evaluating all analogue parameters like gain, noise, peaking time, ADB uniformity as well as chip power consumption. The system enables one to do defect analysis, which is a part of the design validation.

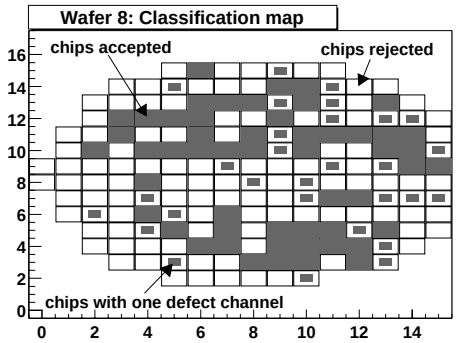

Figure 16: Example of wafer map with chips classified according to the number of defects.

Figure 16 shows an example of a typical wafer map with SCTA128VG chips classified according to the number of defects detected during analysis. The presented wafer shows roughly 30% yield for perfect chips. The percentage of the chips with single defects (channel gain out of specified 20% range or single ADB pedestal out of the normal distribution) was in the range of 15%. The SCTA chips with single defects are usually used for the evaluation of the hybrids when we do not require the 100% good channels as for the final detector modules. Figure 17 shows the distribution of the chip gains on one typical wafer. One can see good uniformity (in the range of 5% RMS) of the mean value of the gains for SCTA128VG chips over a whole wafer.

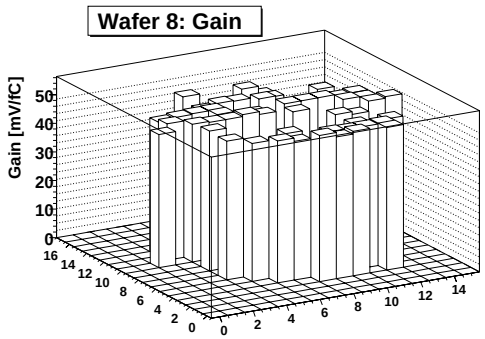

Figure 17: Distribution of the chip gains on a wafer.

VII. CONCLUSIONS

The SCTA128VG chip is an implementation of a full analogue architecture satisfying the requirements of LHC experiments. The analogue performance of the SCTA128VG chip is adequate for the readout of LHC type Si strip detector modules. Excellent uniformity of the analogue parameters on the chip level as well as on the wafer level has been shown. The results of the X-Ray irradiation show radiation hardness of the SCTA128VG chip up to the ionising doses required by LHC experiments. A system for wafer screening of the SCTA128VG chip has been presented. It allows design validation in terms of defect analysis as well as selection of good dices to the users.

VIII. REFERENCES

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