The HAL25 Front-End Chip for the ALICE Silicon Strip Detectors

D. Bonnet, A. Brogna, J.P. Coffin, G. Deptuch, C. Gojak, C. Hu-Guo*, J.R. Lutz, A. Tarchini
IReS (IN2P3-ULP), Strasbourg, France

J.D. Berst, G. Claus, C. Colledani
LEPSI (IN2P3-ULP), Strasbourg, France

*Corresponding author Christine.hu@ires.in2p3.fr

Abstract

The HAL25 is a mixed low noise, low power consumption and radiation hardened ASIC intended to read out the Silicon Strip Detectors (SSD) in the ALICE tracker. It is designed in a 0.25 micron CMOS process and is conceptually similar to a previous chip, ALICE128C. It contains 128 analogue channels, each consisting of a preamplifier, a shaper and a storage capacitor. The analogue data is sampled by an external logic signal and then is serially read out through an analogue multiplexer. This voltage signal is converted into a differential current signal by a differential linearised transconductance output buffer. A slow control complying with the JTAG protocol was implemented to set up the circuit.

Introduction

The HAL25 is a mixed, analogue digital, ASIC designed for read-out of Silicon Strip Detectors (SSD) in the ALICE tracker. It is based on the ALICE first generation chip, ALICE128C [1]. The ALICE128C chip performances were successfully maintained up to 50 krad of the ionising dose. It is now used in the SSD front-ends electronic of the STAR tracker.

In order to maintain some safety margin in radiation environment a new circuit has been designed. It has been demonstrated that commercial deep sub-micron CMOS processes exhibit intrinsic radiation tolerance [2]. HAL25 has been designed in a 0.25 micron CMOS process. In addition special design techniques have been used to meet the demands of low noise, low power consumption and radiation hardness required by the ALICE experiment.

For the SSD layer, the ALICE experiment needs a readout device having a very large dynamic range (+/- 13 MIPs) with a good linearity and an adjustable shaping time from 1.4 µs to 2.2 µs. This is a challenge for such a circuit designed in a deep sub-micron process operated at only 2.5 V which is the edge of the use of standard analogue design techniques.
This paper explains the design of the chip. Since HAL25 is still under evaluation, only preliminary results will be given.

HAL25 Block Diagram

Figure 1 shows the circuit block diagram. HAL25 contains 128 channels, each consisting of a preamplifier, a shaper and a capacitor to store the voltage signal proportional to the collected charge on a strip of a silicon detector. The data is sampled by an external logic signal and is read out at 10 MHz through an analogue multiplexer. This voltage signal is converted to a differential current signal by a differential linearised transconductance output buffer. The chip is programmable via the JTAG protocol which allows:

- to set up a programmable bias generator which tunes the parameter of the analogue chains;
- to check analogue behaviour of the chip by injecting adjustable charges to the inputs of selected channels with a programmable pulse generator ;
- to perform the boundary scan.

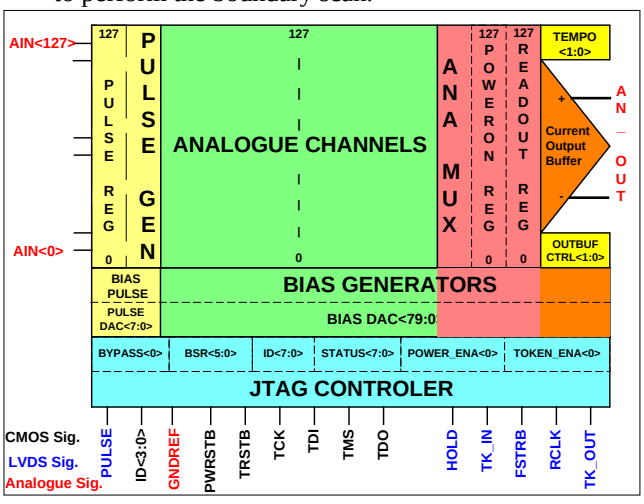

Fig. 1 HAL25 block diagram

Table 1 shows the main specifications

	Specification
Input range	± 13 MIPs
ENC	≤ 400 e^-
Readout rate	10 MHz
Power	≤ 1mW / Channel
Tuneable Shaping Time	1.4 µs to 2.2 µs
Single power supply	0 – 2.5 V

I. Preamplifier

The preamplifier is a charge amplifier made from a single-ended cascode amplifier with an NMOS input transistor dimensioned to meet the noise specification. The additional bias branch is used to increase the current in the input transistor [3]. Figure 2 shows the preamplifier schematic.

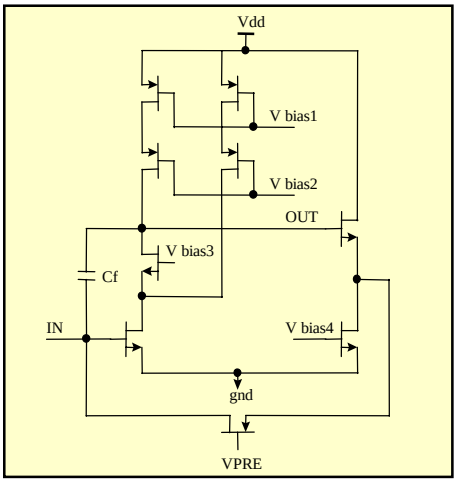

Fig. 2. Preamplifier schematic

The advantages of the circuit compared to a conventional folded cascode structure are as follows:

- A 2.5 V single power supply voltage which simplifies power supply circuit. This is a strong requirement from the ALICE experiment.
- The drain current of the input transistor which is the sum of the current flowing in both bias branches. This improves power efficiency.

Simulation shows that preamplifier has a gain of 10 mV/MIP (24000 e^-) and a power consumption of 225 µW.

II. Shaper

The ALICE experiment needs a front-end circuit having a very large dynamic range (±13 MIPs) with a good linearity and a shaping time adjustable from 1.4 to 2.2 µs. A conventional shaper using a transistor as a feedback resistor (Fig. 3a) cannot satisfy the required dynamic and the linearity range. A linearised source degenerated differential pair (Fig. 3b) is used as an active feedback resistor. The details of the shaper are shown in figure 4.

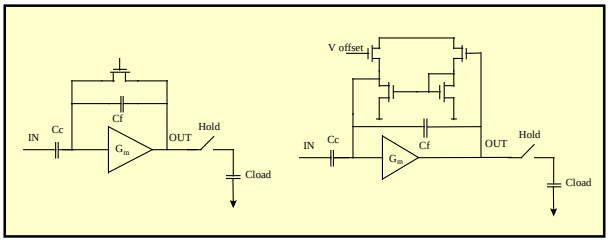

Fig. 3a. Shaper A Fig. 3b. Shaper B

The active feedback circuit is a linearized transconductance amplifier with a very low transconductance value built with the differential pair M1, M2 transistors. Transistors M3, M4 are used for source degeneration of the differential pair linearising its transconductance. Transistors M5, M6 are current sources. The M7 and M8 constitute the non-symmetrical active load of the differential pair. The transconductance value of the feedback circuit depends on the transconductance of M1, M2 and the value of conductance g_{DS} of the transistors M3, M4 connected in parallel [4]. Because the transconductance value of the transistors M1 and M2 depends on the bias current, it is easy to change the total transconductance of the circuit. This means that the equivalent resistance, on the feedback path, can be varied by changing the bias current. The output DC level of the shaper is fixed by Vdc.

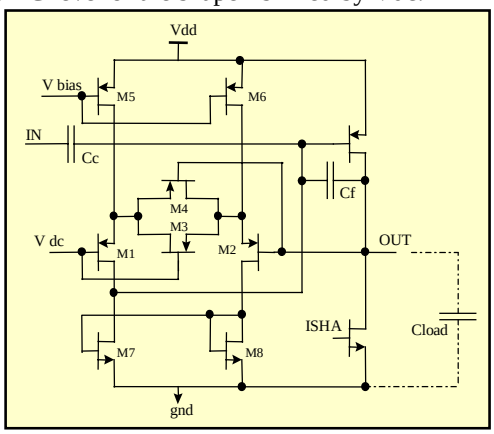

Fig.4 Shaper schematic

The noise contribution from the active feedback depends mainly on the bias current and the value of g_m of M7. In order to reduce the noise of the circuit, the following points are taken into account:

- minimum bias current ;
- minimum g_m of M7.

A PMOS inverter is chosen as an amplifier stage in the shaper because it is the simplest way to meet the specification of the very long peaking time. This approach is a trade off between the values of the capacitors and the g_m of the amplifier. The coupling and feedback capacitors are 3 pF and 0.6 pF, respectively. The storage capacitor is 10 pF.

Another advantage of this shaper is that its DC output level is adjustable via M1. It is possible to tune different voltage values for positive and negative inputs in order to increase dynamic range.

The shaper has a power consumption of 65 and 130 µW corresponding to the shaping time of 2.2 µs and 1.4 µs respectively. The total front-end gain is 35 mV/MIP in ± 13 MIPs range. A non linearity less than 3% is obtained by simulation within ± 10 MIPs range. The simulated ENC of the front-end circuit is :

ENC = 207 e^- + 10 e^- /pF for τ_s = 1.4 µs
ENC = 158 e^- + 10 e^- /pF for τ_s = 2.2 µs

Where τ_s is the peaking time.

The signal is sampled on the storage capacitor by an external LVDS HOLD signal activated at τ_s with respect to the peaking time.

III. Analogue Multiplexer

The analogue multiplexer is made of 128 intermediate buffers, two 128 bits shift registers (POWERON, READOUT) and two extra bits flip-flop cells (TEMPO) (Fig. 1). The readout is performed by injecting a token which is shifted through READOUT. TEMPO is used to delay by two clock pulses the injected token (TK_IN) in order to switch "ON" the first two intermediate buffers before beginning the readout. POWERON controls the power on and off of the intermediate buffers while READOUT controls the serial data transfer.

Only 3 of 128 buffers are powered on at the same time during the readout cycle. They are the buffer N corresponding to the channel being read and two adjacent buffers i.e. channels N-1 and N+1. At the same time the buffer N-2 is switched off and the buffer N+2 is switched on. This means only 4 buffers dissipate power during the readout.

The out going token (TK_OUT signal) is picked up two channels before the end of the readout of a chip in order to allow a daisy chaining of several HAL25 circuits without extra clock cycles. An asynchronous FAST CLEAR signal can reset the token and abort the cycle at any moment of the readout.

The multiplexer can be set by JTAG in order to test a single channel. This test is called "transparent mode". With HOLD signal inactive, the analogue response of an injected signal can be observed at the output of the chip.

IV. Differential Current Buffer

Figure 5 shows the three main parts of the analogue output buffer:

- Single ended to differential voltage converter;
- Linearised transconductor;
- Output voltage reference controller.

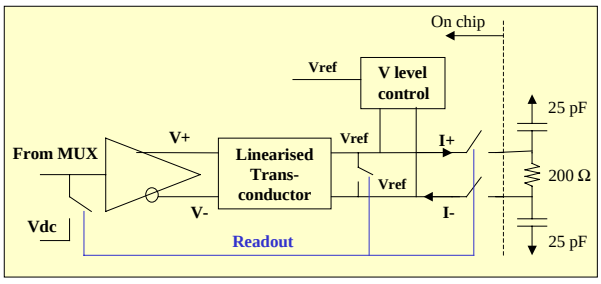

Fig. 5. Output buffer block diagram

The current gain and the output DC level are adjustable by the programmable bias generator. Analogue output of several chips can be connected in parallel. Only the chip selected to be read out drives the output lines. The outputs of the remaining chips are in a high impedance state. Non selected chips have their output buffers powered off in order to reduce the total power consumption. The voltage reference controller sets the quiescent output level. This allows to use a simple floating input differential buffer outside the chip to pick up the signal.

a. Single ended to differential voltage converter

The single ended to differential voltage converter has a unity gain. It is built with three operational amplifiers and a resistive ladder. The common mode output signal of this stage is clamped to the internal reference DC level, Vdc, common to the shaper and the multiplexer.

b. Linearised transconductor

The linear transconductor is based on the differential pair linearised by the cross-coupled quad cell [5].

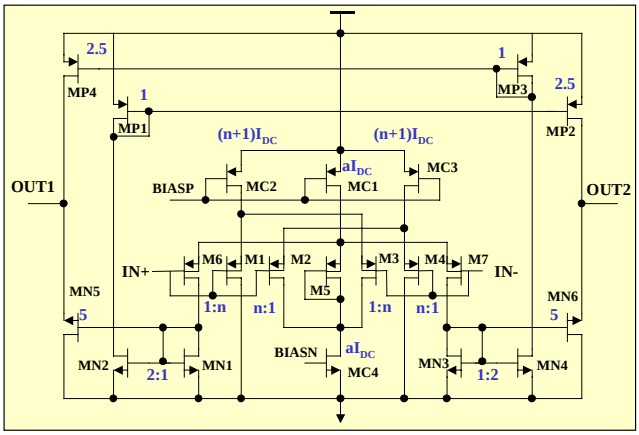

Fig. 6 Linearised transconductance

The schematic of the transconductance element is shown in Fig. 6. Transistors M1-M4 form the cross-coupled quad cell, while M6 and M7 constitute the differential pair. The bias current of the differential pair is delivered by the cross-coupled quad cell through the M5 transistor and the current source MC1. The bias current of the differential pair has a quadratic dependence on the differential input voltage. The output current presents a linear dependence of the input signal by a careful choice of the weighting factor *n*. The additional current gain is achieved on the cascade of current mirrors MN1-MN2 with MP1-MP2 and MN3-MN4 and MP3-MP4. The output has a gain of 175 μA/MIP at nominal bias.

c. Output voltage reference controller

The classical control of the quiescent output levels by a common mode feedback circuitry with low pass signal filtering was not possible because it has to be off when the chip is not selected. Another solution, using a dummy transconductance stage and a feed forward circuitry for referencing the output of the buffer, was preferred (Fig. 7). Both inputs of the dummy transconductor are fed with the common mode signal and resulting not balanced output signal is assumed to be the same for the main circuitry. The output of the dummy element is balanced by comparing its voltage level to the reference signal in

the error amplifier. As a result, a balanced voltage equal to the reference value Vref is established at the output of the dummy transconductor. The both outputs of main transconductor are forced to the same value through current mirrors. This design is potentially sensitive to mismatches, thus special care was taken at the layout level. An eventual mismatch in the output voltage quiescent level can be adjusted by changing Vref.

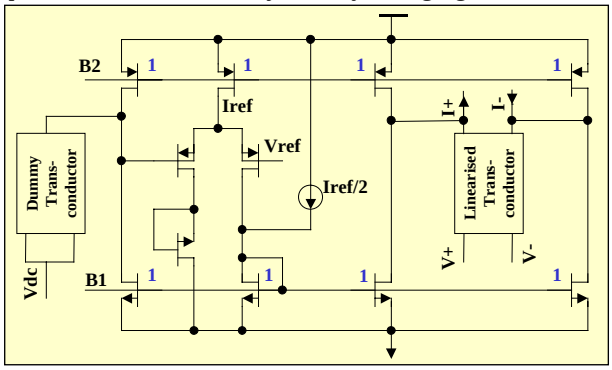

Fig. 7. Quiescent output level controller

V. Bias Generators and Current Reference

The bias generators provide DC currents and voltages to bias accurately all the analogue parts. They consist of nine 8 bit DACs. Each DAC is made of a JTAG register, current sources and when necessary a current to voltage converters. The JTAG register consists of a shift register and a shadow register designed with a majority voting logic approach in order to prevent Single Event Upset (SEU).

In the HAL25 chip, an internal current source provides current reference to the bias generators. It is designed to be insensitive to a +/- 8% power supply variation. To prevent poly-silicon resistor value variation (+/- 20%) due to the process, the reference is adjustable by JTAG in 5 steps from -15% to +15% around nominal value.

VI. Test Pulse Generator

This feature can test analogue channels by injecting adjustable charge pulses. The dynamic range for test pulse is more than +/-15 MIPs, enough to test the full dynamic range of analogue channels. A programmable number of channels can be tested together.

VII. JTAG Controller

The control interface of HAL25 complies with the JTAG IEEE 1149.1 standard. It allows the access to the registers in the chip, especially for setting the bias and switching between the running and the test modes. These modes are the pulse test, the transparent test and the boundary scan of the pads involved in the readout.

After reset of the controller, the circuit is in the bypass state. For JTAG this means that serial data can skip the circuit with one extra JTAG clock cycle per bypassed circuit. For the readout part the token passes directly from the previous to the next HAL25. An ID number can be read from the chip by setting 4 input pads.

HAL25 Power Consumption

Three types of power consumption can be calculated:

- Power consumption per channel during acquisition:
  P (no read out) = 355 µW (τ_s =1.4 µs)
  P (no read out) = 290 µW (τ_s = 2.2 µs)
- Power consumption per channel during readout:
  P (read out) = 750 µW (τ_s =1.4 µs)
  P (read out) = 680 µW (τ_s = 2.2 µs)
- Mean power consumption per channel for a read out cycle of 1 ms:
  <P> = 360 µW (τ_s =1.4 µs)
  <P> = 265 µW (τ_s = 2.2 µs)

HAL25 Layout

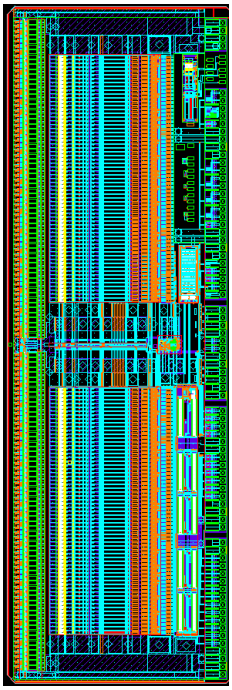

Fig. 8. HAL25

The HAL25 has an area of 3.65 x 11.90 mm^2 (Fig. 8). The process has 1 poly and 3 metal layers. The enclosed gate geometry with guard ring technique was used in the layout to prevent post-irradiation leakage currents in NMOS channel transistors.

The I/O pad sizes and placement pitches were designed to be directly compatible with the existing Tape Automated Bonding (TAB) technique. All the pads except the power supply pads are protected with diodes. Pads used by the JTAG protocol are CMOS while the readout control pads comply with the LVDS standard.

Circuit Evaluation

Evaluation of HAL25 is underway. Several chips have been tested on a probe station. Correct functionality of the chip has been verified.

Figure 9 shows output stream from channel 1 to channel 128. A 1 MIP signal injected on one channel shows up clearly after the average channel pedestals have been subtracted.

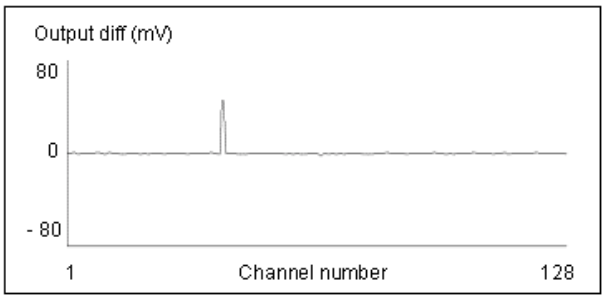

Fig. 9 Output stream

Figure 10 shows analogue pulse shapes at output buffer as a function of the injected charges.

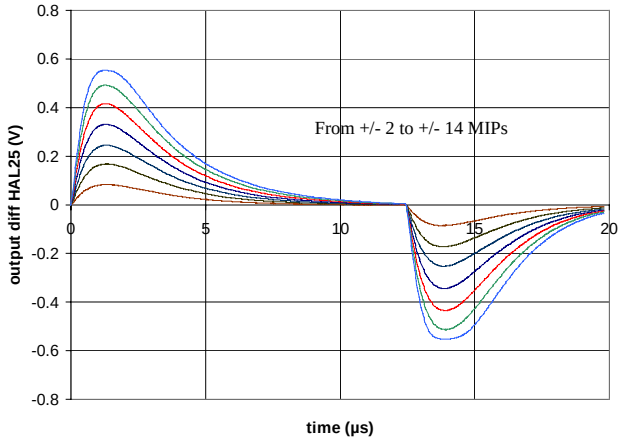

Fig. 10 Output shapes

A good linearity (<4%) has been obtained (Fig. 11) within ±10 MIPs range. This has good agreement with the simulation results.

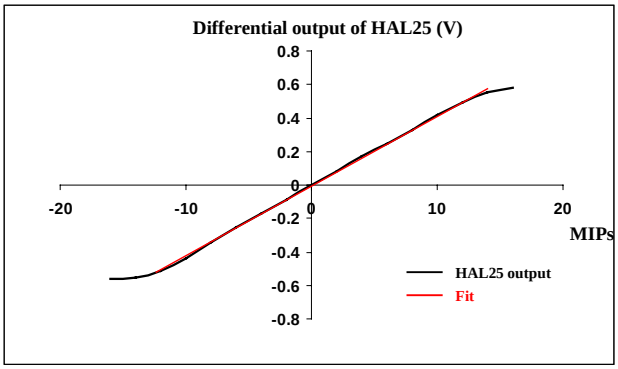

Fig. 11 Output of HAL25 as a function of the input MIPs

Conclusion

A new mixed ASIC intended for read out of SSD in the ALICE tracker has been designed in a deep submicron process. The correct functionality of the chip has been verified.

Further investigations planned with HAL25 will include more detailed performance studies especially the yield optimisation and the irradiation tests.

Acknowledgment

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