

ENHANCED RADIATION HARDNESS AND FASTER FRONT ENDS FOR THE BEETLE READOUT CHIP

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Abstract

This paper summarizes the recent progress in the development of the 128 channel pipelined readout chip *Beetle*, which is intended for the silicon vertex detector, the inner tracker, the pile-up veto trigger and the RICH detectors¹ of LHCb.

Deficiencies found in the front end of the *Beetle* Version 1.0 and 1.1 chips resulted in the submissions of *BeetleFE 1.1* and *BeetleFE 1.2*, while *BeetleSR 1.0* implements test circuits to provide future *Beetle* chips with logic circuits hardened against single event upset (SEU).

Section I. motivates the development of new front ends for the *Beetle* chip, and section II. summarizes their concepts and construction. Section III. reports preliminary results from the *BeetleFE 1.1* and *BeetleFE 1.2* chips, while section IV. describes the *BeetleSR 1.0* chip. An outlook on future test and development of the *Beetle* chip is given in section V.

I. INTRODUCTION

The development of the *Beetle* readout chip started in late 1998. It implements the basic RD20 architecture [4], augmented with a prompt binary readout path like it was implemented on the HELIX128 chip [5] and a pipelined binary operation mode. Besides several (2×2) mm² chips with test structures and components, two complete readout chips (*Beetle1.0* and *Beetle1.1*) have been manufactured in commercial 0.25 μ m CMOS

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¹in case of multianode photomultiplier tube readout

technology. A detailed description of these chips, their architecture and performance can be found in [1] [2] [3].

Beetle1.0, the first complete pipelined readout chip had to be patched with a focused ion beam to become functional. In turn the second one, *Beetle1.1* included all fixes to correct the errors found on its predecessor. However, a few problems still remained:

- Peaking time of the front end $t_{\text{peak}}(0 \dots 100\%) \geq 27$ ns,
- Decay time of the pulse has a remainder above 30% after 25 ns, too long for the operation of the LHCb vertex detector,
- Maximum input current of ≈ 2 nA, too small for the expected occupancies at LHCb
- Digital circuits not robust against SEU.

To overcome these problems, which are primarily related to the actual requirements of LHCb, test chips implementing the necessary circuits were submitted. This allows the test of the circuit's functionality prior to its implementation on a complete readout chip. Furthermore different approaches to solve the same problem can be evaluated to find the optimum solution.

II. NEW FRONT ENDS

The front end implemented on *Beetle1.1* was developed with an early version of the 0.25 μ m CMOS design kit in 1998 and submitted on the first test chip *BeetleFE 1.0*. It consists of a charge sensitive preamplifier, a $CR - RC$ pulse shaper and a buffer. The first two stages use *folded cascode* amplifier cores, while the buffer is a source follower. Measurements of its characteristics showed that it was considerably slower than

Table 1: Design parameters of the front ends of the *BeetleFE 1.1* (Set 2) and *BeetleFE 1.2* (Set 5 and Set 6) test chips.

Set	input transistor	W	L	feedback	shaper feedback
2a...c	NMOS rectangular	3744 μm	0.42 μm	PMOS	48.8fF
2d...e	NMOS rectangular	3744 μm	0.42 μm	PMOS	20.5fF
5a	PMOS waffle	8310 μm	0.28 μm	PMOS	15 fF
5b	PMOS waffle	8310 μm	0.28 μm	PMOS	18.75 fF
5c	PMOS waffle	8310 μm	0.28 μm	PMOS	37.5 fF
5d	PMOS waffle	7123 μm	0.28 μm	PMOS	18.75 fF
5e	PMOS waffle	7123 μm	0.28 μm	PMOS	37.5 fF
5f	PMOS rectangular	5852 μm	0.28 μm	PMOS	18.75 fF
5g	PMOS rectangular	5852 μm	0.28 μm	PMOS	37.5 fF
5h	PMOS waffle	5936 μm	0.28 μm	PMOS	18.75 fF
5i	PMOS waffle	5936 μm	0.28 μm	PMOS	37.5 fF
6a	NMOS rectangular	3744 μm	0.42 μm	NMOS	48.8 fF



Figure 3: Layout of the *BeetleFE 1.1*: The new front end channels are indicated

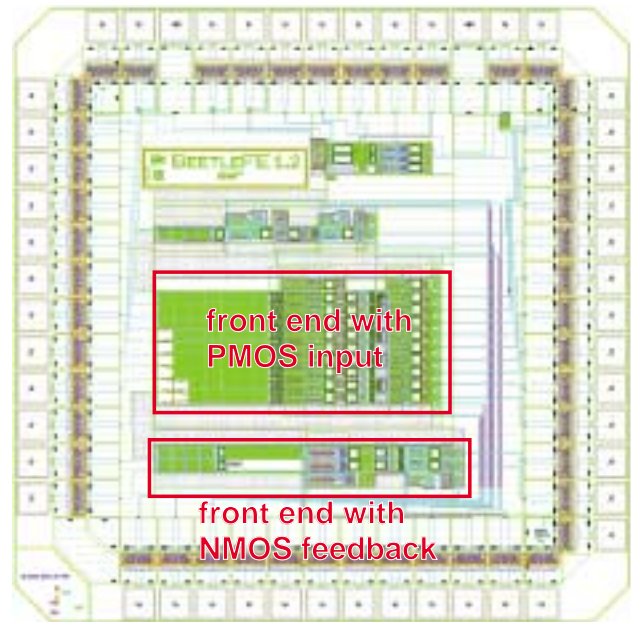


Figure 4: Layout of the *BeetleFE 1.2*: The new front end channels are indicated

III. FIRST RESULTS FROM NEW FRONT ENDS

Measurements on the *BeetleFE 1.1* and *BeetleFE 1.2* (figs. 7 and 8) showed that one of the design goals, a rise time well below 25 ns has been reached with both chips. For the *BeetleFE 1.2* it was also found, that the front end could achieve a rise time of ≤ 24 ns with an input capacitance as high as 40 pF. Measurements of the maximum input current, as well as noise measurements are still in progress.

IV. THE *BeetleSR 1.0* CHIP

The *BeetleSR 1.0* chip implements two blocks of 34 registers, each 8 bits wide. Combinatorial logic calculates the parity of these registers, which is available on two groups of 9 pads. Read and write access to these register blocks is accomplished via two independent I²C interfaces: One is implemented in conventional circuitry, while the other one uses triple redundant flip-flops with majority encoding. The block schematic of the chip is shown in fig. 9, while a triple redundant flip-flop with majority encoder is illustrated in fig. 11.

This chip will permit to measure SEU rates by means of the register blocks, it also allows the calcu-

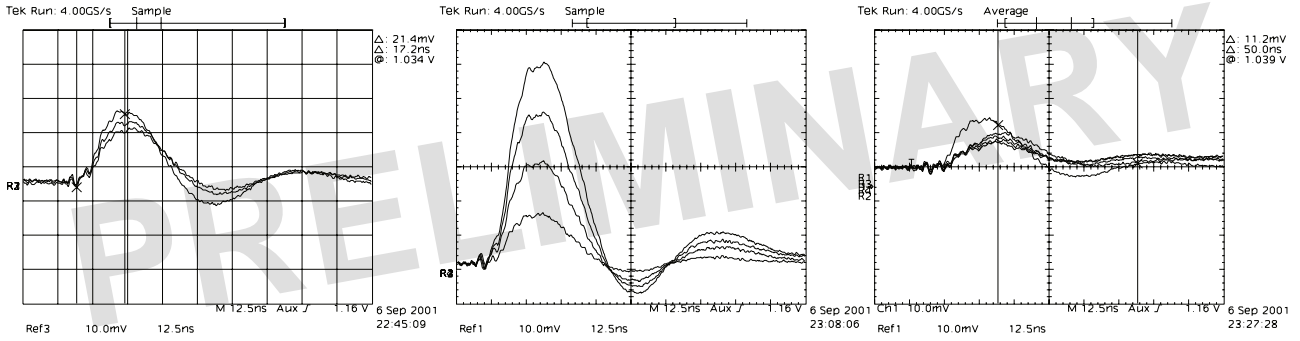


Figure 8: Pulse shapes of the *BeetleFE 1.2* test chip. The left graph shows pulse shapes from different modifications of the "Set 5" (c.f. tab. 1) front end, The middle one shows the response for different input charges, and the right graph depicts the response for input capacitances of 3 pF, 10 pF, 20 pF, 30 pF and 40 pF.

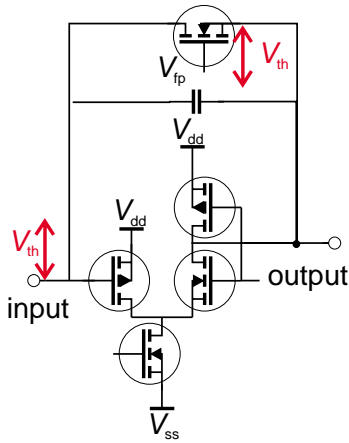


Figure 5: Schematic of the PMOS front ends implemented on *BeetleFE 1.2*: The threshold voltages V_{th} of the PMOS input transistor and PMOS feedback transistor are indicated by arrows.

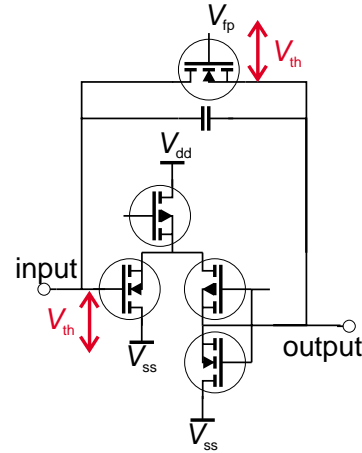


Figure 6: Schematic of the NMOS front ends implemented on *BeetleFE 1.2*: The threshold voltages V_{th} of the NMOS input transistor and NMOS feedback transistor are indicated by arrows.

lation of the SEU suppression arising from the usage of triple redundant flip-flops in state machines.

V. FUTURE PLANS

Beetle1.1 chips will be irradiated up to 10 Mrad (100 kGy) with the X-ray irradiation facility of the CERN micro electronics group. They will also be used in a test beam with prototype detectors of the LHCb inner tracker in October 2001. Studies with the chip bonded to a detector are under way.

The submission of the final version (1.2) of the *Beetle* chip is planned for spring 2002. This chip will implement:

- a modified frontend with a faster shaping and a higher maximum input charge rate, chosen from the front ends on the *BeetleFE 1.1* and *BeetleFE 1.2* chips.

- two single event upset (SEU) detection and correction mechanisms:
 - (i) triple redundant flip-flops with majority encoding in state machines and other frequently changed registers, and
 - (ii) ECC³ based on hamming encoding for more static registers.

Status reports and further test results will be available at [6].

³Error correction circuit

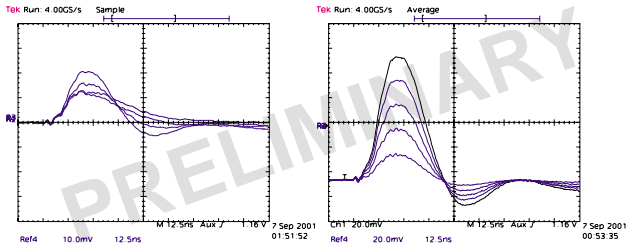


Figure 7: Pulse shapes of the *BeetleFE 1.1* test chip. The left graph shows pulse shapes from different modifications of the "Set 2" (c.f. tab. 1) front end, the right one shows the response for different input charges.

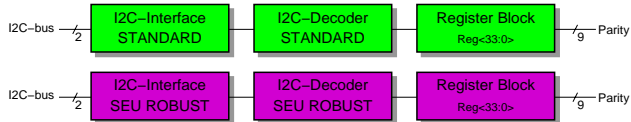


Figure 9: Block schematic of the *BeetleSR 1.0* test chip. Two register blocks with parity encoding are controlled via a standard or a SEU robust I²C interface respectively.

References

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- [5] U. Trunk, Development and Characterisation of the Radiation Tolerant HELIX128-2 Readout Chip for the HERA-B Microstrip Detectors, PhD thesis, Heidelberg (2000)
- [6] <http://wwwasic.kip.uni-heidelberg.de/lhcb/>



Figure 10: Layout of the *BeetleSR 1.0* test chip. The two register blocks are located on the right and left hand side of the chip. The I²C interfaces are the blocks in the centre, the SEU robust one being the larger block.

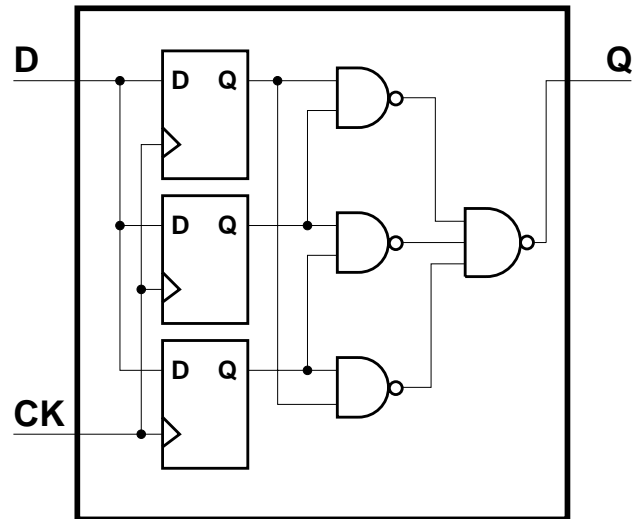


Figure 11: Triple redundant flip-flop with majority encoder used in the SEU robust I²C interface of the *BeetleSR 1.0* test chip.