Performance of the Beetle Readout Chip for LHCb

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Abstract

Beetle is a 128-channel readout chip, which will be used in the silicon vertex detector, the pile-up veto counters and the silicon tracker of the LHCb experiment at CERN. A further application of the Beetle chip is the readout of the LHCb RICH, in case it is equipped with multi-anode PMTs.

The scope of this paper is the design changes leading to the latest version 1.3 of the Beetle readout chip. In addition, measurements on earlier versions and simulation results driving these changes are shown.

I. Introduction

The development of the Beetle chip started in 1998, and up to now resulted in five 128-channel readout chips. The history of the Beetle chip is summarised in Table 1.

II. Chip Architecture

The Beetle [1] is an analogue pipelined readout chip and implements the RD20 front-end architecture [2]. For a fast trigger decision it provides a comparator with prompt binary output signals. Using the comparator output signals instead of analogue front-end signals, the Beetle can alternatively operate in a binary pipelined mode. The chip integrates 128 channels. Each channel consists of a low-noise charge sensitive preamplifier, an active CR-RC pulse shaper and a buffer. The rise time of the shaped pulse is ≤ 24 ns, the spill-over at 25 ns after the peak is less than 30 % of the maximum. The chip provides two different readout paths. For the binary readout the front-end's output couples to a comparator which features invertable outputs to detect input signals of either polarity and individually adjustable threshold levels. Four adjacent comparator outputs are logically ORed, latched, multiplexed by 2 and routed off the chip via low voltage differential signaling (LVDS) ports at 80 MHz. The pipelined readout path can operate in either a binary mode by using the comparator outputs or an analogue mode by sampling the front-end buffer's output with the LHC bunch-crossing frequency of 40 MHz. The sampled amplitudes are stored in an analogue memory (pipeline) with a programmable latency of at maximum 160 sampling intervals. This is combined with an integrated trigger buffer of 16 stages. Upon a trigger the corresponding signals stored in the pipeline are transferred to the multiplexer via a reset-table charge sensitive amplifier. The number of output ports is configurable and allows a readout time of at minimum 900 ns per triggered event. The output of a sense channel is subtracted from the analogue data to compensate common mode effects. On-chip digital-to-analogue converters (DACs) with a resolution of 8 bits generate the bias currents and control voltages. For test and calibration purposes, an adjustable charge injector is implemented on each channel. For applications which require a minimum number of transmission lines and put less strict demands on the readout speed, several Beetle chips can be read out in a daisy chain. All bias settings and configuration parameters, e.g. trigger latency, readout mode and readout speed, can be programmed and read back via a standard I^2C-interface [3]. All digital I/Os, except for the I^2C-lines and the daisy chain ports, use LVDS signals.

The Beetle is designed in a commercial 0.25 µm CMOS technology and has a die size of $6.1 \times 5.4\,mm^2$. The pitch of the analogue input pads is 40.24 µm. If no prompt readout is required, the chips can be mounted

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Table 1: History of the Beetle chip. The table lists all versions of the chip and summarises important informations together with submission dates and chip sizes.

Version	Size [mm^2]	Submitted	Comments
1.0	6.1×5.5	04/2000	First 128-channel pipelined readout chip Had to be patched with an FIB (Focused Ion Beam) to become operational
1.1	6.1×5.5	03/2001	Mask change of 1.0 to become operational Analogue front-end too slow Readout time 925 ns "Sticky Charge" in subsequent readout (c.f. sect. III.*D.*)
1.2	6.1×5.1	04/2002	Faster front-end Readout time 900 ns New feature: triple redundant logic circuits (SEU protection)
1.2 MA0	6.1×5.1	12/2002	Prototype for RICH readout Front-ends partly modified to accept multi-anode PMT signals Modified power routing
1.3	6.1×5.4	06/2003	Correction of cross talk problems Removal of "Sticky Charge" effect Improved comparator (lower spread, better offset compensation) Improved Output driver

side-by-side, since no connections to the top and bottom side of the chip are required. This allows an overall pitch of 50 µm matching most silicon sensors. In case of the silicon vertex detector, the readout chip will be positioned only 5 cm from the LHC beam, which means that the Beetle has to be radiation hard. The chip is designed to withstand a total dose in excess of 10 Mrad (100 kGy) by taking the following design measures [4]: forced bias currents are used in all analogue stages instead of fixed node voltages; enclosed gate structures for NMOS transistors suppress increasing leakage currents under irradiation; a consistent use of guard rings minimises the risk of Single Event Latch-up (SEL) [5].

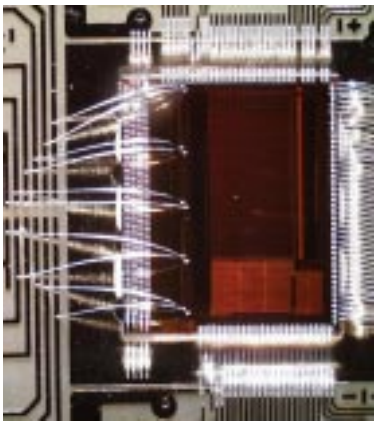

Figure 1: Patched Beetle 1.2 with bond wires attached to the front-end power supply to measure the voltage drop across the channels.

III. The Beetle 1.3 chip

The Beetle 1.3 chip only includes design changes intended to fix all known (and understood) problems with its predecessors. These changes are detailed together with the measurements and simulations which drove them.

A. Front-End

The schematic of the front-end implemented on Beetle 1.2 was not changed, since it fulfills all requirements and exhibited the performance expected from simulation and earlier test chips. However, some changes were applied to its layout and peripheral circuits:

- Test pulse circuit: The original 4-level (staircase) pattern was abandoned in favour of a 2-level pattern (i.e. same charge with alternating polarity). The maskability of the test pulse together with the single charge simplifies chip testing and gain checks on individual channels, since no corrections for the test pulse amplitude have to be applied.
- Power Routing: The readout baseline of the Beetle shows a sagging shape, which was still present on Beetle 1.2MA0, but to a lesser extent. This improvement resulted from changes of the power supply lines in the pipeline readout amplifier. Triggered by this observation, the power routing of the front-end was also investigated. One Beetle 1.2 was patched such, that wires could be bonded to the front-end power supply as shown in fig. 1. Interestingly the voltage drop measured across the 128 channels closely resembled the sagging shape of the readout baseline. In turn a simulation of all 128 front-end channels, connected by resistive power nets was done. Adding resistors representing the connections to the power pads led to the results shown in fig. 2. This simulation also confirmed, that the power distribution of the shaper's folded cascode was the sole source of the baseline sag: The DC-offset of the preampli-

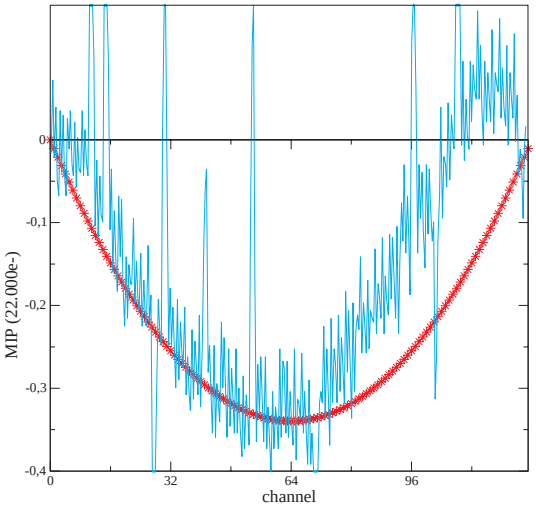

Figure 2: Readout figure of Beetle 1.2 superimposed with a simulation of the front-end channel's DC-offset, including resistive power nets.

fier is removed by the AC-coupling to the shaper, while the buffer stage is a source follower, which is greatly independent from the power supply voltage. To solve this problem, the power bars connecting the 128 channels were widened and additional pads for both power nets were placed on bottom and top of the chip. Along with these measures, blocking capacitors were placed between the power nets for reasons described later.

- Bias networks: The investigations on the front-end's power supply also revealed a minor design flaw in the biasing of the front-end. The DAC generating the bias current was located at the bottom side of the chip. The diode-connected transistor of the current mirror, which operates as a current sink, was located on the top side, leading to a considerable voltage drop across the interconnection. In turn the gate voltages of the current sources in the different channels varied, causing a gain drop towards the higher channel. A similar effect was observed in test beam data taken with a NIKHEF hybrid. On Beetle 1.3 the diode connected transistor of the current mirror was moved to the bottom side of the chip to eliminate this effect.

B. *Discriminator Circuit*

Measurements of the discriminator done at NIKHEF resulted in a measured threshold spread equivalent to $\sigma = 2.4$ DAC units (or $4800e-$), as shown in fig. 3. This meant that the bipolar spread is of the same magnitude as the range of the unipolar 3 bit local DACs intended for its compensation. The measured spread was

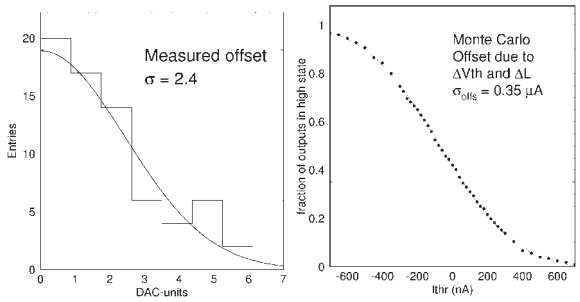

Figure 3: Measured (left) and simulated (right) threshold spread of the Beetle 1.2 comparator circuits. 1LSB ≡ 200 µA.

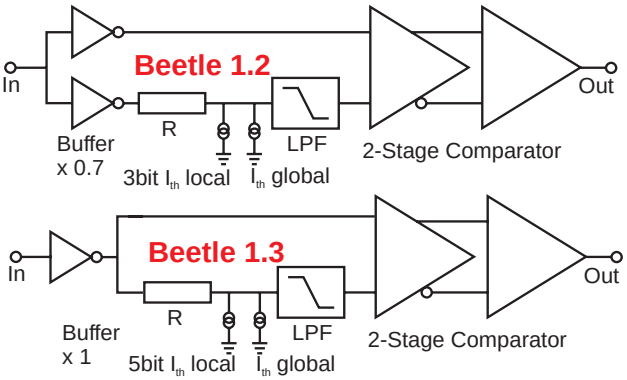

Figure 4: Schematics of the comparators on Beetle 1.2 (top) and Beetle 1.3 (bottom).

also found in good agreement with the spread expected from process parameter variations, which resulted in $\sigma = 2.8$ DAC counts (or $5600e^-$). A major culprit for this spread was found to be the split input buffer of the comparator, which was in turn replaced by a single one with an increased gain (1 instead of 0.7) on Beetle 1.3. To provide a sufficient safety margin, the channel's local DACs intended for offset compensation were improved with a bipolar range of $14400e-$ and 5 bit resolution. Fig. 4 shows the block schematics of the comparators on Beetle 1.2 and 1.3.

C. *Control Core*

The Beetle's control circuit was re-synthesised for Beetle 1.2, especially to include SEU protection/correction circuits. This was done by using triple redundant Flip-Flops with majority voting outputs for all registers, enhanced by self-triggered reprogramming circuits for the static ones. The schematics of these registers are shown in fig. 5. Regarding the digital functionality, the control circuit of Beetle 1.2 worked as expected. But its operation affected almost all other circuits by coupling switching spikes to the chip's outputs and power lines. These spikes appeared on both clock edges (and thus were named "80 MHz

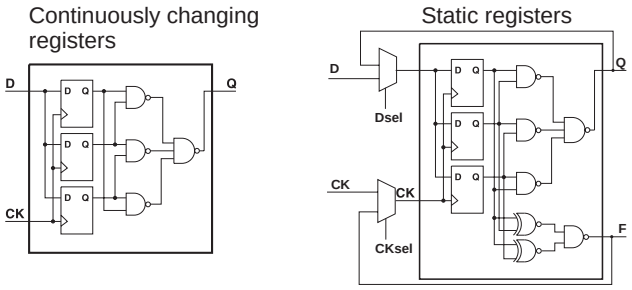

Figure 5: Schematics of a triple redundant register with (right) and without (left) self-triggered reprogramming circuit.

X-talk"), which pointed to the clock tree. The latter had grown from 21 buffers on 1.1 to 275 on 1.2 and was consequently considered as the primary source of the effect. A further increase of the crosstalk was probably due to a guard ring, which was moved from the analogue supply on 1.1 to the digital one on 1.2.

Another feature of the 1.2 core was the absence of a multiplexer at the return-token inputs used for daisy-chained readout. It required that these pads were pulled to ground, if unused. For the core of Beetle 1.3 special care was taken for the clock tree, which was reduced to 104 buffers. In addition the offending guard ring was moved back to the analogue supply and the missing multiplexers were added. Targeted on a further reduction of crosstalk, the digital power supply of the multiplexer was separated from the core supply and both were blocked with gate capacitors on chip.

D. Pipeline Readout Amplifier

The decrease of a readout cycle to the LHCb-required 900 ns on Beetle 1.2 caused the activation of two switches at the same time. Besides some charge injection, this also lead to the back-transfer of the charge present on the multiplexer's hold capacitor to the pipeamp. As a result, a remainder of up to 60% with opposite polarity and a strong distortion of the readout baseline in the next data frame was visible. This so-called sticky charge effect is depicted in fig. 6. A simulation, in which the relative timing of the two switching signals was swept is shown in fig. 7. It revealed that the simultaneous timing on Beetle 1.2 was almost the worst case and delaying either signal would result in a considerable improvement. On Beetle 1.3 the `MuxTrack` signal is delayed by 5 ns, which removes the sticky charge. This was also proven in advance by a patch applied to a Beetle 1.2: An external *mux track* signal was coupled to the corresponding line, overriding the internal signal. The result is shown in fig. 6.

A further modification of the Beetle 1.3 Pipeamp is widened power lines, as already present on Beetle 1.2MA0.

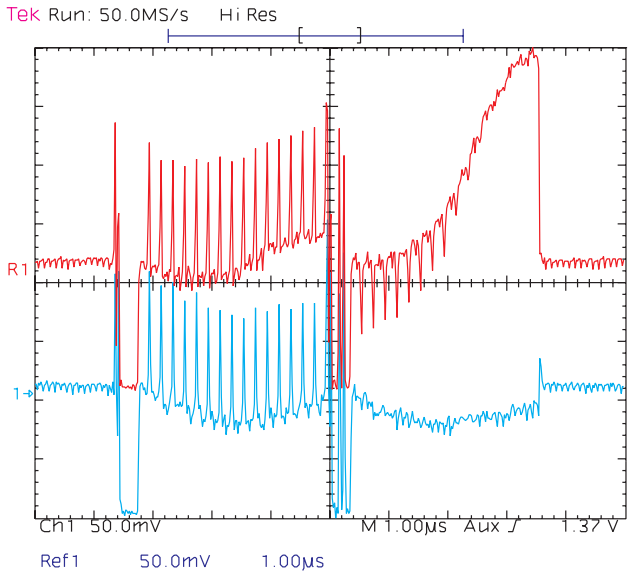

Figure 6: Trace R1: The readout figure of the 2nd data frame shows up to -60% remainder of the first one and a strong distortion of the baseline, the so-called "Sticky Charge" effect. Trace 1: Patched Beetle 1.2 with delayed `MuxTrack` signal. It does not show the "Sticky Charge" effect.

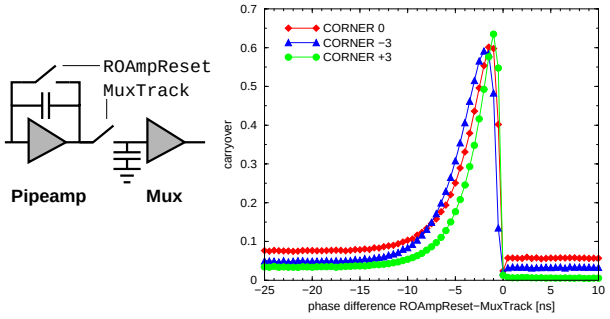

Figure 7: Sticky Charge Effect: The picture shows the "sticky charge" in fractions of the preceeding signal as a function of the relative timing of the two switches `ROAmpReset` and `MuxTrack`. On Beetle 1.2 the timing is in the steeply falling pattern of the curve. In that case different delays across the channels also explain the baseline distortion.

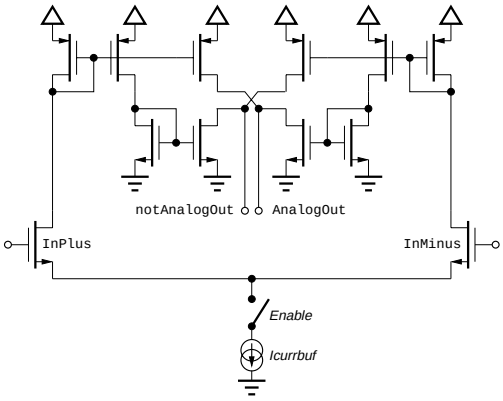

Figure 8: Schematic of the fully differential current driver on Beetle 1.3.

E. Multiplexer

Three changes were applied to the multiplexer of Beetle 1.3: The number of reference channels used for DC level subtraction was increased to 4 – one for each block of 32 channels. This modification is intended to remove spikes at the start and end of a data frame, originating from block to block crosstalk via the reference channel. Also the balance of the switch operation was improved, again targeting on the suppression of spikes. The biggest modification was in the digital part: It received its own power supply and the triple redundant Flip-Flops were removed. This was motivated by the lower switching noise, which was considered more important than SEU robustness in this part. It should be noted, that an SEU can at maximum corrupt 2 data frames by injecting an additional token, since the multiplexer token is discarded after leaving the last channel.

F. Output Driver

The output driver underwent a major redesign, primarily driven by an excessive current density in some part of the circuit. In case of an increased power supply voltage, the latter also caused a failure of the circuit. On Beetle 1.3 the output driver is now a fully differential *current* driver, which also has a higher gain when driving a 150Ω load. The schematic is shown in fig. 8.

G. Other Changes

With very few exceptions, almost all other changes on Beetle 1.3 only affected the layout of the chip. The minor changes are summarised in the following list:

- Merged openings of power pads to apply more bond wires
- Test pad for direct access to the output of the current DAC
- Separated supply for comparator LVDS outputs
- 2 additional supply pads for core power
- 5 V-compatible I^2C pads provided by CERN to get rid of external non radiation-hard level shifter FETs.

IV. Summary and Conclusions

The previous revision, Beetle 1.2, already fulfilled all LHCb requirements regarding signals and timing. It also complied with the VELO[1] requirements regarding the analogue characteristics of the front-end. Its major shortcomings are excessive crosstalk, originating from digital circuits and the "sticky charge" problem. Both were fixed on Beetle 1.3. Detailed invstigations and patches on the Beetle 1.2 and Beetle 1.2MA0 led to a redesign of the power routing on Beetle 1.3. Further improvements on this chip are a comparator with less offset and better compensation and a fully differential current output driver. Various measures were taken against the crosstalk from the digital part of the chip, since a single source of this disturbance could not be isolated. Beetle 1.3 was submitted for manufacturing end of June 2003 and came back from the manufacturer at the end of September 2003. Much like its direct predecessor, it is designed to fulfill all LHCb specifications and to seamlessly fit in the LHCb readout chain. A production run to equip the vertex detector, silicon tracker and pile-up veto counters of the LHCb experiment is planned for 2004.

V. References

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