Radiation tolerance studies of BTeV pixel readout chip prototypes.

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Abstract

We report on several irradiation studies performed on BTeV preFPIX2 pixel readout chip prototypes exposed to a 200 MeV proton beam at the Indiana University Cyclotron Facility. The preFPIX2 pixel readout chip has been implemented in standard 0.25 micron CMOS technology following radiation tolerant design rules. The tests confirmed the radiation tolerance of the chip design to proton total dose of 26 MRad. In addition, non destructive radiation-induced single event upsets have been observed in on-chip static registers and the single bit upset cross section has been measured.

I. INTRODUCTION

The BTeV experiment plans to run at the Tevatron collider in 2006 [1]. It is designed to cover the "forward" region of the proton-antiproton interaction point at a luminosity of $2 \cdot 10^{32}$ $cm^{-2}s^{-1}$. The experiment will employ a silicon pixel vertex detector to provide high precision space points for an on-line lowest level trigger based on track impact parameters. The "hottest" chips, located at 6 mm from the beam, will experience a fluence of about 10^{14} $cm^{-2}y^{-1}$. This is similar to the high radiation environments at ATLAS and CMS at LHC.

A pixel detector readout chip (FPIX) has been developed at Fermilab to meet the requirements of future Tevatron collider experiments. The preFPIX2 represents the most advanced iteration of very successful chip prototypes [2] and has been realized in standard deep-submicron CMOS technology. As demonstrated by the RD49 collaboration at CERN, the above process can be made very radiation tolerant following specific design rules [3]. The final FPIX will be fabricated using radiation tolerant 0.25 micron CMOS process with enclosed geometry NMOS transistors and guard rings.

We show results of radiation tests performed with preFPIX2 chip prototypes including both total dose and single event effects. The tests have been performed exposing the chip to 200 MeV protons at the IUCF. The comparison of the chip performance before and after exposure shows the high radiation tolerance of the design to protons up to about 26 Mrad total dose. Last year exposures of preFPIXT chips to radiation from a Colbalt-60 source at Argonne National Laboratory verified the high tolerance to gamma radiation up to about 33 Mrad total dose [4].

Total dose effects are not the only concern for reliable operation of the detector. Ionising radiation can induce single event upset (SEU) effects, as unwanted logic state transitions in digital devices, corrupting stored data.

The single event upsets just described do not permanently alter the chip behaviour, but they could result in data loss, shifts of the nominal operating conditions, and loss of chip control. If the single event upset rate is particularly high, it could be mitigated by circuit hardening techniques. If it is not high, the upset rate could be tolerated simply by a slow periodic downloading of data and full system resetting in the worse case. During the irradiation, we set up tests in order to observe the occurrence of single event upsets in the preFPIX2 registers and we measured the corresponding single bit upset cross section.

II. THE RADIATION TOLERANT FPIX CHIP

In order to satisfy the needs of BTeV, the FPIX pixel readout chip must provide "very clean" track crossing points near the interaction region for *every* 132 ns beam crossing. This requires a low noise front-end, an unusually high output bandwidth, and radiation-tolerant technology.

A. The preFPIX2I and preFPIXTb chip prototypes

The road to the desired performances has been paved by fabricating preFPIX2 chip prototypes in deep-submicron technology from two vendors. The preFPIX2I chip, containing 16 columns with 32 rows of pixel cells and complete core readout architecture, has been manufactured through CERN. The preFPIX2Tb chip, contains, in addition to the preFPIX2I chip features, a new programming interface and digital-to-analog converters. It has been manufactured by Tiawan Semiconductor Manufacturing Company. Based on test results, some of them reported here, we intend to submit a full-size BTeV pixel readout chip before the end of the year 2001. That chip will include the final 50 micron by 400 micron pixel cells and high speed output data serializer.

The analog-front end [4] and the core architecture [5] of the pixel readout chips fabricated in deep-submicron CMOS technology have been described elsewhere. In this paper we briefly describe the additional features of the preFPIX2Tb chip because of their relevance in the single event upset tests reported.

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B. Registers in preFPIX2Tb readout chip

The programming interface permits download of mask and charge-injection registers and digital-to-analog (DAC) registers. These registers control features of the chip and minimize the number of connections between the chip and the outside world.

The mask and charge-injection registers consist of small size-daisy chained Flip-Flop's (FF's) and are implemented in each pixel cell. A high logic level stored in one of the mask FF's disables the corresponding cell. This is meant to turn off noisy cells. Analogously, a high logic level stored in one of the charge-injection FF's enables the cell to receive at the input an analogue pulse for calibration purposes. Thus, there are two independent long registers, which are serpentine through the chip. In the preFPIX2Tb periphery, there are 14 DAC registers implemented, each one 8 bits long. The stored digital value is translated to in an analogue voltage or analogue current to set bias voltages, bias currents and threshold discriminators.

The FF's for DAC registers are of larger size than the FF's for the shift-registers. In fact, the DAC FF's are more complex and uses larger size NFET devices. The reason for this choice is the high reliability required for the DAC registers, which regulate the operational point of the cells.

III. EXPERIMENTAL SETUP

C. Irradiation facility at IUCF

The proton irradiation tests took place at the Indiana University Cyclotron Facility where a proton beam line of 200 MeV kinetic energy is delivered to users. The beam profile has been measured by exposing a sensitive film. The beam spot, defined by the circular area where the flux is not less than 90% of the central value, had a diameter of about 1.5 cm, comfortably larger than the chip size (the larger chip is preFPIX2Tb which is 4.3 mm wide and 7.2 mm long). Before the exposure the absolute fluence was measured by a Faraday cup; during the exposure by a Secondary Electron Emission Monitor. The cyclotron has a duty cycle factor of 0.7% with a repetition rate of about 17MHz and most of the tests were done with a flux of about $2 \cdot 10^{10}$ protons $cm^{-2}s^{-1}$.

The irradiation was done in air at room temperature, and no low energy particle or neutron filters were used. The exposures with multiple boards were done placing the boards about 2 cm behind each other and with the chips facing the beam. Mechanically, the boards were kept in position by an open aluminium frame. The beam was centred on the chips. The physical position of the frame was monitored constantly by a video camera to ensure that no movements occurred during exposure.

We irradiated 4 boards with preFPIXI chips to 26 Mrad (December 2000), one board with preFPIX2Tb to 14 Mrad (April 2001), and recently 4 boards with preFPIX2Tb to 29 Mrad (August 2001). One of the boards with preFPIX2Tb chips on it was irradiated twice collecting 43 Mrad total dose. Due to the alignment precision and measurement technique employed, the systematic error on the integrated fluence is believed to be less than 10%.

D. Hardware and software

Each chip under test was wire-bonded to a printed circuit board in such a way that it could be properly biased, controlled and read out by a DAQ system. The DAQ system was based on a PCI card designed at Fermilab (PCI Test Adapter card) plugged in a PCIbus extender and controlled by a laptop PC. The PTA card generated digital signals to control and read back the readout chips. The software to control the PCI card IO busses was custom and written in C-code. The PCI card IO busses were buffered by LVDS differential driver-receiver cards near by the PCIbus extender located in the counting room. The differential card drove a 100 foot twisted pair cable followed by another LVDS differential driver-receiver card which finally was connected with a 10 foot flat cable to the devices under test. All the DAQ electronics were well behind thick concrete walls, protecting the apparatus from being influenced by the radiation background from the cyclotron and from activated material.

IV. ANALYSIS AND RESULTS

E. Performed tests

1) Bias currents monitor

During the irradiation tests, the analogue and digital currents where continuously monitored by a GPIB card. The analogue current decreased slightly and the digital currents increased slightly during the proton exposure.

2) Noise and threshold dispersion

The noise and the discriminator threshold of each individual cell were measured before and after the irradiation in exactly the same bias conditions for the four preFPIX2I chips[2]. Every cell works after irradiation with a noise about 10% less and a decrease of about 20% in the threshold dispersion among cells. Figure 1 and 2 show the noise and threshold distributions of a preFPIXI chip irradiated with a proton dose of 26 Mrad.

3) Single Event Upsets (SEU)

In our tests, a great deal of attention was focused on measuring radiation induced digital soft errors. We concentrated our effort on the preFPIX2Tb registers storing the initialisation parameters, because they have a large number of bits and the testing procedure is easy to prepare. The results obtained allow prediction of the performance of other parts of the chip potentially affected by the same phenomena.

[2] The results for the four preFPIXTb chips are going to be available in early October '01.

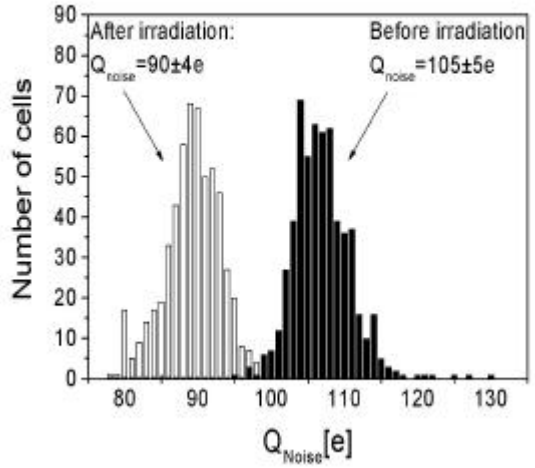

Figure 1: Measured amplifier noise in the 576 cells of preFPIX2I before and after 26 Mrad of 200 MeV proton irradiation.

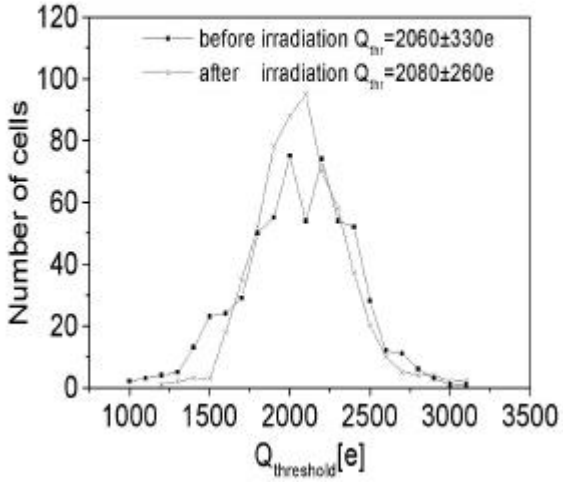

Figure 2: Measured discriminator threshold in the 576 cells of preFPIX2I before and after 26 Mrad of 200 MeV proton irradiation.

The single event upset tests performed are very similar to the ones reported in reference [6]. The SEU measurements consisted of detecting single bit errors in the values stored in the registers. The testing procedure consisted of repeatedly downloading all the registers and reading back the stored values after one minute. The download and read-back phases took about 3 seconds. The download of the parameters was done with a pattern with half of the stored bits having a logical value 0 and the other half having a logical value 1 (except in one case, see Footnote 3). For the shift-registers, the patterns were randomly generated at every iteration loop. For the DAC registers, the patterns were kept constant. A mismatch between the read-back value and the download value is interpreted as a single event upset due to the proton irradiation. No errors were observed in the system with the beam off and running for 10 hours.

In a specific test, the mask register of one board was operated in clocked mode with a clock frequency of 380 kHz. The low clock frequency value was due to our DAQ limitation. In this test, the mask register was downloaded with a logical level 1 in each flip-flop, in order to increase the statistics in view of the fact that a stored logical level 1 is easier to upset with respect to a logical level 0 (see results). After the initialisation, a continuous read cycle was performed and stopped every time a logical level 0 was detected. We collected 14 errors for an effective integrated fluence of $5.8 \cdot 10^{13}$ protons cm^{-2}.

A summary of the total single bit errors detected in the preFPIX2Tb readout chips, together with other relevant quantities, is shown in Table 1. The value in square brackets represents the initial stored logical level of the upset bit. One of the boards (indicated as board 4 in Table 1) was placed not orthogonal to the beam, as the other ones, but at 45 degrees to explore possible dependence of the error rate on the beam incident angle. The number of single bit upsets, for an equal amount of total dose, is statistically consistent among the various chips. In addition, the data do not show any statistically significant difference in the error rate between the tilted board and the other ones.

Table 1: Total single bit errors in preFPIX2Tb registers.

Board	Integrated Fluence (cm^{-2})	Errors in shift-regs (1152 bit)	Errors in DAC regs (112 bit)
1	$2.33 \cdot 10^{14}$	53=18[0] +35[1]	10=8[0]+2[1] [3]
1	$3.65 \cdot 10^{14}$	80=23[0] +57[1]	20=8[0] +12[1]
2	$3.65 \cdot 10^{14}$	74=22[0] +52[1]	19=9[0] +10[1]
3	$3.65 \cdot 10^{14}$	86=27[0] +59[1]	19=8[0] +11[1]
4	$3.65 \cdot 10^{14}$	77=14[0] +63[1]	31=19[0] +12[1]

Table 2: Single bit upset cross section in preFPIX2Tb registers.

Flip-flop	Mode	Cross section (10^{-16} cm^2)
Shift-regs 0 to 1	Un-clocked	1.0±0.1
Shift-regs 1 to 0	Un-clocked	2.7±0.2
Shift-regs 1 to 0	Clocked (380kHz)	4.2±1.2
DAC regs 1 to 0	Un-clocked	5.5±0.6

It is common practise to express the error rate of a register as a single bit upset cross section, defined as the number of errors per bit per unit of integrated fluence. The single bit upset cross section has been computed for the shift-registers and for the DAC registers. The results are shown in Table 2. Only the statistical error on the cross section has been considered. For the shift-registers, the cross section has been computed separately for the radiation induced transition from 0 to 1 and from 1 to 0 because the data have enough precision to show the existence of an asymmetry.

[3] The observed asymmetry in this case is due to the unequal numbers of zero's (82) and one's (30) downloaded into the DAC registers.

The high beam fluence used during the irradiation was of some concern regarding any saturation effect in the error rate. To study this, we collected some data at a fluence of about $4 \cdot 10^{9}$ protons $cm^{-2}s^{-1}$, about 5 times less than the nominal fluence. In this short test, only one board was irradiated (Apr. '01 test) and the single bit cross section was measured to be $(1.4 \pm 1) \cdot 10^{-16}$ cm^{2} and $(3.5 \pm 1.6) \cdot 10^{-16}$ cm^{2} for the shift-registers and $(7 \pm 5) \cdot 10^{-16}$ cm^{2} for the DAC registers in un-clocked mode, statistically compatible with the results at higher fluence.

F. Discussion of the results

No power supply trip-offs or large increases in the bias currents were observed during the irradiation. There is no evidence of single event latch-up or of significant radiation induced leakage currents. Moreover, the absence of noisy cells and no large difference in individual thresholds due to irradiation, strongly suggest that single event gate rapture is not a concern.

The prediction of the single bit upset cross section is very difficult because a lot of parameters came into play [7]. Nevertheless, some gross features of the data can be understood simply by some general considerations.

The disparity in the cross section between the shift registers and the DAC registers is likely caused by the different size of the active area of the NFET transistor, which is larger for the DAC register FF's. Besides that, the DAC register FF's have a more complicated design and an increase in complexity, as a rule of thumb, translates to a larger number of sensitive nodes that can be upset.

The SEU asymmetry for the transition from 0 to 1 with respect to 1 to 0 can be explained in terms of the FF design. The FF's of the shift-registers are D-FF's implemented as cross-coupled nor-not gates. Such a configuration has different sensitive nodes for 0 to 1 and 1 to 0 upsets. No such an asymmetry is expected at all for the DAC registers because the FF's are D-FF's implemented as cross-coupled nor-nor gates. This symmetric configuration has the distribution of sensitive nodes for low logical level the same as when a high logical level is stored.

A decrease of the energy threshold for single bit upset has been reported (in reference [6]) for a static register in clocked mode with respect to unclocked mode. Our data, taken with a clock frequency of 380 kHz, do not show a statistically significant difference from the data taken in the unclocked mode.

In reference [8] a beam angular dependence is expected for devices with very thin sensitive volumes that have Linear Energy Transfer (LET) threshold over 1 MeV cm^{2}/mg and tested with 200 MeV protons. We didn't observe any dependence of the upset rate on the beam incident angle. In fact, due to the smaller device size of the deep submicron elements, the sensitive volumes are more like cubic than slab shaped.

V. CONCLUSIONS

The results of the total dose test validate the deep submicron CMOS process as radiation tolerant, particularly suitable for pixel readout chips and other electronics exposed to large integrated total dose. The single event upset cross sections of static registers are relatively small, but measurable (10^{-16} to $5 \cdot 10^{-16}$ cm^{2}). The experience gained from the gamma and proton irradiation of pre-prototype chips has been of importance in allowing us to proceed with the submission of a full-size BTeV pixel readout chip and developing an approach to handle SEU.

VI. ACKNOWLEDGEMENTS

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