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# LARGE SIGNAL MODEL OF A FOUR-QUADRANT AC TO DC CONVERTER FOR ACCELERATOR MAGNETS

R. de la Calle, R. Garcia Gil*, L. Rinaldi**, F. Völker

* Visitor from LEII, University de Valencia, Spain
** OCEM, S.p.A., Italy

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# Large Signal Model of a Four-Quadrant AC to DC Converter for Accelerator Magnets

R. García Gil[1,2], R. de la Calle[1], F. Völker[1], L. Rinaldi[3]

[1] CERN. Geneva, Switzerland

[2] LEII Dpto. Ingeniería Electrónica. Universitat de València

[3] O.C.E.M. S.p.A, Italy

## Abstract

This paper presents the large signal model of a four-quadrant AC to DC converter, which is expected to be used in the area of particle accelerators. The system's first stage is composed of a three-phase boost PWM (Pulse Width Modulated) rectifier with DSP (Digital Signal Processing) based power factor correction (PFC) and output voltage regulation. The second stage is a full-bridge PWM inverter that allows fast four-quadrant operation. The structure is fully reversible, and an additional resistance (brake chopper) is not needed to dissipate the energy when the beam deflection magnet acts as generator.

## 1. Introduction

In particle accelerators the beam trajectory is controlled by precise magnetic fields generated by a large number of magnets. These magnets require power supplies capable of providing precise DC currents with very little drift and low noise (output current precision < 100 ppm). The correction field in these magnets can be either positive or negative, so true bipolar power converters are needed. Moreover, some of these converters have to provide smooth zero-crossing of the load current and fast response to generate the required current functions, with di/dt up to several kA/s.

Present trends in power electronics aim at making efficient use of mains power, both from the point of view of energy recuperation and from the interaction of the power equipment with other main users. To achieve the first requirement, a true four-quadrant power converter will give back energy to the mains when the beam deflection magnet acts as a generator. The second requirement implies a unity displacement power factor (DPF) at the input and a very low total harmonic distortion (THD) of the input current; therefore, power factor correction (PFC) is required. A new standard such as the IEC 1000-3-2 is becoming compulsory regarding limitation of the total harmonic distortion of power equipment.

The block diagram of the whole system is shown in figure 1. The basic system's first stage configuration is a so-called Current Source Rectifier (CSR) or Voltage Source Inverter (VSI). It consists of a three-phase boost rectifier made up of six switches, bi-directional in current but not in voltage, on account of the internal anti-parallel diodes of the IGBTs. However, for the application under consideration, where both rising and falling DC current has to be controlled, bipolar load voltages are required. Therefore a second stage with a full-bridge IGBT inverter is needed. The output voltage and current regulation is done in this second stage.

The VSI is seen from the AC side as a PWM voltage generator producing chopped waveforms. With the addition of a small inductor $L_i$, the input currents will be continuous with superimposed triangular ripple. Hence very little additional EMI filtering is required compared with the three-phase buck rectifier.

The high-frequency switching harmonics are filtered and have little influence on the low-frequency AC components of the waveform. This fact allows the elimination of the high frequency components in the analysis for a better understanding of the whole system. This leads us to the large signal model, which will be simulated using SIMPLORER[1]. The switches of each phase of the converter are controlled to obtain unity power factor at the input and voltage regulation at the DC-link. To obtain an undistorted line current waveform, the DC-link output voltage $V_o$ must in any case be larger than the peak line-to-line AC mains voltage.

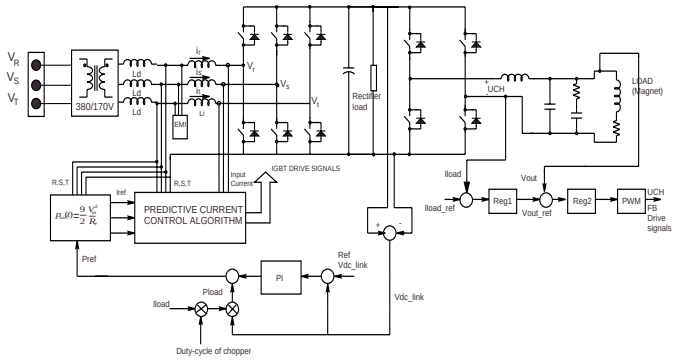



***Fig. 1.*** *Block diagram of the magnet power converter*

A 50 kW (± 170 V and ± 300 A) current source matrix converter was developed by OCEM/Italy[2]. A DSP based Space Vector Modulation (SVM) is used to control both the power factor at the AC input and the voltage at the DC-link. This digital control is implemented by a Texas

[1] SIMPLORER is a registrated trademark of Simec GmbH

[2] http:www.ocem.com

Instrument TMS320C32 DSP that provides the switching signals that are the inputs of the PWM switch sequencer.

A switching frequency of 16 kHz has been chosen for both the CSR and the full-bridge inverter (the two clocks being synchronised), with the aim of minimising the size of the reactive components whilst keeping switching losses at an acceptable level.

## 2. Large Signal Model

A better understanding of the converter shown in figure 1 can be obtained by neglecting switching ripple and by modelling only the underlying lower frequency AC variations in the waveforms [1]. The high frequency ripple in the inductor current and in the capacitor voltage waveforms is removed by averaging over one switching period.

The resultant model is not a linear model, hence it cannot be directly used to calculate small-signal transfer functions, output impedance and other frequency-dependent properties for stability analysis. But small signal response can be easily obtained by superimposing small AC variations onto the working point by AC analysis with SIMPLORER, PSPICE or other simulation tools.

The large signal model obtained, according to [2], [3], [4] and [5], is shown in figure 2, where the average of the switching functions is made by replacing them by the duty cycle that corresponds to each switch. Figure 2 also includes the average model of the full-bridge inverter with both voltage and current control loops.

## 3. Current Source Rectifier with Power Factor Correction Modulation Laws

According to the circuit of figure 2, the modulation laws can be obtained if we consider that each input basic cell can be represented by the following differential equation:

$$\begin{bmatrix} V_{rs} \\ V_{st} \\ V_{tr} \end{bmatrix} = \vec{d} \cdot V_o = \begin{bmatrix} d_{rs} \\ d_{st} \\ d_{tr} \end{bmatrix} \cdot V_o = \begin{bmatrix} V_{RS} - 3 \cdot L_i \dfrac{di_{rs}}{dt} \\ V_{ST} - 3 \cdot L_i \dfrac{di_{st}}{dt} \\ V_{TR} - 3 \cdot L_i \dfrac{di_{tr}}{dt} \end{bmatrix} \qquad (1)$$

Here $V_{RS}$, $V_{ST}$, $V_{TR}$ are the line-to-line voltages of a balanced system with amplitudes $V_m$, and $d_{rs}$, $d_{st}$, $d_{tr}$ are the so-called modulation laws that will be generated by the DSP controller. To obtain a power factor near to unity, the desired line-to-line input currents $i_{rs}$, $i_{st}$ and $i_{tr}$ have to be sinusoidal and in phase with the mains voltages. With these conditions, all variables of equation (1) are known, except the peak input current $I_m$ of each line-to-line input currents, which can be calculated considering that the instantaneous power flow ($p_{tot}$) in any balanced three-phase AC system is constant and is given by the following equation:

$$I_m = \frac{9}{2} \cdot \frac{p_{tot}}{V_m} \qquad (2)$$

Solving the equations in (1), the following modulation laws are found as equations (3), (4) and (5):

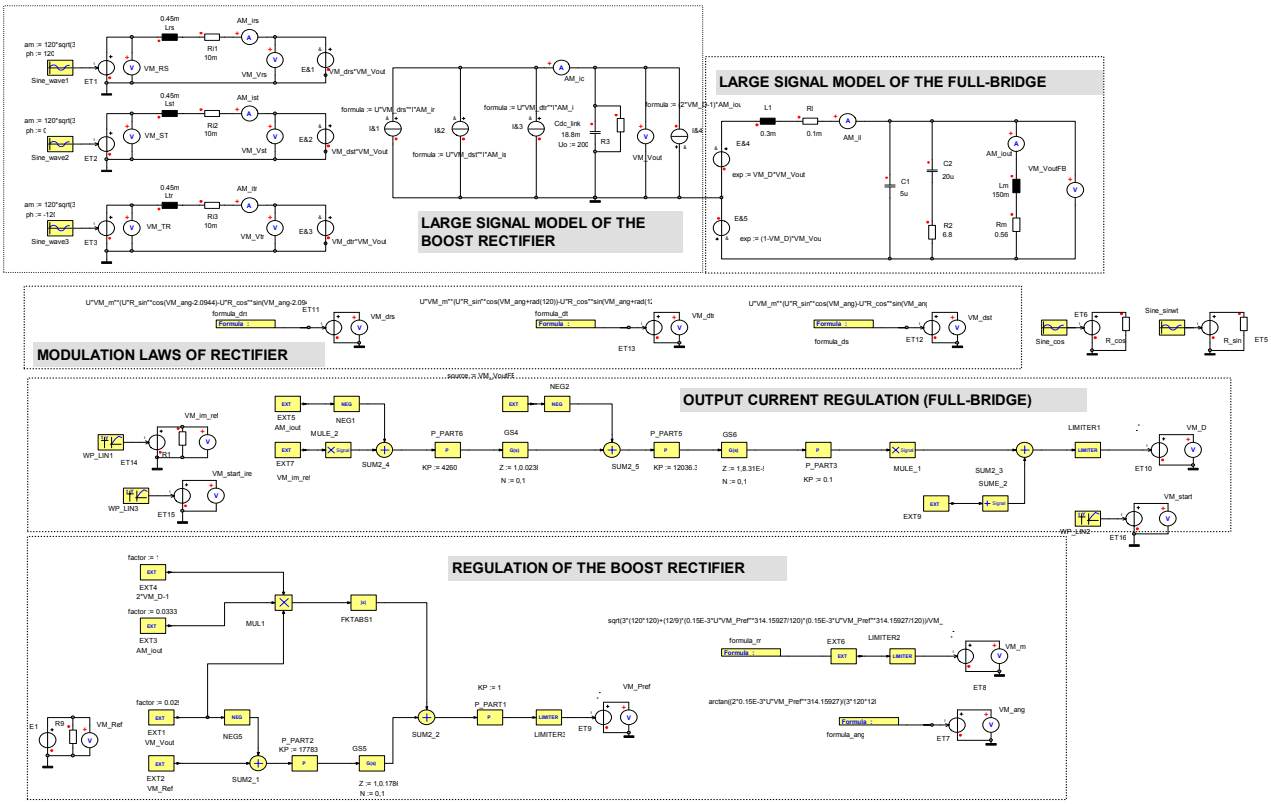



***Fig. 2:*** *SIMPLORER schematic. This block diagram includes the large signal model of CSR, with its regulation loop (DSP based) and the large signal model of the full-bridge inverter with the analog output current regulation loop.*

$$d_{rs}(t) = m \cdot \sin\left(\omega t - \theta + \frac{2\pi}{3}\right) \quad (3)$$

$$d_{st}(t) = m \cdot \sin(\omega t - \theta) \quad (4)$$

$$d_{tr}(t) = m \cdot \sin\left(\omega t - \theta - \frac{2\pi}{3}\right) \quad (5)$$

with,

$$m = \frac{1}{3} \cdot \sqrt{9 \cdot V_m^4 + 4 \cdot L_i^2 \cdot P_{out}^2 \cdot \omega^2} \cdot \frac{\sqrt{3}}{V_m \cdot V_o} \quad (6)$$

$$\theta = a\tan\left(\frac{2}{3} \cdot L_i \cdot P_{out} \cdot \frac{\omega}{V_m^2}\right) \quad (7)$$

Here $0 \le m \le$ is named the modulation index and θ is the phase-shift introduced by the input filter. Assuming the switching frequency to be sufficiently high, the filter inductors $L_i$ can be small and then the angle θ from equation (7) tends to zero. So a nearly sinusoidal modulation law is applied, and the modulation index m can be approximated by:

$$m\ (L_i \to 0) = \frac{\sqrt{3} \cdot V_m}{V_o} \quad (8)$$

This expression represents the static voltage gain of the system. In steady state, the output DC voltage is kept constant and the phase currents are controlled to be sinusoidal and in phase with the corresponding input phase voltages. To obtain undistorted line current waveforms *m* must be ≤ 1 and the output DC voltage > $\sqrt{3} \cdot V_m$ (the peak of the line to line voltage). In a practical case a typical value of *m* is found between 0.8 and 0.9.

## 4. Power Factor Correction and DC-link Voltage Regulation

The power factor regulation is performed through the modulation laws by imposing the amplitude and the angle of the AC input current through equations 1 to 7. This is implemented digitally by means of the Predictive Current Control Algorithm explained in [6].

The block diagram of the feedback system is shown in figure 3. The control network is a lag (PI) compensator, which has been designed to compensate the R-C output filter, where C is the DC-link capacitor and R is the equivalent load resistance at the DC-link level. This R-C output filter can be represented by the following transfer function:

$$\frac{\tilde{v}_{dc\_link}}{\tilde{p}_{tot}} = \frac{R}{V_{dc\_link}} \cdot \frac{1}{1 + s \cdot \frac{R \cdot C}{2}} \quad (9)$$

where the input represents the power given by the rectifier ($\tilde{p}_{tot}$) and the output is the DC-link voltage ($\tilde{v}_{dc\_link}$).

The PI compensator is designed to compensate the minimum load condition, which is the worst case as far as stability is concerned, and has the following transfer function:

$$D(s) = K \cdot \frac{1 + s \cdot \tau}{s} \quad (10)$$

with K = 17783 and τ = 0.1786

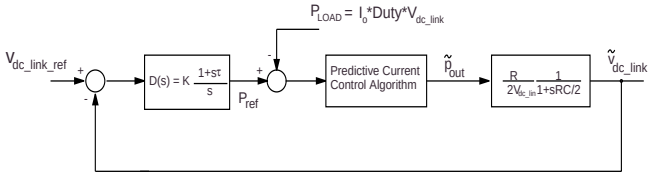



***Fig 3:*** *Block diagram of voltage regulation at the DC-link*

To be implemented in the DSP this PI compensator is transferred into the z-plane.

The acquisition board of the DSP samples the DC-link voltage and compares it with the reference voltage (fixed at 250 V). The error voltage passes through the PI compensation circuit whose output becomes a power reference $P_{ref}$ for the rectifier control.

For the second control loop the reference is the power that the rectifier has to supply to the load, which is compared with the actual load power $P_{LOAD}$. This power is calculated by knowing the duty cycle of the output full-bridge inverter and by sampling the magnet current and voltage at the DC-link.

The DSP calculates the input current reference by imposing a unity power factor and by measuring the phase voltage at the AC input. The DSP assumes that the power given by a balanced three-phase system is constant and given by equation (2). Consequently the power reference is converted into an AC current reference. Finally the DSP implements the Predictive Current Algorithm according to the modulation laws defined by equations (3), (4) and (5), and this guarantees that the AC input currents will be in phase with the mains voltages.

## 5. Output Current Regulation

The regulation proposed is included in figure 1 and has been implemented in an analog way. There are two loops: the internal one (a fast loop with lower accuracy) regulates the voltage UCH at the full-bridge output, and the second one (slower but of higher precision) regulates the magnet current. For the design of this control system the load is made of L=150 mH and R=0.56 Ω. The current reference can have a trapezoidal shape with rounded corners. The high precision is reached only during the flat-top while in the ramps there is a tracking error of about 1 %.

## 6. Simulation and Experimental Results

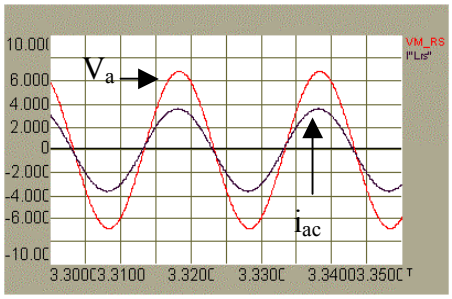
To demonstrate the concepts presented in the previous paragraphs, the average model was simulated using SIMPLORER. The schematic, shown in figure 2, includes the modelled three-phase CSR and the full-bridge inverter, both with their respective feedback loops. The use of SIMPLORER has allowed the simulation of the whole system without convergence problems, while reducing the time needed for each simulation as compared with PSPICE. The average model is not only used for the control design, but is also much more efficient in

simulation than the switching model, where often it is difficult to converge for such a discrete high order system.

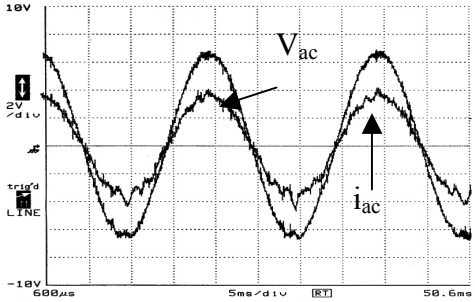
The comparison between simulated and experimental results is presented below and shows a good agreement. Figure 4 shows the AC input current and voltage waveforms at maximum load condition (300 A). It can be seen that the phase voltage and current are almost in phase, i.e. the power factor is one. Obviously the experimental current waveform is not exactly sinusoidal as only the first harmonic is considered in the simulation.

Figure 5 shows a current step from –110 A to 0 with a ramp of 100 A/100 ms. Special attention must be given to the overshoot of the DC-link voltage when a current reference step is applied.

Parasitic loss elements, such as the inductor equivalent series resistance (ESL), would cause a lower damping factor to be observed. In the simulated circuit shown in figure 2, a higher ESL component has been taken to improve the simulation time. As a result, the simulated voltage at the DC-link, shown in figure 5a, needs much more time to reach the steady-state than the measured one shown in figure 5b.




*a) Simulated*

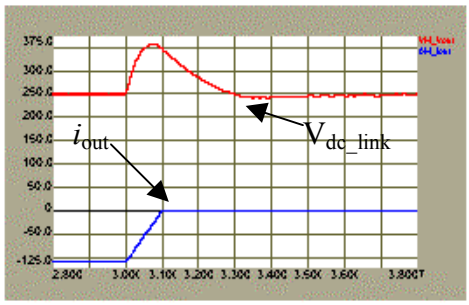



*b) Experimental*

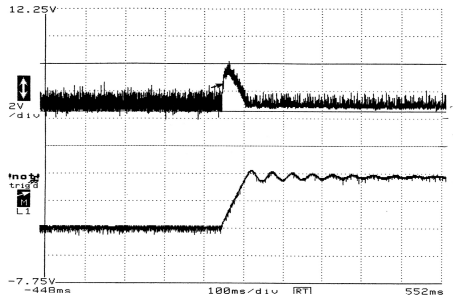
***Fig. 4:*** *AC input current and voltage waveforms at R phase, where a good power factor is obtained. Set-up conditions:*

## 7. Conclusions

In this paper, the large signal model of a four-quadrant AC to DC converter for particle accelerator applications has been analysed. The whole system has been simulated with SIMPLORER, where the power block has been replaced by its average model. The average model is used not only for control design but also to perform overall simulations over a longer time, being much more efficient than the switching model, which sometimes has convergence difficulties. The simulated results show a good agreement with the experimental ones.




*a) Simulated*



*b) Experimental*

***Fig. 5:*** *Response of the voltage at the DC-link for a current step of –110 to 0 A. Set-up conditions: (1) $V_{dc\_link}$(ac): 20 V /div; (2) $i_{out}$: 60 A/div.*

## 8. Acknowledgement

The authors would like to thank G.Basile/OCEM for having decided to develop this prototype power converter as a R&D investment. Our thanks go also to A.Coraluppi and L.Rinaldi/OCEM, for their enthusiasm and effectiveness during the development, the final tests and the documentation of the equipment.

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