Fast Pre-Trigger Electronics of T0/Centrality MCP-Based Start Detector for ALICE

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(For the ALICE collaboration)

Abstract

This work describes an alternative to the current ALICE baseline solution for a TO detector, still under development. The proposed system consists of two MCP-based T0/Centrality Start Detectors (backward-forward isochronous disks) equipped with programmable, TTC synchronized front-end electronic cards (FEECs) which would be positioned along the LHC colliding beam line on both sides of the ALICE interaction region. The purpose of this arrangement, providing both precise timing and fast multiplicity selection, is to give a pre-trigger signal at the earliest possible time after a central event. This pre-trigger can be produced within 25 ns. It can be delivered within 100 ns directly to the Transition Radiation Detector and would be the earliest L0 input coming to the ALICE Central Trigger Processor. A noise-free passive multichannel summator of 2ns signals is used to provide a determination of the collision time with a potential accuracy better than 10 ps in the case of Pb-Pb collisions, the limit coming from the electronics. Results from in-beam tests confirm the functionality of the main elements. Further development plans are presented.

I. Introduction

A fast pre-trigger decision (which can be made within one 25 ns bunch crossing) for the ALICE experiment at the LHC should handle the following functions([1]):

(i) precise T0 determination (better than 50-100 ps resolution);

(ii) centrality of the collision determination;

(iii) min-bias pre-trigger production within 100 ns after the collision for the Transition Radiation Detector;

(iv) coordinate of primary vertex (indication of collision with the interaction diamond);

(v) beam-gas interaction signal;

vi) indication of the pile-up signal.

These functions could be combined into one logic signal or a set of signals forwarded to the Central Trigger Processor (CTP).

This work is a continuation of [2] and [3], combining both the upgrade of the functional pre-trigger scheme, new developments and the in-beam test results of the fast detector and electronics.

II. Functional scheme

The fastest pre-trigger decision in the ALICE detector could be made using the information from two T0/Centrality disks covering 2.5-3.5 regions of pseudorapidity on both sides of interaction region. The system is based on the application of Microchannel Plates (MCPs). The signals from these MCP detectors are very short (less than 2 ns at the base), they allow very precise timing and their pulse height is proportional to the multiplicity. It is possible to use these features for the fastest preliminary decision making done by the ALICE pre-Trigger. The extremely good timing resolution and counting rate properties of the MCP-based detector implies the possibility to obtain the first fast indication of a central event within two neighbouring 25 ns bunch crossings in case of pp collisions.

A. Detector

Detectors are placed symmetrically on both sides of the interaction region [4]. They are hermetically sealed inside thin-wall disk vacuum chambers. A multianode MCP isochronous readout system provides the needed high accuracy in timing measurements. Passive summation of signals from the anode of the segmented MCP disk gives a multiplicity signal with very precise timing properties. The pre-trigger decision is based on the information obtained for each bunch crossing on the total multiplicity for the event in a given rapidity range (2.6-3.6), primary vertex Z-location within the interaction region , while permitting the rejection of beam gas events. A general functional scheme of a fast trigger is shown in Figure 1.

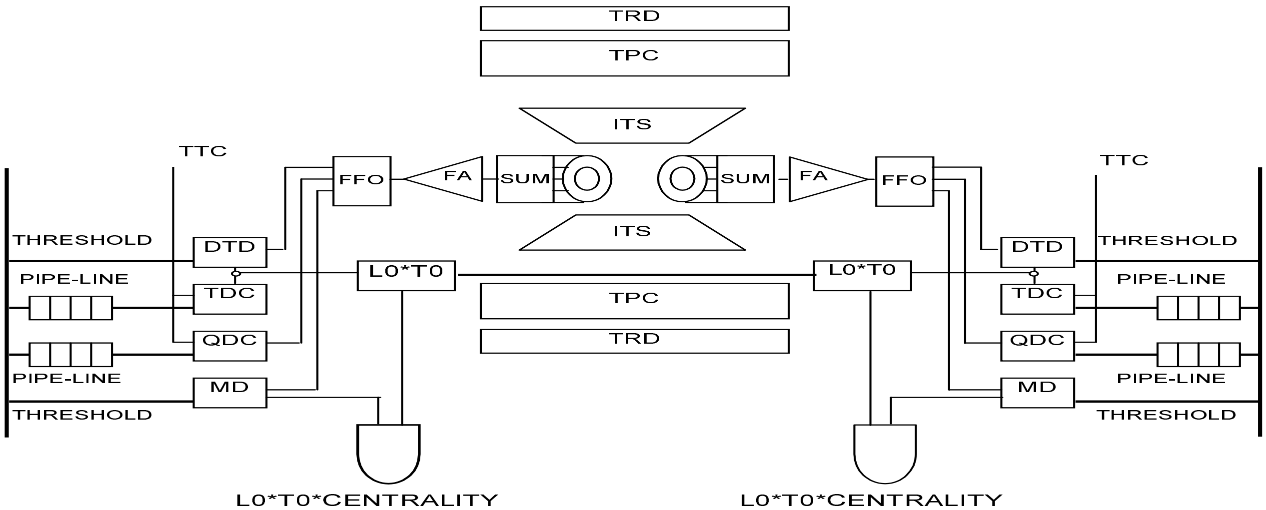

Figure 1: Functional scheme of ALICE pre-trigger T0/Centrality detectors and electronics. Two MCP based disks are situated on both sides (”backward-forward”) of the interaction region. The ALICE’s Inner Tracking System (ITS), Time Projection Chamber (TPC) and Transition Radiation Detector (TRD) are shown schematically (not to scale). SUM - passive multichannel summator of short 2ns pulses; FA - fast amplifiers; FFO - fast fan-out; DTD - Double Threshold Timing Discriminator; TDC,QDC - time and charge digital converters; MD - fast multiplicity discriminator; L0*T0 -Fast Programmable Logic Unit.

B. General Scheme

The new scheme of the fast front-end electronics (ALICE L0 trigger electronics or ALICE pre-trigger) integrated for each half of two MCP T0/Centrality disks into one Front-End Electronics Card (FEEC) is represented here in Fig. 1. The scheme is based on the passive multichannel summator application which is integrated into the detector design providing the noiseless precise summation and isochronous timing for a large area MCP disk while preserving the charge information.

As previously mentioned [1], precise timing from a large area detector implies a high granularity of the detector elements (cells) This is because individual elements must be small in order to minimize the signal propagation spread within a given cell. Using the most straightforward approach, one would have to develop about 300 fast electronics channels with very high precision timing properties matching the total number of pads in a MCP disk that covers 1 unit of pseudorapidity. In order to simplify the task, we propose to use the isochronous summation of signals from many pads belonging to one disk, preserving the timing precision and good linearity of the pulse heights. The proposed use of noise-free passive isochronous summators has the advantage of a strong decrease in the number of electronic channels and simplifies considerably the fast logic for multiplicity and timing. The analogue signal from the passive UHF summator output is used for the LO trigger applications (see splitter FFO on the Fig. 1). In general the duration of a signal from the MCP detector is about 2 ns with 200-300 ps peaking time. This implies a UHF requirement for the design and development of the fast electronics (1GHz frequency range).

C. Fast Front-End Electronics Cards

Each FEEC integrates preamplifiers , QDC chips, pipeline FIFO and new type fast TDC chip (we supposed to apply the developments started in[5]). FEEC contains also the interface between the L0-Trigger electronics and DAQ system.

The FEECs are situated close to the T0/Centrality MCP disks providing service to one half of the disk or for the whole disk (a baseline option). The FEEC contain the following (programmable) units:

(i) fast input signal splitters (FFO) matched in impedance with transmission lines coming from the fast pre-amplifiers (50 Ohm) and the inputs to discriminators;

(ii) a fast analogue single threshold discriminator for multiplicity analysis (MD);

(iii) a fast timing discriminator (TD) which provides precise time mark of the incoming analogue sum signal for a given MCP half-disk;

(iv) a fast TDC for precise timing of the incoming signal;

(v) a fast 8 bit QDC for charge digitization of the signal for a given disk.

(vi) a pipe-line for storing the MCP disk data during the L0 decision making. Only about 240bytes per card are required for storage of data from all 40MHz bunch crossings during 3mks time.(Here we apply some extra margins).

(vii) The FEEC also provides the place for the TTC adaptors (TTCrx chip) and elements for the connection to the DDL. (This should be developed in the future using the standard approach for ALICE.)

D. Functions

Centrality of collisions:
We use the pulse height analogue sum from the MCP disk to make selections based on multiplicity. This is done by a fast Multiplicity Discriminator [6] which gives the logic signal as an indication of high multiplicity event. A minimum-bias pre-trigger signal could be delivered within 100 ns directly to the ALICE Transition Radiation Detector (the TRD start). Selection on multiplicity, which is done by the fast Multiplicity Discriminator(MD), would provide the earliest L0 input signal coming to the Central Trigger Processor [8].

Event vertex location:
The fast vertex determination is done by time of flight difference measurements (50ps timing resolution is to provide about 1.5 cm accuracy).

Precise T0 signal for TOF system:
The general LHC TTC distribution ("the LHC clock") is included as the most efficient and independent "start" signal in TOF measurements for each of MCP disk detectors. Any possible TTC jitter would not affect these timing measurements results because the present design implements isochronous measurements done using two disks. Proposals for a TOF measuring system using very fast time-to-digital precise converters (TDC) were suggested earlier [3]

A precise T0 signal could be supplied in two ways:

1) By the hardware electronics ("meantimer" device) that is supposed to provide the T0 relevant to the collision vertex coordinate Z.

2) By software TOF off-line data treatment using precise "left" and "right" T0 data obtained by the relevant TDCs. This is considered as the most suitable option.

Pre-trigger signal:
Logic signals L0*T0*Centrality from the TDC and from the multiplicity discriminator are the result of two criteria (multiplicity and vertex location)being satisfied for each MCP disk. The Programmable Fast Coincidence Logic (PL) provides the necessary logic decisions concerning the location within the interaction diamond, pile up and beam-gas interaction logical signals. A pipe-line of about 120 cells depth is proposed to store the 8 bit multiplicity information from individual disk Thus the reliability of the fast L0 decisions can be monitored and the multiplicity data for a given selected event fed to the DAQ.

"Wake-up" signal for TRD
Two Programmable Logic (PL) units (left and right) placed near the MCP disks are connected by 1.5m cable passing outside the ITS cylinder surface. This thin signal cable is used for the transfer of the minimum bias MD logical signals. Another two signal cables (left and right) transfer the TDR pre-trigger signals to the left and right parts of the TRD pre-trigger signal distribution system (SDS). We suppose that 10 m cable length is a reasonable estimate to get a signal from the T0/centrality PL card to the input of the TDR SDS providing 60-80ns delay after the collision.

T0/Centrality MCP Detector Data Link
The simplest evaluations of the T0/Centrality MCP Detector Data Link (DDL) feasible distribution have been made taking into account total amounts of data from the detector (240 bytes/event), a limitation for a total readout time ($< 140\ \mu$sec) and a suggested DDL transfer rate (100 MBytes/sec). Only one DDL is sufficient for the start detector.

Central Trigger Processor(CTP) User Requirements
The L0 decision, - as formulated in [8] - is to be done by the CTP within 1.2 μs which is limited by the signal propagation time from the detector to the trigger crate. This means that (*i*) the minimal depth of the FEEC pipeline should provide at least 1.2μs storage time and that (*ii*) the "wake-up"signal for the TRD should be generated by the FEEC logic and submitted by the shortest way to the TRD Signal Distribution System within the required 100ns limit after the collision.

III. Simulation

Numerical estimates of the ALICE MCP-disks pretrigger efficiency were obtained for various colliding relativistic nuclei at LHC energies. The existing detector response functions and signal shapes, experimental noise levels of the electronics, measured values of efficiency for MIPs, gamma and neutral particle detection were taken into account. Results are shown in Fig. as a function of start detector general efficiency. One can see that in case of O–O,Ar–Ar,Kr–Kr,Sn–Sn and Pb–Pb collisions the pretrigger efficiency will be 100% even for small acceptance detectors. However, in case of pp collisions HIJING and PYTHIA event generators produce considerably different predictions in terms of multiplicity and trigger efficiency. This brings the requirement of 100 % geometrical efficiency for any detector applied as ALICE start counter in case of possible low multiplicity events studies. Estimates for high multiplicity events show that with suitable electronics a limiting time resolution better than 10 ps could be achieved (see Fig. 3). These very promising estimates confirm the use of a noise-free summation concept.

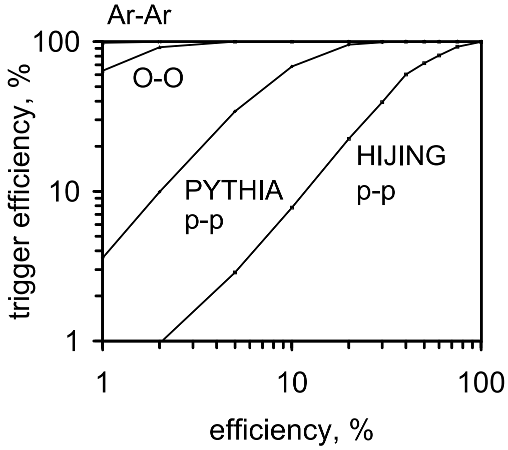

Figure 2: Estimated ALICE pre-trigger efficiency for different colliding relativistic nuclei at the LHC energies vs. start detector general efficiency.

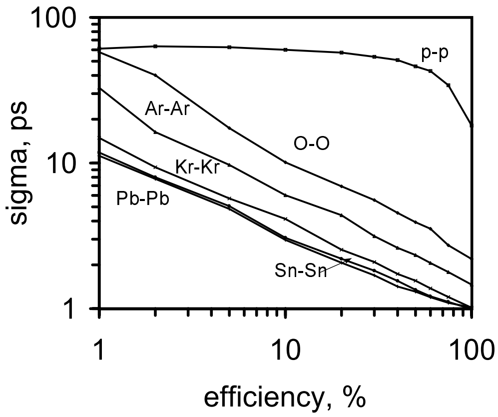

Figure 3: Timing resolution estimated for the case of relativistic nuclei collisions vs. start detector general efficiency.

IV. Passive summators development

The passive summators (see[2,3]) were simplified following the new concept of the start detector [4]. A batch of microelectronics design thin film summators based on circular bridges (see Fig.4) was produced. The application of 0.5mm thick ceramics (instead of previously used 200 microns large area plates) was found to be more successful. In-lab UHF test results for these summators showed the operational frequency range up to 1 GHz. This technology provides the value of signal transfer coefficient at the level of 0.2 that is better then obtained for other types of the summators. The measured response on the 100ps step-function was found also satisfactory: 500ps signal rise-time was obtained that is quite adequate to the requirements. 50 Ohms input and output summator impedances allow possible cascading. One of this summators was used integrated with the MCP detector during the in-beam tests at CERN providing short 2ns (base) signals for MIPs and for high multiplicity events.

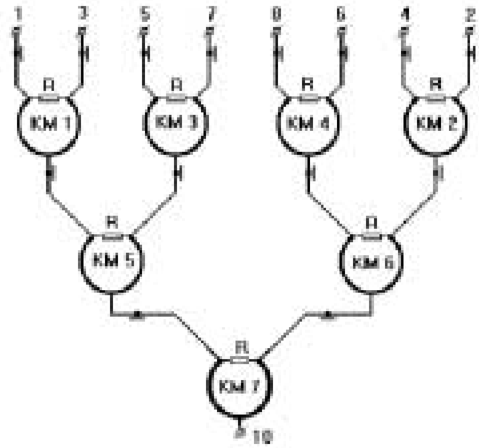

Figure 4: 8-channel passive summator of 2ns signal based on the UHF circular bridges application - general scheme

V. Results of tests

Tests of the main functional elements of the ALICE pretrigger scheme include the in-beam studies of a microelectronic multichannel passive summator (1.0 GHz frequency range), low-noise 50-Ohms impedance preamplifiers (3000e noise in 1GHz range), a fast Multiplicity Discriminator, standard Constant Fraction Discriminators, the Philips Scientific Instruments Timing discriminator

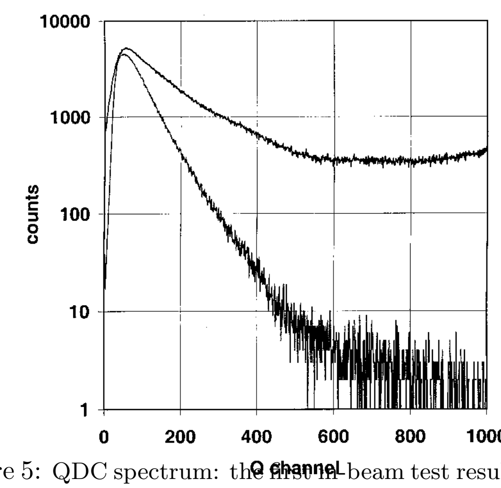

Figure 5: QDC spectrum: the first in-beam test results of multiplicity registration with 5cm Pb target in front of the detector (upper curve) and empty target (low).

It is important to notice here that the short 2ns pulses coming from the detector, the wide dynamic range of signals and variations(distortions) of signal shape observed at the in-beam studies made the use of standard timing CFDs, mentioned above, extremely difficult.

Results of in-beam tests at CERN of the main system elements, including the fast summators, preamplifiers, MD and the DTD, confirmed their functionality. A measured value of 75 ps timing resolution was achieved for MIPs during our in-beam tests at CERN PS, close to the predicted result for a single particle.

The same electronics was used in the first in-beam studies of multiplicity events done with MCP detector. The measurements were performed at the SPS with proton 40 GeV/c beams using a 5cm Pb target positioned in front of the detector. QDC spectra are shown at the Fig.5. The low curve is obtained without any target and demonstrates a single particle detector response function. The high multiplicity events were obtained with Pb target positioned in the beam 13cm from the detector (the upper curve). This spectrum is in line with the first simulations showed wide distribution expected in this case (multiplicities up to 20 are predicted for the given dynamic range).

VI. Plans

Further developments of the electronics are foreseen:

A). Development of the electronic card (FEEC) including the following fast analog devices : MD,DTD, preamplifier-shaper for 2ns signals timing preamplifier, FFO and gain variation unit.

b). Investigation of different ASIC -Application Specific Integrated Circuits) with embedded PL - (Programmable Logic) based configurations for making high speed (40 MHz clock) pre-triggers and precise (50 ps resolution) pipe-lined TOF measurements;

c). The search and study of a suitable schematic approach to charge-to-digital conversion arrangement for the 40 MHz pipe-lined measurement of the charge accumulated by MCP disk ;

B. Concept investigation, design and layout of Detector Data Link/Source Interface Unit protocol and schematic drawings (DDL/SIU) for its arrangement in the MCP front-end electronics :

a). Data readout algorithms and circuitry implementation in FEE.

b). Control algorithms and circuitry implementation in FEE.

C. The investigation and adaptation to the MCP FEEC of the LHC Synchronizing Clock System interface.

D. The concept and initial schematic design of the standard bus-based Fast Programmable Modular Units (PL) for integrated pre-triggers assembling aimed at making ALICE Pre-trigger and Veto signals.

VII. Conclusions

1) New functional scheme of the pre-trigger electronics with very promising features has been developed.

2) The upgraded technology of the microelectronic passive summator integrated with the fast MCP based detector is successfully tested.

3) Results of the in-beam tests of multichannel passive summator and standard available fast electronics modules (timing discriminators, QDC,TDC) developed for other applications confirm the expectations coming from simulations of timing resolution and multiplicity signal measurement(75ps timing resolution is obtained for MIP registration, the 1st multiplicity spectra with Pb target were obtained).

4) Further plans involve the development of the FEEC and continuation of the in-beam studies at high multiplicity environment.

Acknowledgements: Authors are indebted to NA57 Collaboration for the support of these studies, to L.Ulrice and L.Dimovasili for their help with targets during the in-beam tests at CERN, to J.Stachel, G.Valenti and C.Williams for their interest and useful discussions. This job is partially supported by the International Science and Technology Center, Grant No.1666 and by grant from Higher Education Ministry of Russian Federation No.520.

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