Test results of the front−end system for the silicon drift detectors of ALICE

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Abstract

The front−end system of the Silicon Drift Detectors (SDDs) of the ALICE experiment is made of two ASICs. The first chip performs the preamplification, temporary analogue storage and analogue−to−digital conversion of the detector signals. The second chip is a digital buffer that allows for a significant reduction of the connections from the front−end module to the outside world.

In this paper the results achieved on the first complete prototype of the front−end system for the SDDs of ALICE are presented.

I. Introduction

Silicon drift detectors provide *xy* coordinates of the crossing particles with a spatial precision of the order of 30 *μm*, as well as a charge resolution such that the *dE/dx* is dominated by Landau fluctuation. The detector is hexagon−shaped with a total area of 72.5x87.6 mm^2 and an active area of 70.2x75.3 mm^2. It is divided into two 35 *mm* drift regions. At the end of each drift region 256 anodes collect the charge. The pitch of the anodes is 294 *μm*.[1][2]

Each anode has to be readout with a sampling frequency of 40 *MS/s*. The number of samples to be taken per event must cover the whole drift time, which is around 6 *μs*, therefore a number of 256 samples has been chosen. The total amount of data for each half−detector (corresponding to one drift region) is 64 *kSamples*.

The basic idea behind our readout scheme is to convert the samples into a digital format as soon as possible. Due to the tight requirements in term of material and also the small space available on the support structures (ladders) it would be extremely difficult to transmit analogue data outside the detectors at the required speed.

Owing to the low power budget (5 *mW*/channel) it is not possible to have a 40 *MS/s* A/D converter for each channel, therefore a different approach has been adopted. The signal from the detector is continuously amplified and sampled on an 256−cells analogue memory at 40 *MS/s*. When the trigger signal is received the analogue memory stops the write phase and moves to the read phase where its samples are converted by a slower A/D converter. This of course introduces some dead time since during the conversion the system is not sampling the detector signal. The maximum allowed dead time is 1 *ms*/event. A reasonable value for the settling time of the analogue memory is 500 *ns* and a 2 *MS/s* ADC every two channels is also acceptable in term of area and power consumption. With those values the dead time is 512 *μs*, a factor of two below the requirement.

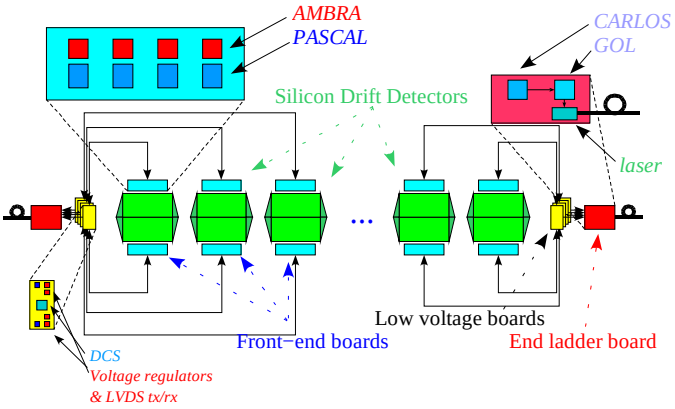

Figure 1 : SDD readout scheme

A schematic view of the readout architecture is shown in Figure 1.

In order to further decrease the number of cables from the front end system a digital multi−event buffer is placed close to the front−end chip. The data from the A/D converter are first quickly stored into a digital event buffer over a wide bus and then sent outside the detector area over a single 8−bit bus for each front−end board.

The introduction of the event buffers introduces an additional dead time; however, it has been calculated that with 4 buffers the dead time due to event buffer overflow is only 0.04%.

II. The front−end ASICs

The front−end system is based on two ASICs, named PASCAL and AMBRA.

PASCAL can be divided in three parts : 64 preamplification and fast analogue storage channels, 32 successive approximation A/D converters (each ADC is shared between two analogue memory channels) and a logic control unit that provides the basic control signals for the analogue memory and the converter.

The present prototype is half sized : 32 input channels with preamplifier and 256 cells analogue memory are connected to 16 A/D converters. A scheme of the prototype is shown in Figure 2.

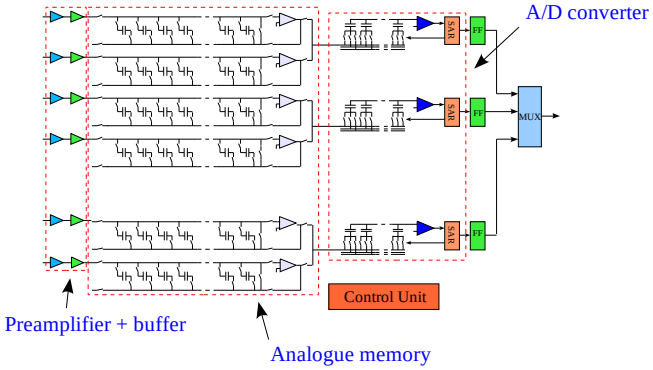

Figure 2 : PASCAL scheme

The preamplifier is based on the standard charge amplifier plus shaper configuration and provides a gain of around 35 *mV/fC* with a peaking time of 40 *ns*. The preamplifier is DC coupled with the detector; baseline variations and detector leakage currents are compensated via a low frequency feedback around the second stage. The amplifier is buffered with a class−AB output stage in order to be able to drive the analogue memory with a low power consumption.[3]

The analogue memory is an array of 256x32 switched capacitor cells controlled via a shift register. The cells can be written at 40 *MHz* and read out at 2 *MHz*. The architecture is such that the voltage across the capacitor (and not the charge) is written and read; therefore the sensitivity to the absolute value of the capacitors and to the timing is greatly reduced.[5]

The 10−bit A/D converter is based on the successive approximation principle; a scaled array of switched capacitors provides both the DAC and the subtraction functions, and a three−stage offset compensated comparator is used to check if the switched capacitor array output is positive or negative and to drive the successive approximation register that, in turn, controls the DAC. The successive approximation architecture is a good compromise between speed and low power consumption; it requires no operational amplifiers and only one zero crossing comparator. The conversion speed is one clock cycle per bit.[6]

Two calibration lines, connected to the even and odd channel inputs via a 180 *fF* capacitor, provide the capability of testing the circuit without the detector.

The prototype has been designed in a commercial 0.25 *µm* CMOS technology with radiation tolerant layout techniques. The chip size is 7x6 mm^2.

AMBRA provides 4 level of event buffering. Each buffer has a size of 16 *kbytes* and is based on static RAM in order to increase the SEU resistance and to avoid the refresh circuitry. The control unit provides buffer management, controls the operations of PASCAL and provides the front−end interface to the rest of the system. The present prototype has only 2 event buffers and can work up to 50 *MHz*. [4]

The prototype has been designed in Alcatel 0.35 *µm* technology with standard layout. The chip size is 4.4x3.8 mm^2. 89% of the core area is occupied by the two memory buffers.

The PASCAL−AMBRA system operates as follows : when AMBRA receveis the *trigger* signal it sends an *SoP* (Start of oPeration) command to PASCAL. PASCAL stops the sampling of the detector outputs and starts the readout of the analogue memory and the A/D conversion. When the first sample of the 32 channels has been converted, a *write_req* (write request) signal is sent to AMBRA which in turn, if a buffer is available, replies with a *write_ack* (write acknowledge) and starts the data acquisition. The sequence continues for the other samples of the analogue memory until AMBRA sends an *EoP* (End of oPeration) command, then PASCAL returns to the acquisition phase. The *EoP* command can be issued for two reasons : all the 256 cells have been readout, or an *abort* signal has been received. The latter indicates that the trigger signal, which is generated from the level−0 ALICE trigger, has not been confirmed by the higher level triggers. Since the reject probability can be very high (it can reach 99.8% in Pb−Pb interactions) it is very important to stop as soon as possible the conversion and restart the acquisition.

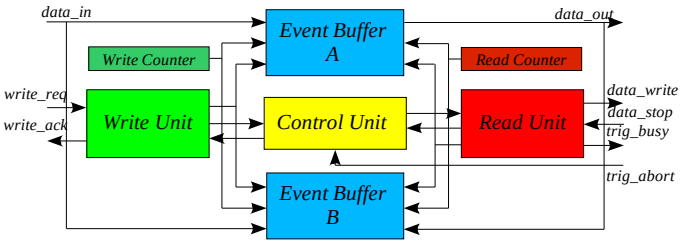

Figure 3 : AMBRA scheme

As soon as an event buffer is full, AMBRA starts the transmission of the data. The *data_write* command is used to indicate that there are valid data on the output bus. This signal remains high as long as the data are transmitted. A *data_end* signal remains high for one clock cycle in correspondance of the last byte. It is possible to suspend the data transmission via the *data_stop* command.

III. Test results of the front−end circuit

The two prototypes have been evaluated together on a test board.

The inputs have been provided via the calibration lines while the outputs have been readout via a logic state analyzer. A data pattern generator has been used to provide the clock and the other digital control signals to the two chips.

The two prototypes have also been tested connected to a detector in a test beam at CERN PS. Data analysis is in a preliminary stage; therefore in this paper we discuss only the lab measurement performed on the system.

Figure 4 shows a typical output from a 4 *fC* charge signal from the calibration lines. Even with a δ−like pulse at least 4 samples are significantly above the noise in the time direction. For a particle crossing the detector far from the anodes a slower signal is obtained and more samples can be above the noise floor; on the other hand, since the total charge does not change, the signal to noise ratio on the individual sample is worse.

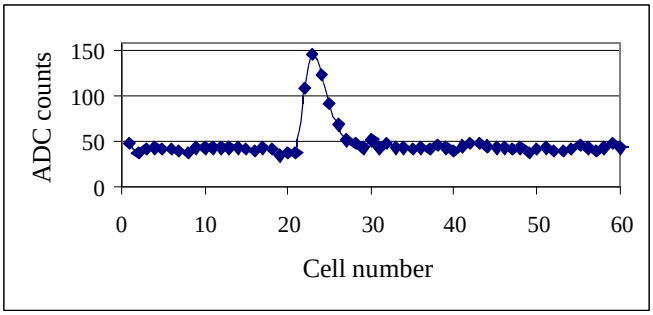

Figure 4 : Typical output from a 4 fC input signal

Figure 5 shows the output code against the input charge for the 32 channels of a chip. It can be seen that the dynamic range is well above the required 32 *fC*.

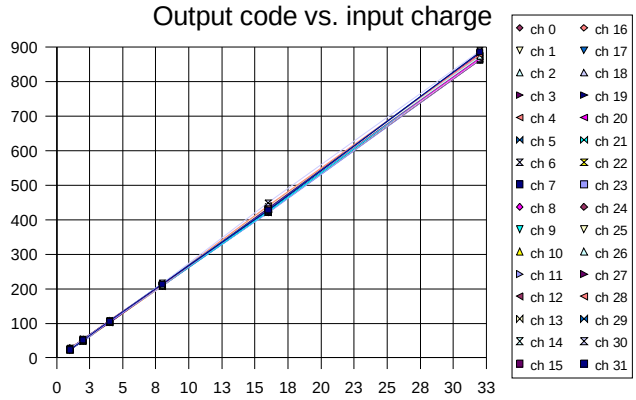

Figure 5 : Dynamic range

Figure 6 shows the deviation of the curve of Figure 5 from linear fit. The non−linearity is less than 0.8% over the whole dynamic range and it is mainly related to the saturation of the preamplifier at the highest part of the range. Another source of non−linearity is the voltage dependance of the memory capacitors, again in the highest part of the range.

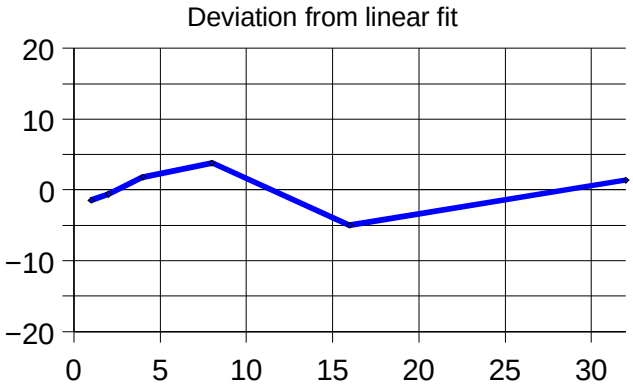

Figure 6 : Linearity

Figure 7 shows the gain variation across channels of 5 different chips. The number of tested chip is too small to have a significant statistic; however, from these results the variation between channels of the same chip is of the order of few percent while the chip to chip variation is of the order of 10−15%.

A small slope of the gain distribution across the channels of the same chip can be identified. This slope is due to a voltage drop on the power and reference lines across the chip. With a proper sizing of these critical lines it will be probably possible to recover some of the gain variation in the final version of the chip.

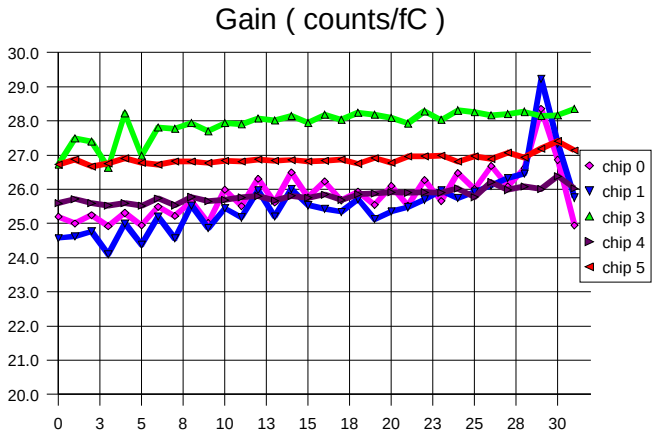

Figure 7 : Gain

Noise measurements give an rms noise below 2 counts, which corresponds to around 400 e^-. This number is slightly above the requirements and comes essentially from the coupling between the analogue part and the digital one at the substrate level and/or at the board level (the measured noise of the preamplifier alone is less that 180 e^-). A better grounding scheme is under study for the final version of the chip and for the final board design.

The measurements give less than 5 and around 10 *mW* per channel for average and peak power consumption,

respectively. These numbers fulfill the ALICE SDD requirements.

Another important aspect is the amplifier recovery time from saturation. In the ALICE environment very high signals (up to 400 *fC*) are possible. Despite these signals are not of concern for the data analysis, it is important that the preamplifier does not remain "hanged" for milliseconds. Tests show a recovery time of 350 *ns* for a 100 *fC* signal. This time rises with higher signals and saturates at 500 *ns* for signals above 200 *fC*. These very high signals are very rare, therefore this recovery time is acceptable.

IV. Radiation tolerance and technology issues

The drift detectors and the front−end electronics in the ALICE environment will have to survive to a quite low, but not negligible, level of radiation. The foreseen dose for 10 years of operation is around 20 *krds*. This value is at the limit of what a modern standard technology can accept, therefore the choice between a standard and a radiation hard technology was not straightforward.

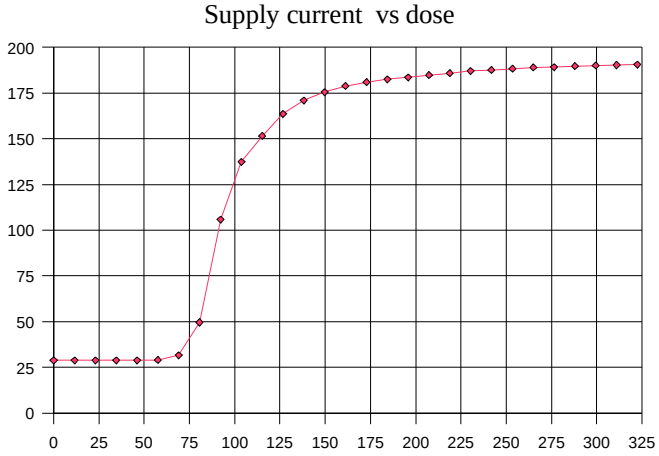

Figure 8 : AMBRA irradiation test results : supply current (mA) vs dose (krds)

While radiation hard technologies remain two or three generation behind the standard technologies, a new approach based on specific layout techniques and deep submicron standard technologies has been carried out by the RD49 research program at CERN. The effectivness of this approach has been demostrated up to 30 *Mrds*. Its main disadvantage is some area penalty, expecially in the digital design, if compared with a standard deep submicron technology. However, the digital radiation tolerant cells are still smaller when compared with the standard cells of a radiation hard processes.

Owing to the low radiation level in ALICE the first PASCAL prototype has been designed in a commercial 0.25 *µm* with radiation tolerant techniques while the first AMBRA has been designed in Alcatel 0.35 *µm* technology with the commercial standard cell library.

The reason of this choice was that, on one side, analogue circuits are more sensitive to leakage currents and threshold variation (expecially the analogue memory, where leakage currents would destroy the cells content) while, on the other hand, digital circuits are more robust but the area penalty due to the radiation tolerant techniques is much more significant.

Radiation tests for total dose effects have shown very small variations in the parameters of the PASCAL chip up to 30 *Mrds*. The irradiated AMBRA chips show full functionality up to 1 *Mrd*; unfortunately the leakage current shows a dramatic increase at 50−60 *krds* (Figure 8) and, despite this effect does not affect the chip functionality, it will lead to an unacceptable power consumption.

For this and other reasons (cost, phasing out of the 0.35 *µm* process by Alcatel) the final version of the AMBRA chip will use the 0.25 *µm* technology radiation tolerant standard cells library.

V. Conclusions

A 32 channels prototype and a 2 event−buffer prototype of the two ASICs for the readout of the ALICE SDDs have been designed and tested. The 2−chip system shows an excellent linearity and a good gain uniformity. The system fulfills the ALICE requirements and shows the effectivness of the chosen architecture.

A minor problem related to voltage drop in the internal power supply and reference lines has been identified and will be corrected in the final version. Owing to the fact that the threshold for the leakage current in the 0.35 *µm* process used for AMBRA is too close to the foreseen radiation level, the final version of both chips will be designed using the radiation tolerant approach.

VI. References

[1] ALICE Technical Design Report, CERN/LHCC 99−12

[2] ALICE Technical Proposal, CERN/LHCC 95−71

[3] A.Rivetti et al, "A mixed−signal ASIC for the silicon drift detectors of the ALICE experiment in a 0.25 µm CMOS" CERN−2000−010, CERN−LHCC−2000−041, pp. 142−146

[4] G.Mazza et al, "Test Results of the ALICE SDD Electronic Readout Prototypes", CERN−2000−010, CERN−LHCC−2000−041, pp. 147−151,

[5] G.Anelli et al., "A Large Dynamic Range Radiation−Tolerant Analog Memory in a Quarter−Micron CMOS Technology", *IEEE Trans. on Nucl. Sci.*, vol.48, pp. 435−439, Jun 2001

[6] A.Rivetti et al., "A Low−Power 10 bit ADC in a 0.25 µm CMOS: Design Consideration and Test Results", presented at *Nucl. Sc. Symposium and Med. Imaging Conference*, Lyon, Oct 2000