A Large Dynamic Range Radiation-Tolerant Analog Memory in a Quarter-Micron CMOS Technology

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Abstract—An analog memory prototype containing 8∗128 cells has been designed in a commercial quarter-micron CMOS process. The aim of this work is to investigate the possibility of designing large dynamic range mixed-mode switched capacitor circuits for high-energy physics (HEP) applications in deep submicron CMOS technologies. Special layout techniques have been used to make the circuit radiation tolerant. The memory cells employ gate-oxide capacitors for storage, permitting a very high density. A voltage write-voltage read architecture has been chosen to minimize the sensitivity to absolute capacitor values. The measured input voltage range is 2.3 V (the power supply voltage V_{DD} is equal to 2.5 V), with a linearity of almost 8 bits over 2 V. The dynamic range is more than 11 bits. The pedestal variation is ± 0.5 mV peak-to-peak. The noise measured, which is dominated by the noise of the measurement setup, is around 0.8 mV rms. The characteristics of the memory have been measured before irradiation and after 100 kGy (SiO_2), and they do not degrade after irradiation.

Index Terms—Analog memories, deep submicron CMOS, radiation hardening, switched capacitor circuits.

I. INTRODUCTION

DEEP submicron CMOS technologies are good candidates to implement radiation tolerant application-specific integrated circuits (ASICs) due to their thin gate oxides. Special layout techniques can be used to solve the remaining radiation-related problems such as leakage current inside a transistor and between transistors [1], [2]. On the other hand, thin gate oxide technologies have a reduced power supply voltage compared to their less advanced counterparts, and this can make it more difficult to implement some circuit architectures. Moreover, deep submicron CMOS technologies do not always offer all kinds of devices which are useful for analog design.

An analog memory has been designed because this circuit topology contains many examples of the previously mentioned problems and because it is a circuit often used in the ICs for HEP experiments. The circuit contains capacitors and switches, and therefore we dealt with the problem of implementing high-density capacitors with acceptable C–V characteristics and having switches with a reasonably high conductance over the entire input voltage swing. Since the power supply voltage V_{DD} is equal to 2.5 V for this 0.25 μm technology, it is also interesting to investigate what is the maximum dynamic range attainable.

Last but not least, the circuit also contains some digital circuitry, allowing the study of the problems related to substrate noise in mixed mode ICs.

II. CIRCUIT DESCRIPTION

In this section we present the main features of the capacitors and switches used in the memory, and we describe the schematic and layout of the circuit.

A. Capacitors in Submicron CMOS Processes

There has always been a strong interest in the design of analog–digital systems on a single chip [3]–[6]. Since the IC market has been driven in the last 20 years by memories, microprocessors, and in general by digital ICs, digital CMOS processes offer the most advanced characteristics and are the least expensive. On the other hand these low-cost processes do not have, at least in their early stages, many devices which are useful for the analog designer. Among them, there is in deep submicron CMOS processes a lack of high-density high-quality capacitors, where high-quality means uniformity, low voltage coefficient, and low temperature coefficient. Dense high-quality capacitors are generally implemented as double-polysilicon capacitors [7], but this requires extra processing (i.e., implies extra costs).

An alternative, which is generally available in any CMOS process, is to use metal-to-metal capacitors. These capacitors have good characteristics but offer a rather low specific capacitance (generally less than 1 fF/μm^2 in present processes).

For applications where an intensive use of capacitors is necessary (e.g., switched capacitor circuits, analog memories etc.), one could exploit the high specific capacitance of the thin gate oxide of the transistors. In a 0.25 μm technology with a physical gate oxide thickness of around 5 nm, the specific capacitance is around 5.5 fF/μm^2. This value is lower than the one expected from the formula $C_{ox} = \varepsilon_{SiO_2}/t_{ox}$, where C_{ox} is the capacitance per unit area, ε_{SiO_2} is the silicon dioxide permittivity, and t_{ox} is the effective oxide thickness. This is due to the polysilicon-gate depletion effect [8], [9], which results in an effective oxide thickness greater than the physical oxide thickness. Besides the high specific capacitance, MOS capacitors offer other advantages such as no extra costs and good matching [10], [11]. On the other hand, these capacitors present a nonlinear behavior, as the capacitance is strongly dependent on the dc bias condition. This problem can be overcome in some applications with special techniques, as shown for example in [6].

Fig. 1 shows four possible MOS capacitor structures which can be implemented in an n-well CMOS process [12]. To have
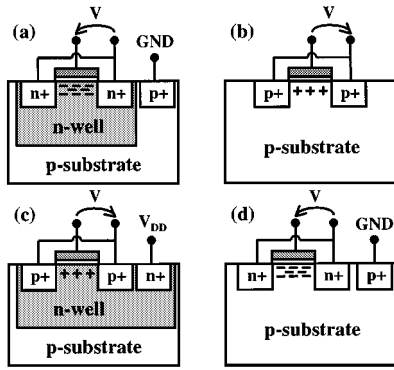
Fig. 1. Possible MOS capacitor structures in an n-well CMOS technology. The polarity that should be used is indicated in the pictures.
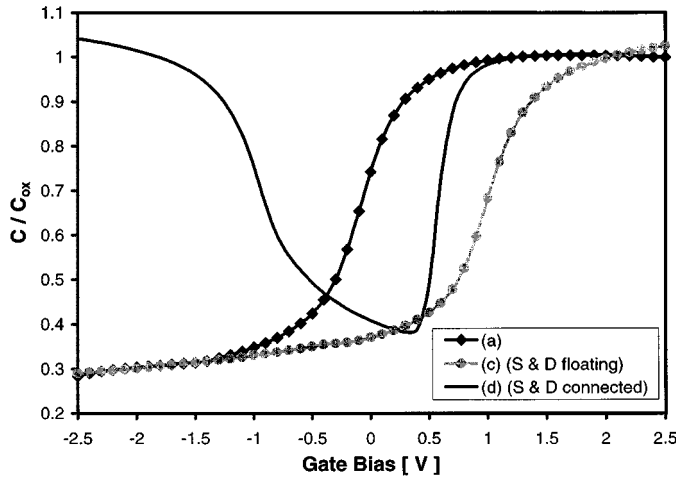

Fig. 2. Gate capacitance (normalized to the oxide capacitance) as a function of the gate bias voltage. The curves correspond to the structures indicated in Fig. 1.

Fig. 3. (a) Sample and hold, made by a CMOS switch and a capacitor. (b) Conductance of the switch (in the "on" state) as a function of the input voltage when the power supply voltage is 5 V. In this case, one of the two transistors of the switch is always on. The situation in the case of a too small power supply voltage is depicted in (c).

the best performance (i.e., little dependence of the capacitor value on the bias), the capacitors (a) and (b) should work in accumulation and (c) and (d), which are respectively like a p-channel and a n-channel transistor, in strong inversion. The capacitor (b) has the bottom plate ac-grounded. The capacitor (c) can be shielded from substrate noise by applying a fixed bias to the n-well. We have only implemented structures (a), (c), and (d), since (b) has the limitation of having the bottom plate grounded.

The C–V characteristics (Fig. 2) were measured with a HP4284A Precision LCR Meter at a frequency of 100 kHz. The curves of Fig. 2, labeled with the letters (a), (c), and (d), represent the measurements of the corresponding structures of Fig. 1. The curve (d) shows the case of an n-channel transistor, as shown in Fig. 1(d). The strong inversion region is on the right part of the plot, and the capacitance value is stable for bias voltages higher than about 1 V. Similar results were found for p-channel transistors, i.e., the structure (c) in Fig. 1. The curve (a) is the characteristic of the structure made as an n-channel transistor in an n-well.

The technology used has double-flavor polysilicon gates (n+ doped polysilicon for n-channel transistors and p+ for p-channel). In structure (a) the gate is strongly n+ doped as for the n-channel transistor, which allows us to have a wider flat
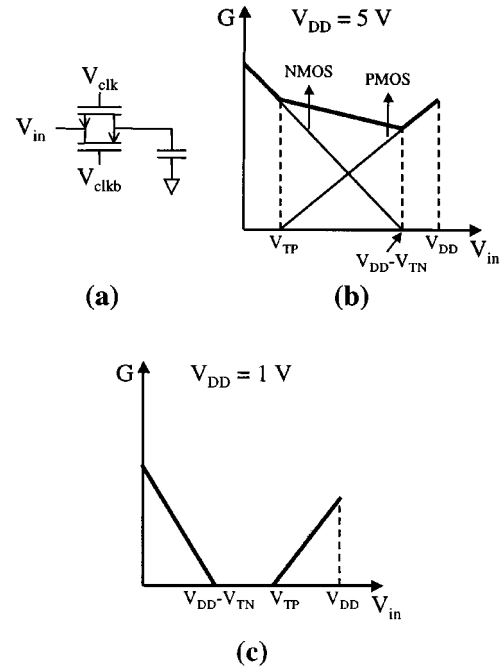
part in the C–V characteristic. The C–V characteristic of capacitor (c) is reported in Fig. 2 not to make a comparison: in this case we should have plotted its C–V characteristic, measured with the source and drain connected, flipped horizontally, and we would have obtained a curve coincident with (d). Curve (c) has been plotted to show the difference in the flat-band voltages (equal to $E_g/q \approx 1.1$ V) of the two structures in accumulation but with the different doping of the polysilicon gate.

From Fig. 2 we can see that the capacitor which shows the widest flat region is the N+ poly-n-well capacitor (a). The two other structures have a smaller flat region and, even more important for some applications, have a dramatic decrease (nearly a factor of three) of the capacitance reducing the gate voltage from 1 to 0 V. The capacitor (a) has a decrease of its value from 1 to 0 V of "only" 25%.

B. Switch "On" Conductance

A transistor in the linear region can be used as a switch. To be able to transmit signals from 0 V to V_{DD}, an n-channel and a p-channel transistor can be used in parallel [Fig. 3(a)]. In this way, if $V_{DD} > V_{Tn} + |V_{Tp}|$, the switch is able to conduct all the voltages from 0 V to V_{DD}. Fig. 3(a) shows an example of a CMOS switch used in a sample and hold. The switch conductance (when the switch is on, i.e., $V_{clk} = V_{DD}$ and $V_{clkb} = 0$ V) is also shown as a function of the signal we want to sample on the capacitor, for two V_{DD} values. In the first case [Fig. 3(b)], the conductance of the switch G (which is the sum of the conductances of the two transistors, G_n and G_p) stays above a certain level for all the possible values of the input signal V_{in}. In the second case [$V_{DD} < V_{Tn} + |V_{Tp}|$, Fig. 3(c)], even when the switch is biased on, we have a gap in its conductance.
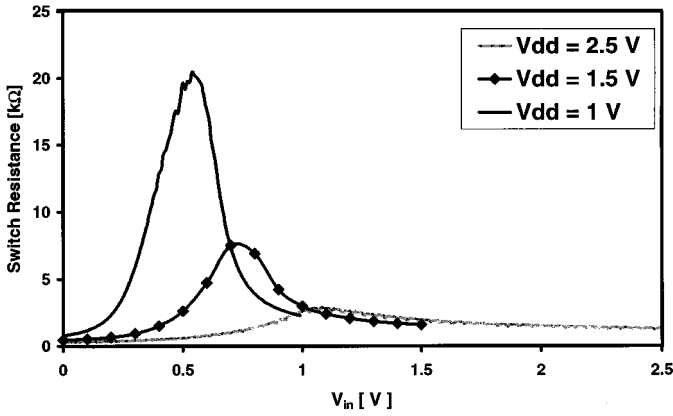
Fig. 4. Resistance of a CMOS switch in the "on" state as a function of the signal to be transmitted through the switch (V_{in}). The substrate bias is 0 V, the well bias is V_{DD}. The three curves show measurements done with three different values of V_{DD}.

Fig. 5. Analog memory channel schematic.

To measure the "on" state resistance of the switches used in the analog memory, we laid out a CMOS switch made with two minimum-sized Enclosed Layout Transistors (ELTs) [1]. Also the p-channel transistor was designed enclosed (i.e., identical to the n-channel) to have better clock feedthrough cancellation and less charge injection. The "on" state resistance of the switch as a function of the input voltage for three different power supply voltages is shown in Fig. 4.

Biasing the switch at the nominal power supply voltage of the technology used (2.5 V), it can be seen that the maximum resistance is below 3 kΩ. The value of the resistance is important because, for a given storage capacitance, it limits the maximum speed which can be used writing to the memory. Since we want to write to the memory at a speed of 40 MHz, the RC constant of the switch has to be significantly smaller than 25 ns. In the memory we have used 600 fF capacitors, so the maximum RC constant will be 1.8 ns, which meets the requirements perfectly. Fig. 4 also shows how fast the maximum resistance of the switch grows as the power supply voltage is reduced. This will create problems scaling down a technology, and new switch architectures will have to be studied to implement switched capacitor circuits. The last observation from Fig. 4 is that the shape of the curves is quite different from what one could expect by taking the inverse of the conductance plotted in Fig. 3. This is due to the body effect. The substrate is connected to ground and the well of the p-channel transistors to V_{DD}, and therefore the threshold voltages of both the n-channel and the p-channel transistors depend on the signal to be written, making the plots of Fig. 4 nonlinear.

Once the input signal is sampled on the capacitor and the switch is open, the charge representing the information does not stay on the capacitor indefinitely, due to the switch leakage current which degrades the information. The leakage current is made up by two components: one is the subthreshold current and the other is the leakage associated with the junctions of the transistors of the switch. To minimize this leakage, minimum-sized transistors are generally used. CMOS switches are better than single transistors switches, since the two junction leakages of the two devices tend to compensate for each other. The subthreshold leakage component can be increased by ionizing radiation; therefore, ELTs must be used.
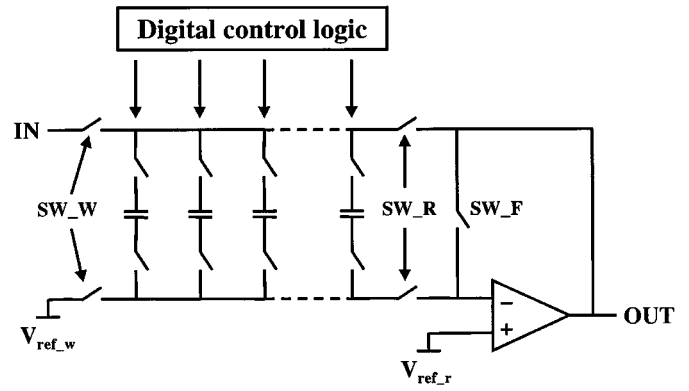
C. Memory Description

The architecture chosen for the memory is shown in Fig. 5 [13]. Several alternative solutions have been explored, for example, in [14], but we think that the one described here is the best to achieve a high dynamic range with the limited power supply voltage available in a deep submicron process. A voltage write–voltage read architecture has been chosen, to minimize the sensitivity to the capacitor value. The circuit works as follows: during the write cycle the switches SW_W are closed and connect the common lines to the input signal. The switches SW_R are open and the switch SW_F is closed. The digital control logic closes the switches of each cell, one cell after the other, to sample the input signal on the capacitors (write cycle). The values stored can be read (read cycle) opening the switches SW_W and SW_F, closing the switches SW_R, and connecting the cells one after the other in the amplifier feedback loop. The switch SW_F is closed at the end of the reading of each capacitor to discharge it and to reset the read amplifier. Two switches for each cell have been used to connect the capacitors to the common lines, in order to have a more symmetric charge injection. The switches connecting the bottom plates of the capacitors to the reference line are also there to avoid charging the read amplifier with all the parasitic capacitances associated with the bottom plates.

In order to avoid charge sharing between adjacent cells, it is very important to have no overlap between the signals driving two consecutive cells. This has been achieved by putting between the output of each flip–flop of the shift register of the digital control logic and the corresponding cell a series of inverters with one of them controlled by a low biasing current. This allows the delay of the rising edge of each flip–flop output, and in this way the rising edge of the flip–flop number n will be delayed compared to the falling edge of the flip–flop number $n-1$. The delay can be adjusted by changing the current in the controlled inverter.

The read amplifier has been implemented as a simple operational transconductance amplifier with a Miller compensation capacitor. The power consumption is around 3.6 mW, and the output response to an input step of 1 V has a rise time of 32 ns with a capacitive load of 20 pF (which could be, for example, the input capacitance of an ADC which has to be driven by the memory read amplifier).

The layout of a single memory cell occupies $11.1 \times 56.1 \ \mu m$, the switches are CMOS and are laid out with ELTs and guard rings in order to prevent post-irradiation leakage currents. The capacitor, which has a value of 600 fF, is laid out as an n-channel transistor in an n-well. The chosen value of the capacitor is a tradeoff between speed and accuracy. It cannot be too large, to limit the time necessary to write to it. On the other hand, it cannot be too small, otherwise the leakage current would quickly degrade the information. The layout of the cell is symmetric with respect to a horizontal as well as a vertical axis passing through the center of the cell. The clock lines, which pass over the cell, are made in the third level of metal (the furthest from the substrate) and carry opposite signals, so they do not disturb the top plate of the capacitor. Additionally, a metal-2 plate has been put between the clock lines and the capacitors to provide some shielding.

We have designed a prototype chip composed of eight memory channels, each one made by 128 cells and the read amplifier, and the digital control logic, whose main part is the shift register. The memory cell is very narrow (11.1 μm), and this means that 128 cells can fit in less than 1.5 mm. Attention has been paid to keeping the digital circuitry separate as much as possible from the analog parts, to reduce the substrate noise [15]. In the chip we kept separate the analog ground and V_{DD} (GND and VDD) from the digital ground and V_{DD} (GNDD and VDDD). In the digital circuitry, all the n-channel sources have been connected to GNDD, while the substrate contacts have been connected to a separate GND, to avoid injecting high switching currents into the substrate. To prevent crosstalk between channels, each channel is surrounded by a guard ring, and between one channel and the other there is a space of 50 μm. This space is anyhow required to match the bonding pad pitch.

III. MEASUREMENT RESULTS

The measurement setup is composed of an HP1663EP Logic Analyzer and Data Pattern Generator, a Tektronix TDS540 Digital Oscilloscope, a test board and the necessary power supplies and waveform generator. This setup offers a great flexibility in changing the digital patterns sent to the memory and testing quickly the functionality of different chips (chips are packaged in LCC40 chip carriers which fit in the socket of the board and which can be easily changed). The drawbacks of the setup are that it is limited to the 8-bit precision of the Digital Oscilloscope and that the noise introduced by the board does not allow the measurement of the intrinsic noise of the memory.

To characterize the performance of the analog memory we measured the linearity of the input–output characteristic, the dynamic range, the pedestal uniformity, the noise, the power consumption (analog and digital), and the crosstalk between channels. The measurements were done writing at frequencies up to 100 MHz and reading at frequencies of a few megaHertz. The measurements presented here were done writing at 50 MHz and reading at 2 MHz.

A. Preirradiation

The input–output characteristics measured on one cell of the analog memory start to deviate considerably from a straight line
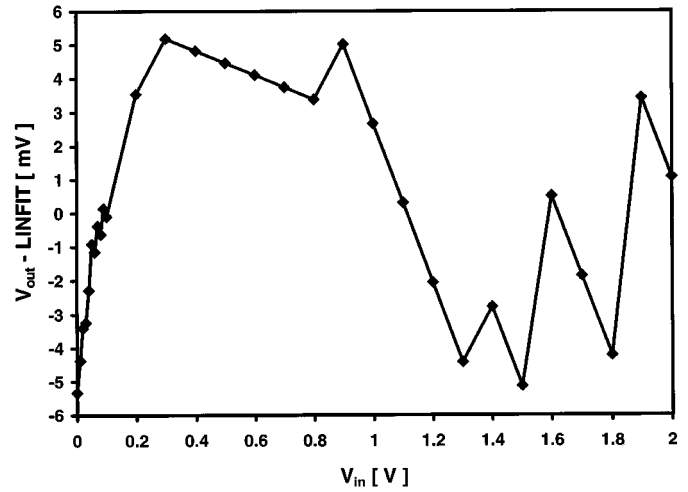

Fig. 6.   Deviation of the input–output characteristic from its linear fit.

for input values higher than 2 V, since the output voltage of the read amplifier starts to saturate. Fitting with a straight line the characteristics and extracting the slope of the fit we find the dc gain, which is always very close to one (around 0.97). Fig. 6, shows the deviation of the input–output characteristic from its linear fit. It is interesting to note that the deviation varies from its minimum to its maximum for an input signal varying from 0 to 0.5 V. This is related to the change in the capacitor value when writing signals in that range (see Fig. 2). The values plotted for $V_{\rm in} > 1.3$ V are clearly affected by the 8-bit precision of the oscilloscope.

Defining the linearity as the ratio of the input voltage range (2 V in our case) and the double of the maximum deviation of Fig. 6 we find values (expressed in equivalent number of bits) close to 8 bits, which is actually the resolution of our measurement setup.

The dynamic range is defined as the ratio of the input voltage range to the minimum detectable signal [14], which can be considered equal to the input referred rms noise voltage. From our measurements, values of a dynamic range between 11 and 12 bits are found.

We have measured the output of all the cells of a memory channel and repeated the measurement for several channels. An example is given in Fig. 7. The pedestal variation is ± 0.5 mV. This variation can be seen as a source of noise, and the rms noise value can be calculated with the formula

$$\overline{v}_{\rm rms} = \frac{\sqrt{\displaystyle\sum_{1}^{M}(V_{\rm oi} - V_{\rm avg})^2}}{\sqrt{M-1}} \qquad (1)$$

where M is the number of cells. Applying (1) to the measurements we found values between 180 and 220 μV rms. These numbers indicate that the memory cells are extremely uniform.

The noise of each cell has been measured to be around 0.8 mV rms. As already mentioned earlier, we cannot measure the noise of the memory itself due to the noise introduced by the measurement setup, which determines the measured value 0.8 mV rms. In fact, the expected noise is a lot less than the one measured.
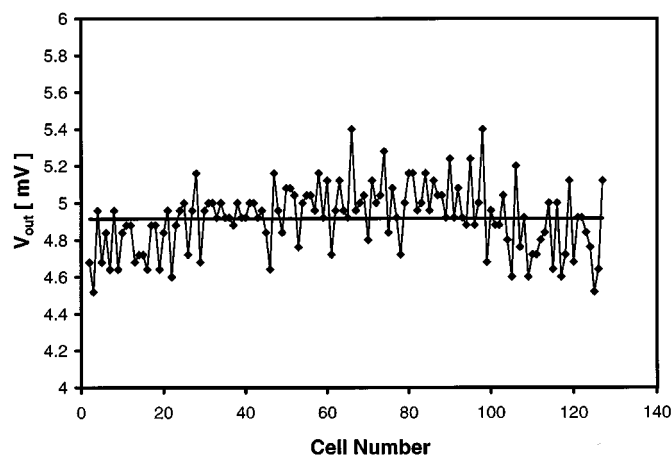
Fig. 7. Pedestal variation from cell to cell. The measurements were done with $V_{\text{ref}_r} = V_{\text{ref}_w} = 100$ mV. The horizontal line shows the average value.

The main sources of noise are the kT/C noise of the sampling capacitor and the noise of the read amplifier (we neglect here the noise at the input, which comes from the 50-Ω input resistance.). These two sources should account, respectively, for 80 μ and about 100 μV rms. The quadratic sum of these two values is a lot smaller than the measured value.

We did not observe any crosstalk between channels, which means that the precautions taken doing the layout (guard rings around each channel and 50-μm space between channels) are effective.

B. After Irradiation

To test the radiation tolerance of the analog memory we have used 10-keV X-rays. We irradiated the chip up to a total dose of 100 kGy (SiO_2) with a dose rate of 316 Gy/min. During irradiation the chip was biased and clocked with a dc input signal of 1.5 V. The irradiation affected neither the dynamic range nor the pedestal variation. Also the noise remained unchanged. Both the analog and the digital power consumption decrease by only a few percent after irradiation. This decrease is due to the increase (in absolute value) of the threshold voltages of both the n-channel and the p-channel transistors.

IV. CONCLUSIONS

The outcome of this study allows us to draw the following conclusions.

- The very dense capacitors available in the quarter-micron process under study can be used, with some precautions, for implementing switched capacitor circuits.
- A 2.5 V supply voltage is enough to drive efficiently CMOS switches and allows large dynamic ranges.

- The presence of digital circuitry on the chip does not affect its analog performance, showing the effectiveness of the precautions taken.
- The radiation-tolerant approach used is effective in achieving multi-Mrad radiation tolerance.

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