

An 80Mbit/s radiation tolerant Optical Receiver for the CMS digital optical link

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ABSTRACT

The CMS tracker slow control system will use approximately 1000 digital optical links for the transmission of timing, trigger and control signals. In this system, the 80Mbit/s optical receiver at the detector end of each optical link has to be radiation hard since it will operate in the severe radiation environment of the CMS tracker (10 Mrad in 10 years). We have developed a prototype circuit in a 0.25 μm commercial CMOS process using radiation tolerant layout practices to achieve the required radiation tolerance. This effective technique consists in the systematic use of enclosed (edgeless) NMOS transistors and guardrings, and relies in the natural total dose hardness of the thin gate oxide of deep submicron processes. The circuit features an Automatic Gain Control (AGC) loop allowing detection of wide dynamic range input signals (-20 to -3 dBm) with minimum noise, compatible with the maximum expected radiation-induced drop in quantum efficiency of the PIN photodiode. A second feedback loop compensates a photodiode leakage current up to 100 μA , and the circuit outputs an LVDS signal. Four receiver channels were integrated in a 2x2mm² chip, out of which two were simultaneously bonded to two PIN photodiodes, and their Bit Error Rate (BER) performance was measured before and after an irradiation with 10 keV X-rays up to 20 Mrad(SiO₂).

1. INTRODUCTION

Particle physics experiments at the Large Hadron Collider (LHC), the new accelerator presently in construction at the European Centre for Nuclear Research (CERN), will need radiation tolerant microelectronic circuits. Sophisticated mixed analog-digital integrated circuits will operate close to the vertex and tracking detectors in the inner region of the experiments. In the case of CMS and ATLAS, the two biggest LHC experiments, the total dose requirements approach and sometimes exceed 10 Mrad.

The CMS tracker control system will use approximately 1000 digital optical links for the transmission of timing, trigger and control signals [1]. These digital signals, transmitted serially at a bitrate of 40 Mbit/s (80 Mbit/s for the clock signal), will be converted into electrical signals by a PIN photodiode at the receiver end. One of the transmission channel ends will sit inside the detector, in the radiation environment of the CMS tracker: its components need therefore to be radiation hard.

The front-end element of the optical receiver is a transimpedance amplifier, which has to amplify the photocurrent delivered by the PIN diode and detect the presence of a reset signal. In the CMS control system, the PIN diode is a commercial component and its performance will be affected by radiation. To compensate for the radiation-induced degradation of the photodiode quantum efficiency, the amplifier should have a wide dynamic range (-20 to -3 dBm input signal modulation amplitude). Moreover, it should be able to compensate a photodiode leakage current of up to 100 μA . Since no commercial amplifier satisfying all these conditions and able to survive the required level of radiation exists, the development of an ASIC was necessary. To meet all the specifications, a commercial 0.25 μm CMOS technology has been chosen for the development of the amplifier. This advanced technology allows to easily meet the speed requirements with minimum power consumption: the bandwidth of 80 MHz can be achieved without large currents, resulting in a power consumption below 25 mW per channel at the nominal voltage of 2.5 V.

This paper describes the approach followed to meet the radiation tolerance requirements of the receiver, the choices that have been made for the circuit architecture and the results obtained on the first prototype of the circuit.

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2. RADIATION TOLERANT DESIGN APPROACH

Irradiation measurements on MOS capacitors performed in the early 80's showed a significant decrease of the radiation induced oxide trapped charge and interface states for oxides thinner than about 10 nm [2]. Since gate oxides in present day submicron CMOS technologies are in this range, they are becoming increasingly radiation tolerant. This has been confirmed on commercial-grade CMOS processes in several works [3, 4].

Ionising radiation can nevertheless induce positive charge trapping in the still thick field and lateral oxides of modern CMOS technologies, opening up leakage current paths that can lead to device failure after a moderate level of total dose, of the order of 10-40 krad. The leakage paths can open at the edge of the NMOS transistors (source to drain leakage current) or between adjacent n+ diffusions (transistor to transistor, transistor to n-well, ...). A smart layout technique based on the use of enclosed (edgeless) NMOS transistors and of guardrings can prevent both sources of leakage, and has been demonstrated on simple devices and complex mixed-signal circuits up to multi-Mrad total dose levels [5]. Additionally, the use of guardrings is an effective tool to decrease the sensitivity to Single Event Latchup (SEL) [6], and no such destructive event has ever been observed on simple test structures [7] and, more recently, on a variety of mixed-signal circuits during heavy ions irradiation. All these circuits were designed using this layout technique in a quarter micron process.

The use of this design approach allows the use of modern CMOS technologies in a radiation environment. This gives the opportunity to profit from all the advantages of these technologies: speed, reduced power consumption, high level of integration, high volume production (and consequently low cost) and high yield.

To assist designers in the development of complex circuits for LHC, we have implemented a radiation tolerant digital standard cell library on a commercial deep submicron CMOS technology. All the cells systematically use the radiation tolerant layout technique described above. Moreover, we have studied a model for the effective size of enclosed transistors, and implemented it in the design CAD extraction tools. The optical receiver has been designed using these tools, but only a couple of cells from the library have been employed in the almost full analog architecture of the IC.

3. CIRCUIT DESCRIPTION AND IMPLEMENTATION

The global architecture of the optical receiver is shown in Figure 1. The PIN diode is connected to the receiver circuit, which is mainly composed of four blocks: a transresistance preamplifier, a chain of limiting gain amplifiers, an LVDS driver and a block to detect and generate the reset signal.

The PIN diode is DC coupled to the preamplifier, which also supplies the bias voltage to the photodiode (about 1.8 V). This solution also allows for an easy integration of a feedback loop to sink the radiation-induced leakage current of the photodiode.

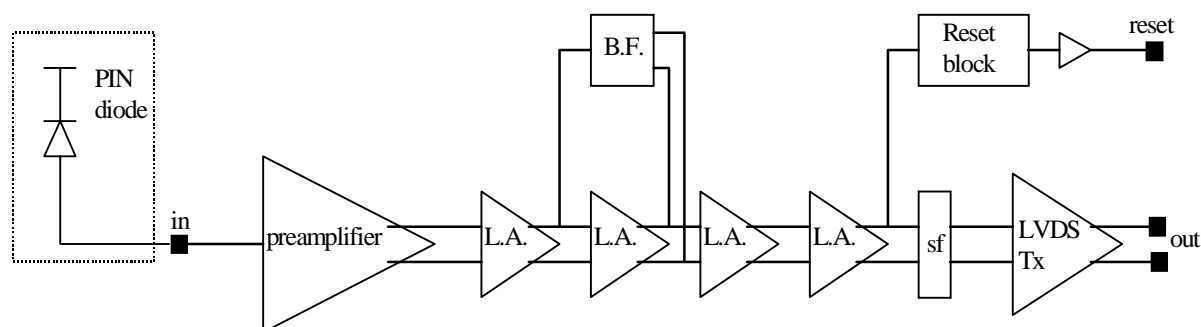


Figure 1: Global architecture of the receiver circuit, DC connected to the external PIN diode. The transresistance preamplifier is followed by a chain of limiting amplifiers (L.A.), where a Balancing Feedback (B.F.) block ensures that the average of the two differential signals is identical.

3.1. The transresistance preamplifier

The architecture of the preamplifier is shown in Figure 2. The transresistance amplifier transforms the current signal from the PIN diode into a voltage signal, with a variable transresistance. This sort of Automatic Gain Control (AGC) is necessary to cope with the large dynamic range required for the amplifier. The presence of an AGC mechanism, other than ensuring a constant output signal irrespective of the input current, allows for optimum noise performance: maximum gain (maximum transresistance), hence minimum noise, is used for small signals.

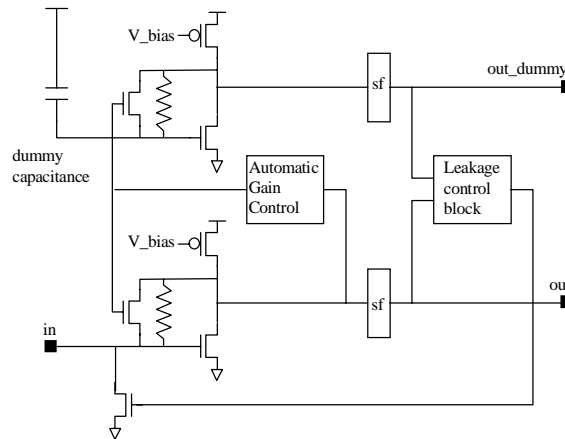


Figure 2: Architecture of the transresistance preamplifier. The two blocks marked “sf” are simple source followers.

The AGC is implemented by a transistor in parallel with the 16 k Ω polysilicon resistance, having its gate voltage controlled by a feedback loop. This feedback loop needs to be slow so as to be negligible at the signal frequency, as it needs only to compensate for the radiation-induced drop in the quantum efficiency of the photodiode. Such drop occurs during the whole LHC life cycle (10 years). The transresistance changes from about 16 k Ω for a 10 μ A signal (-20 dBm) to about 175 Ω for a 500 μ A signal (-3 dBm). Correspondingly, the bandwidth passes from 105 to 858 MHz.

To improve the Power Supply Rejection Ratio (PSRR) of the circuit, a pseudo-differential scheme has been used. The transresistance input stage has been replicated as a “dummy” circuit, as shown in the upper part of Figure 2. The output of both the true preamplifier and the dummy stage is used as the input to the differential limiting amplifier chain. Therefore, from the preamplifier output to the LVDS driver output, the signal is fully differential. This pseudo-differential scheme requires good matching between the input capacitance of the true and dummy branches. To match the PIN diode capacitance, we have integrated a dummy capacitance at the input of the dummy branch.

The output of the dummy circuit is moreover used as an input to the additional feedback loop controlling the photodiode leakage current sink. As for the Automatic Gain Control, the leakage control feedback needs to be very slow compared with the lower signal frequency. In fact, this circuit has to compensate for the increase in the photodiode leakage current, which is a slow radiation-induced process occurring during the whole LHC life cycle.

3.2. The limiting gain chain, the LVDS driver and the reset detection block

The output of the preamplifier is not fully differential, the signal coming from the dummy branch being DC. The first limiting amplifier of the chain needs therefore to be unbalanced for its output signal to be fully differential. This is implemented through the action of a “balancing” feedback block, as shown in Figure 1. This circuit block senses the peak of the output signals from the second amplifier of the chain, and controls the current unbalance between the two output branches of the first amplifier. The

amplifier chain performs an amplification of the signal and limits it to a pre-fixed peak-to-peak value, preparing it for optimum input to the LVDS driver.

The specifications of the circuit require the output to be Low Voltage Differential Signaling (LVDS). LVDS is a high speed, low power general-purpose interface standard using differential data transmission, and it is independent of a specific power supply [8]. The LVDS driver has been designed as a differential amplifier with load resistors, and its speed performance is well above the required 80 Mbit/s.

The transmission protocol foresees that the reset signal is coded as missing pulses for a long time period (2 μ s or more) [9]. The amplifier circuit is required to detect the transmission of the reset and respond to it by changing the status of a flag on a dedicated output line. To perform this task, we have integrated a reset block in the amplifier, connected to one of the differential outputs of the limiting gain amplifier chain as shown in Figure 1.

3.3. Circuit implementation

The final ASIC includes 4 amplifier channels, each occupying an active area of $0.5 \times 0.25 \text{ mm}^2$. The distance amongst the pads has been chosen to be compatible with wire-bonding and low cost bump-bonding techniques. Input pads are on the left of the chip, LVDS output pads on the right, and the power is distributed along the y-axis with pads on both the top and bottom of the chip. A layout view of the receiver chip is shown in Figure 3.

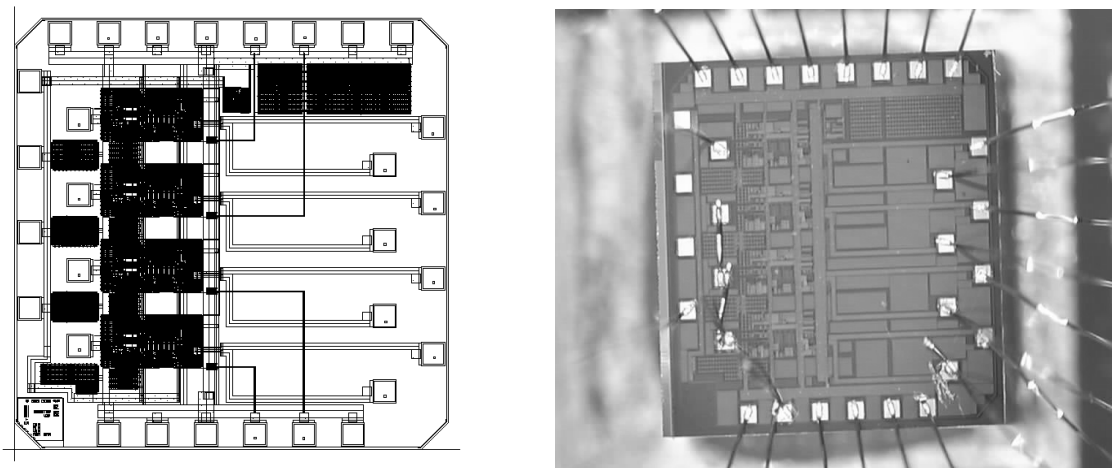


Figure 3: Layout view and picture of the receiver chip.

4. MEASURED PERFORMANCE OF THE OPTICAL RECEIVER

The optical receiver circuit was fabricated in a quarter micron CMOS process, then mounted on a dedicated test board bonding two channels to two PIN photodiodes, as shown in Figure 4. One of the two diodes had been previously irradiated with neutrons (mean energy 6 MeV) to a level of $6.5 \cdot 10^{14} \text{ cm}^{-2}$, whilst the other was new. The photodiodes were Fermionics type FB80S-7F InGaAs/InP detectors with $80 \mu\text{m}$ diameter and approximately $2 \mu\text{m}$ active InGaAs layer thickness on an InP substrate. The radiation hardness of this photodiode type has already been demonstrated [10].

4.1. Measurement of the circuit functionality

The chip has been measured and the performance is well within all specifications. The current consumption for the full chip is about 50 mA, which for the operating voltage of 2.5 V corresponds to a power consumption of 125 mW, or approximately

32 mW/channel. We could test the functionality of the AGC over a wide input signal range up to +2.8 dBm (1.9 mA) without observing any sign of saturation: a dynamic range of more than 30 dB is therefore achieved. Increasing the DC level of the input signal to simulate the radiation-induced photodiode leakage current, we could test with success the functionality of the leakage compensation feedback loop up to 200 μ A. The circuit performance is not affected by a change of the power supply voltage of $\pm 20\%$ around the nominal value of 2.5 V. Figure 5 shows an example eye diagram measured at the output of one of the receiver channels for an input signal modulation amplitude of -20 dBm at 80 MHz. On the right side, it is possible to appreciate the increase of the noise in presence of a leakage current of about 130 μ A.

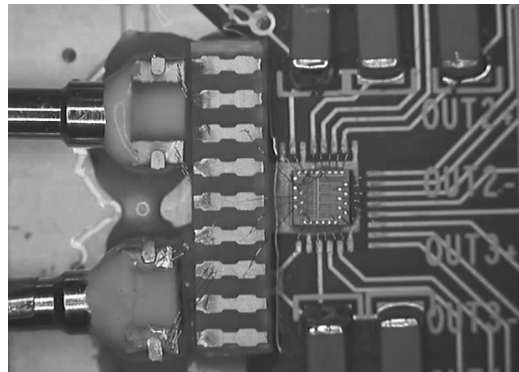


Figure 4: The optical receiver chip has been mounted on a dedicated test board and two channels have been bonded to two PIN photodiodes.

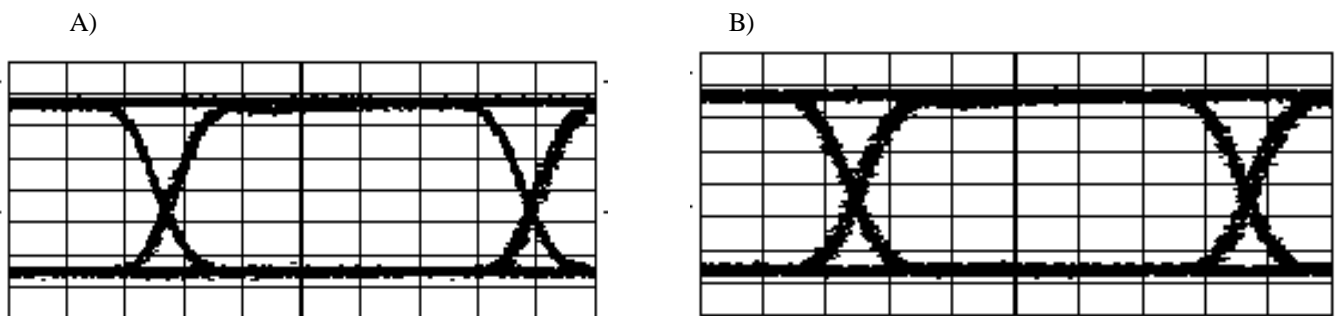


Figure 5: Eye diagram measured at the output of the receiver circuit for an input signal of 10 μ A at 80 MHz. A) without any leakage current. B) with 130 μ A leakage. X-axis: 50 mV/division. Y-axis: 2 ns/division.

4.2. Bit Error Rate (BER) measurements

The most complete way to assess the transmission quality of a digital optical link is to measure its Bit Error Rate (BER), defined as the ratio of incorrectly received bits to the total number of bits received. We performed this measurement with the setup shown in Figure 6, at a bit rate of 80 Mbit/s.

We measured the BER of one optical channel of the receiver (the channel where the new photodiode was mounted) and evaluated the impact of the channel-to-channel crosstalk and of noise on the power supply line. The result is shown in Figure 7. We first measured the BER of the optical channel while keeping the other channel silent (“no crosstalk”). As in the application two channels will operate at the same time, this measurement is only representative of the “absolute” channel performance. Then, an uncorrelated signal of maximum amplitude (-3 dBm) was applied to the neighbour channel, and the measurement was repeated (“crosstalk”). This measurement, which is representative of the application, shows that the specified BER of 10^{-12} is

achieved for an input optical power of about -27 dBm. Finally, this last measurement was repeated while simultaneously introducing a 20 mV peak-to-peak signal on the 2.5 V power supply (“crosstalk + noise on PS”) to evaluate the Power Supply Rejection Ratio (PSRR) of the circuit. Even in this severe condition, the knee of the BER curve is around -24 dBm, and the specification of 10^{-12} at -20 dBm is met with wide margin. The same set of measurements was repeated with very similar results on the channel where the irradiated photodiode was bonded. The diode was actually irradiated with neutrons several months before this measurement, and the damage from the neutron irradiation was very limited: the efficiency decreased by about 10% and the leakage current rose to less than $5 \mu\text{A}$ [10].

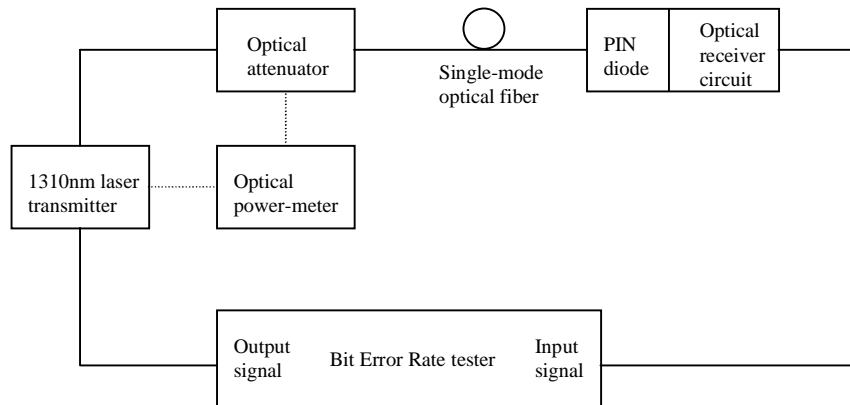


Figure 6: Test setup for the BER measurements.

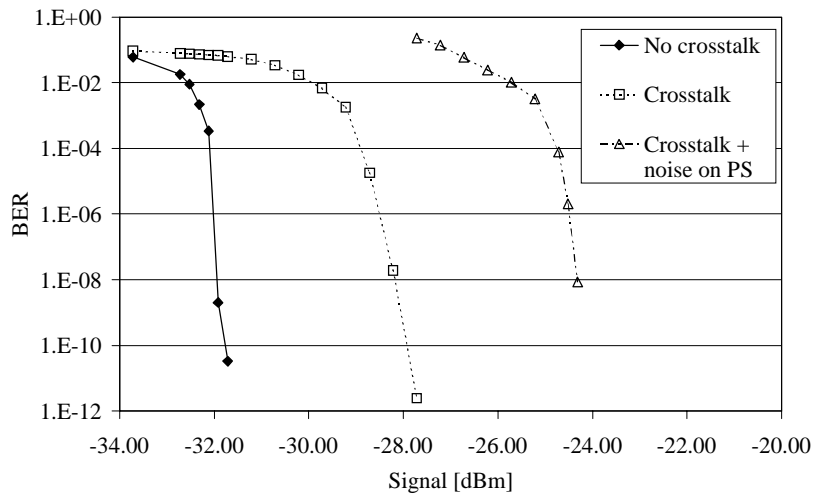


Figure 7: BER measured on one of the optical channels in different conditions.

In presence of a leakage current from the photodiode, we expect the BER performance to degrade. This current is sunk to ground by the NMOS transistor whose drain is connected to the preamplifier input as shown in Figure 2, introducing an additional noise source. We measured the performance degradation repeating the BER measurement in the “crosstalk” condition, and simulating the diode leakage current by increasing the input signal DC level. The comparison with the absence of leakage current in Figure 8 shows that the performance penalty is less than 1 dB for the highest current of $96 \mu\text{A}$.

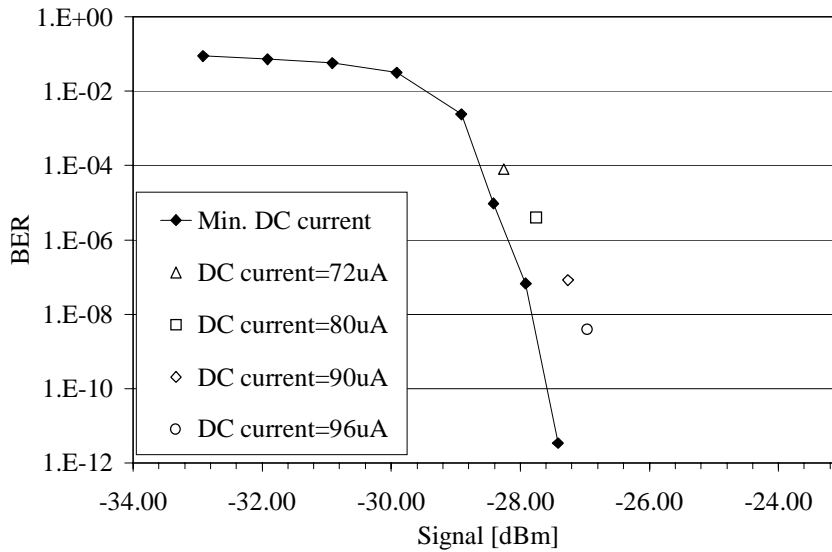


Figure 8: Influence of increasing levels of DC input current on the BER. The measurements were made in the “crosstalk” condition and simulate the effect of radiation-induced leakage current in the diode.

A final BER measurement was made to evaluate the receiver performance in the real operational condition, that is when both the clock and the data pattern are transmitted through the optical link. The two optical channels were therefore used, one to transmit the 80 MHz clock (signal amplitude: -3.46 dBm; DC current: 100 μ A) and the other for the data pattern (signal amplitude: -18.5 dBm; DC input current: 96 μ A). This represent a condition which is very close to the worse possible according to the design specification, with the additional use of an irradiated photodiode for the optical line where data were transmitted. In these conditions, the transmission line run without any error for 15 days and 14 hours, which indicates a BER below $9.27 \cdot 10^{-15}$, by far better than the specified 10^{-12} .

5. IRRADIATION RESULTS

The receiver circuit has been irradiated with X-rays at our SEIFERT RP-149 irradiation system, which produces a spectrum peaked at about 10 keV. The irradiation took place at room temperature up to a total dose of 20 Mrad(SiO_2), at a dose rate of about 18.4 krad(SiO_2)/min. The functional test performed after irradiation showed that a 6% increase of the power consumption was the only measurable effect. To more precisely evaluate the impact of the irradiation, we repeated the BER measurement, then put the chip in the oven for an annealing at high temperature for 168 hours. Due to the presence of materials possibly damageable on the test board, we did not apply the standard 100°C [11] during the annealing, but we limited the temperature to 80°C. After annealing, the BER measurement was repeated again. Since no difference was observed in both the power consumption and the BER performance immediately after irradiation and after the annealing, only the after-annealing results are shown.

The radiation-induced performance degradation is observable in the BER curve measured on one optical channel while the other channel is kept silent. In that case, the shift of the knee towards bigger signal is limited to about 1 dB, as shown in Figure 9.

When the measurement is repeated in the “crosstalk” condition, that is with the neighbour channel operational, the BER curve superposes to the one measured before irradiation. Moreover, Figure 10 shows that no difference is observed between the two optical channels, even though one of them actually mounts an irradiated photodiode. Also in the presence of noise injected on the power supply, the BER performance is not affected by the irradiation.

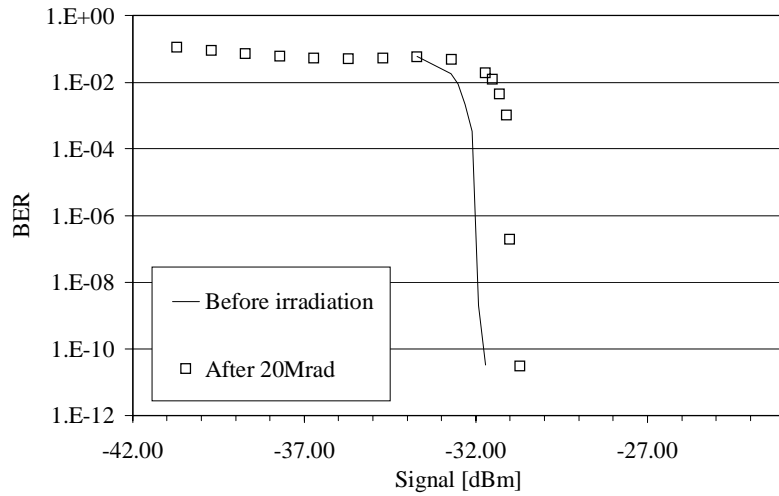


Figure 9: Shift in the BER curve induced by an irradiation up to 20 Mrad(SiO_2). The measurement has been made while keeping the neighbour optical channel silent.

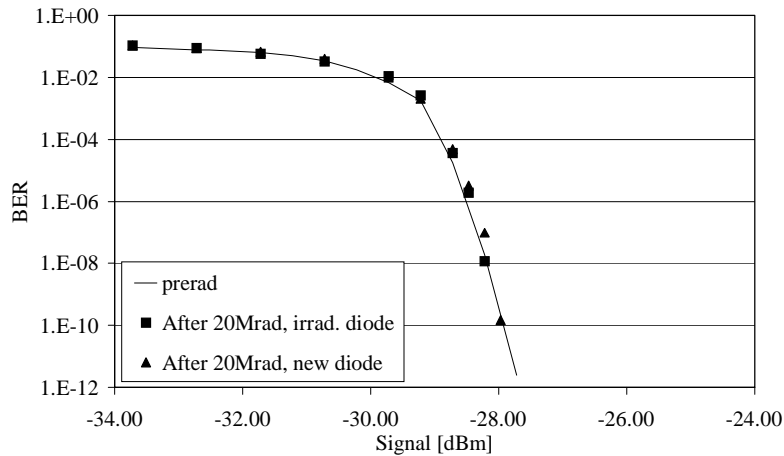


Figure 10: Measured BER before and after irradiation in the “crosstalk” condition, which is representative of the application. The performance of the two optical channels is very similar, even though one of them is mounting an irradiated photodiode.

6. CONCLUSION

The first prototype of the optical receiver developed for the digital optical link of the CMS tracker has been fabricated in a commercial quarter micron CMOS technology. The thin gate oxide of such deep submicron process, together with the systematic use of enclosed NMOS transistors and guardrings in a radiation tolerant design approach, allow to achieve the multi-Mrad radiation tolerance required for the CMS tracker electronics.

The measured performance of the optical receiver is well within specifications: a dynamic range of more than 30 dB is achieved thanks to the use of AGC in the preamplifier, and the 80 MHz bandwidth is easily reached. The leakage current control feedback loop works beyond the required 100 μA to compensate the radiation-induced photodiode leakage current. All these

characteristics are unaffected by an X-ray irradiation up to 20 M rad(SiO₂). The power consumption of the four-channel chip amounts to about 125 mW, and increases by only about 6% after irradiation.

We measured the BER of two adjacent optical channels, and found that the required level of 10⁻¹² is reached for an optical power of the input signal modulation of about -28 dBm. Also the BER curve measured in these conditions was not affected by the irradiation, confirming the excellent hardness achieved using the radiation tolerant design approach.

A slightly modified version of the receiver circuit has been submitted for fabrication in the same CMOS technology. The modification to the previous design were required to cope with a change in the specification for what concerns the maximum DC input power. Moreover, a change in the detection of the reset signal was necessary to ensure a better reliability in the transmission of the system reset.

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