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# STATUS AND RECENT DEVELOPMENTS OF THE ANALOG SIGNAL OBSERVATION SYSTEM AT CERN PS

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# Status and recent developments of the Analog Signal Observation System at CERN PS

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***Abstract*--The nAos (new Analog observation system) at CERN's PS complex allows visualization of some 1500 analog signals in any of the workstations connected to the controls network. Signals are digitized close to their source using VXI oscilloscope modules and sent to the users via Ethernet. A sophisticated application program conveys the signal selection and settings to the VXI front-ends and displays all the requested signals in one virtual oscilloscope window.**

**The trigger pulses for the VXI oscilloscope modules are produced centrally near the Main Control Room of the PS and sent to the VXI crates oscilloscopes through long dedicated copper cables. To get to a sharper time definition, a new trigger production method has been tested with successful results. Timing events, encoded with an ultra-stable 10 MHz clock are sent as 32-bit messages through an optical fiber and converted locally into trigger pulses. The precision achieved with this method is better than 1 ns.**

**The paper describes the current system, presents its performances in operation and details the recent development on the trigger generation.**

## I. Introduction and System Topology

The nAos system has been in use at CERN since 1993, allowing operators and machine specialists in all of the laboratory's accelerators to precisely monitor more than 1500 analog signals in a coherent way. Before nAos, signals were distributed from their sources to the PS MCR[2] in analog form, leading to high levels of degradation and attenuation. Even with the use of thick copper cables, signals were severely distorted after traveling through distances of 100 meters or more of wires and relays. In the current system, signals are digitized as close to their source as possible to preserve their quality. Once digitized, the waveforms are sent to the MCR and office workstations, where an application program ensures the coherence of the acquisitions and displays the results in three virtual oscilloscope screens of four traces each.

Figure 1 shows the general system topology. There are two types of VXI crates: i) acquisition crates containing one or more multiplexer modules and typically four oscilloscope modules, ii) timing crates producing the trigger pulses that fire each oscilloscope in an acquisition crate. There are currently 22 acquisition crates and 2 timing crates installed in the PS. Both timing crates are populated by several 8-channel counter modules designed at CERN. Each output of these modules is programmed to produce a pulse after counting different amounts of four different external clock ticks following one of the 40 start pulses present in the front panel flat cable connector. It is tricky to ensure that two oscilloscopes of interest will fire their acquisitions at the same time, since their external trigger inputs are connected to two different outputs of the counter modules. This is achieved by placing all counter modules close together and making them share both the clock signals and the start pulses.

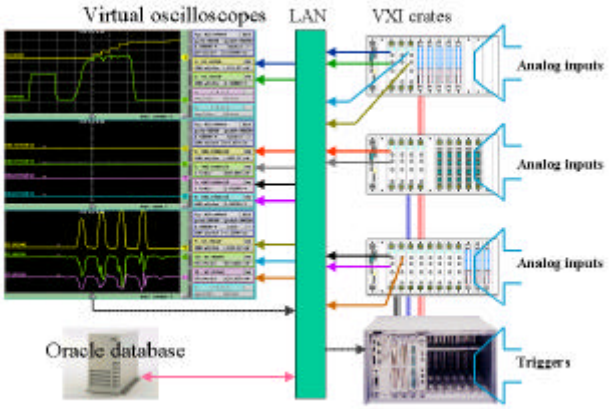


Fig. 1. General hardware topology of the nAos system.

On the software side, the VXI crates are controlled by the National Instruments VXIcpu-030 slot 0 module. This card allows a diskless boot though the network and runs the VxWorks real-time operating system. All startup and configuration data are stored in a central Oracle server, which is used both in the boot process and as a statistical tool for data logging and fault diagnostics. All the VXI crates communicate through the classic socket mechanism among themselves, as well as with the Oracle server and the application program running under Linux PCs in the MCR.

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[2] Main Control Room of CERN's Proton Synchrotron complex.

## II. REAL-TIME SOFTWARE ARCHITECTURE

One of the design requirements for the nAos system stated that the time between the acquisition of a signal and its visualization in the application program under Linux should never exceed 100 ms. An operator in the Control Room receives all kinds of real-time visual indications of machine performance, including video signals from beam screens, and a longer delay in the refreshment of the nAos display could lead to a feeling of incoherence. To achieve this 100 ms limit, VxWorks was chosen as the real-time operating system to develop all the front-end software. The NI-VXI libraries from National Instruments were used to control the VXI bus. Dynamic address allocation and module configuration at startup, a very nice feature of the VXI bus, is handled by the *resman* utility, the Resource Manager included in the same software package.

The real-time software running in each VXI crate controller is organized as a set of inter-communicating tasks as can be seen in figure 2.

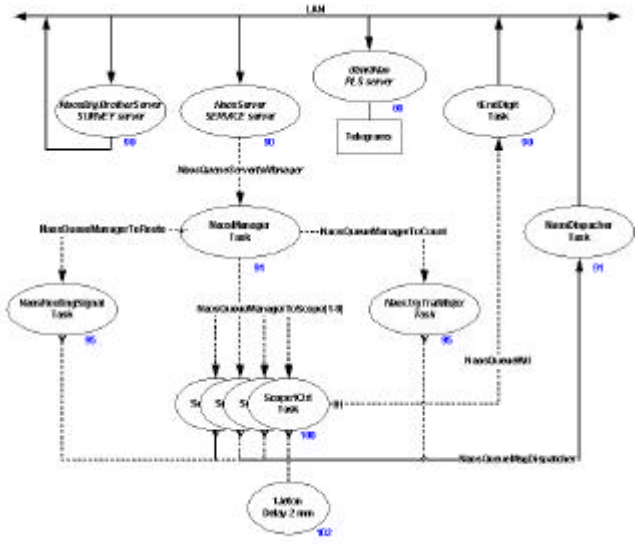


Fig. 2. A schematic view of the real-time software developed for nAos. Ovals represent tasks, with their priority indicated next to them. Tasks communicate among themselves via message queues (dashed lines) or through the network via sockets (solid lines).

Some of the tasks receive requests from the upper-level application program through sockets while others service the requests by actually communicating with the VXI modules. An example of such requests could be a user changing the time base of an oscilloscope by clicking four times on a wheel switch button. The four clicks are in fact four requests, which will be serviced one after the other. Due to the asynchronous nature of user requests, message queues were found to be the best approach for inter-task communication.

A set of test and diagnostic programs has been developed to make maintenance easier, and all user requests are logged to an Oracle server to derive statistics every month. These data determine whether the availability of certain signals must be increased. This availability depends on the scope to multiplexer input ratio for a given VXI crate. Some of the signals, called essential, have a dedicated oscilloscope input for themselves and are therefore always available.

The application program knows the layout of all signals, including their multiplexer and input numbers, as well as their possible routing paths, thanks to Oracle tables sitting on the server. All changes in layout must therefore be reflected immediately on the tables, but this is a minimal effort considering the benefits.

## III. VXWORKS TO LYNX-OS MIGRATION

In spite of many advantages of VXI systems, vendors tend to discontinue development and fabrication of VXI modules. E.g., the slot 0 module used in nAos, the National Instruments VXIcpu-030, based on the MC68030, is not produced anymore and has not been replaced by an equivalent module. In addition, the standard operating system used in the PS control system, LynxOS, is not available for any commercial VXI slot 0 module.

The solution to these problems considered as most suitable is the development of a VME-VXI adapter, which allows using any VME processor as VXI slot 0 module. This makes it possible to ensure a common evolution of the processor hard- and software in VXI and VME crates in the PS control system. The cost is to write some specific software: a resource manager to integrate the VXI systems in the general configuration management system, the drivers to support the VME-VXI interface, and a set of library routines to provide the application programs with the set of functions implementing a library interface to support the VXI register based protocol and the VXI word serial protocol.

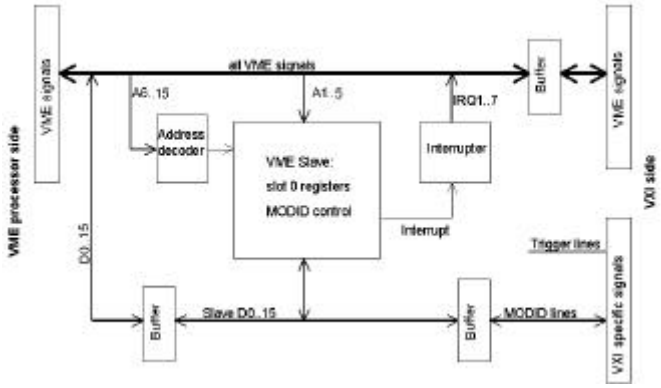


Fig. 3. A schematic view of the VME-VXI interface.

The VME-VXI interface essentially consists of a VME slave in the short address space, accessible both from the VME processor and the VXI devices. It contains all slot 0 registers and the control mechanism for the MODID lines. A critical part is the VME interrupt mechanism serving interrupts from register based VXI modules, from the location monitor (indicating the arrival of a serial message to the slot 0 module), and from writing into the signal register. Since writing into the signal register can be done simultaneously by more than one (message based) VXI

module, the slot 0 slave has to provide a queuing mechanism for the information written into the signal register.

## IV. Developments on the Trigger Side

As we described earlier, the current trigger subsystem consists of a centralized set of two VXI timing crates with counters that produce trigger pulses. Because they are very close together, each counter module can receive the same set of clocks and start pulses and we can be sure that the jitter between two counter outputs is negligible. One can argue that this solution requires a copper cable per oscilloscope trigger input, which is quite a burden considering that the nAos system consists of more than 100 oscilloscopes, some of them being more than 300 meters away from the trigger production facility. The fact is that the cables were already installed, since they were the way for the analog signals to get to the MCR in the system existing before 1993.

However, for new signals and for the use of nAos in other facilities, the wiring cost remains high, and a different solution has been developed and successfully tested in the lab. This new subsystem uses the standard Manchester-encoded messages (see figure 4) used for slow timing in all of CERN's accelerators to produce the trigger pulses close to the oscilloscopes after reception of a pre-defined message. These messages are all validated by the arrival of a special *millisecond* message, which contains a value of 0x01 in the first byte. A major improvement has been achieved on the jitter among the different receivers, going from ±150 ns in CERN's timing system to better than 1ns.

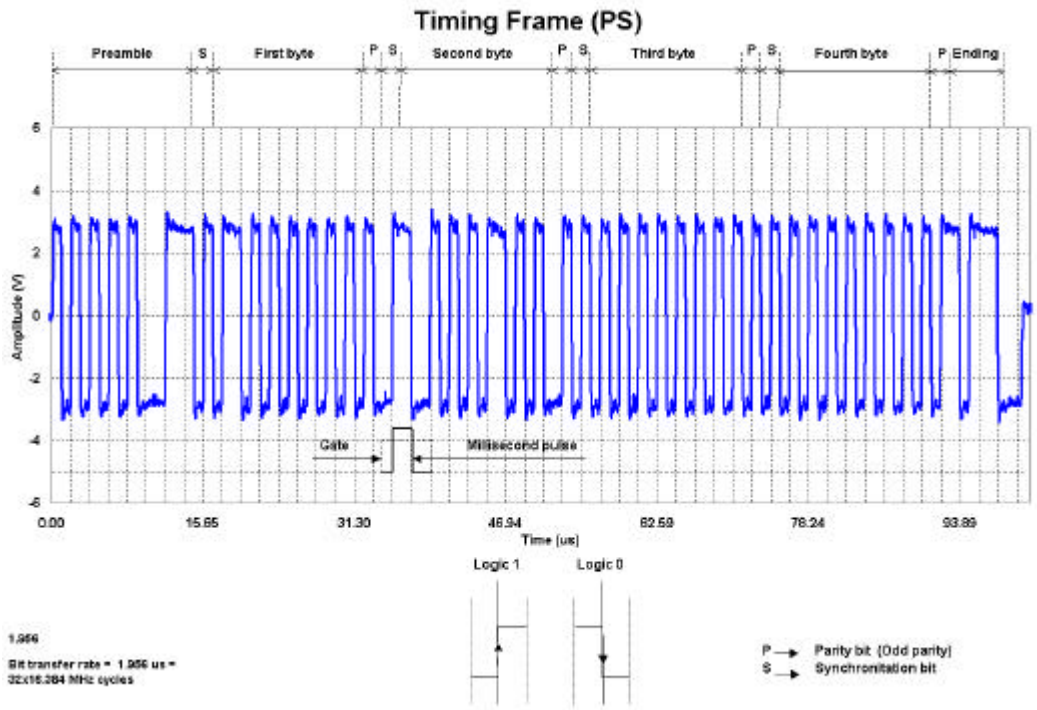


Fig. 4. An example of a Manchester-encoded 32-bit message used in the timing distribution network of CERN's SPS accelerator. The master encoding frequency is 16.384 MHz. Note that the first byte is 0x01: this is a millisecond event.

This has needed the development of a new timing message decoder in VHDL that uses a clever trick: because the millisecond message is completely defined by the first byte, one can open a gate after the first parity bit and let the sync bit of the next byte go through as the millisecond tick. This lifts any uncertainty due to the free-running oscillators used for decoding, since the rising edge of the message signal itself is seen by all receivers at the same time. The drawback is that the granularity of this trigger source is only1 ms, but this is often enough for most signals, and can be used as a start for local high-speed counting in other cases.

## V. References


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[2] J. C. Bau, G. Daems, J. Lewis, J. Philippe, "Managing the Real-Time Behaviour of a Particle Beam Factory: the CERN Proton Synchrotron Complex and its Timing System Principles" *Xth IEEE Real-Time Conference 97, Beaune (France), September 22-26, 1997.*