Design and Characterization of a DAC for the Slow Control of the Pixel Chip

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Abstract

A digital to analog converter for slow control of pixel front-end chip has been designed in a standard 0.35µm CMOS technology to prove the effectiveness of the chosen circuit structures for this application. The DAC provides a total output current variation of about 13 µA with 8 bits of accuracy (LSB ≅ 51nA). The circuit is based on a PMOS current bank, since an "enclosed" NMOS of reasonable size would operate in weak inversion for these current levels and would hence be unsuitable for accurate current sources. The bit value determines whether the corresponding current is switched to the output or sent to ground. The occupied area is about 300µm x 300µm and total power dissipation is 85µW. The results of the test measurements performed on 31 fabricated prototypes show that statistical fluctuations of the output current due to mismatch are negligible compared to the desired accuracy for all the input configurations. Results of X-ray irradiation tests carried out at the CERN facility will be also presented.

I. INTRODUCTION

One of the main requirements in a large pixel detection system, like ALICE's one [1], is the performance uniformity among the several thousands of channels which compose the system. This property must be preserved also in presence of significant irradiation doses, which can cause drifts in the behaviour of the different channels. To get more uniformity and to counteract the irradiation effects, each pixel read-out chip must be equipped with some digital to analog converters (DACs) able to vary some crucial bias settings of the front-end circuit in dependence of a digital configuration word. In this way, a re-calibration of the whole pixel detection system can be done on a regular basis, thus increasing the detector lifetime.

The DAC should deliver in output a variable current which can be used directly to set the bias points most effective on the behaviour of the single channel. Of course the DAC specifications are given in terms of area occupancy, less than 500µm x 500 µm, power consumption, which must be less than 200µW, accuracy, at least 8 bits, and last, but not least, radiation hardness. In particular, the DAC accuracy is strongly dependent on the effects of parameter mismatch which, in the design phase, is the most important issue to deal with. The kind, size and bias of the devices used to generate the output current must be carefully chosen to control at acceptable levels the errors induced by mismatch. Moreover suitable layout techniques must be adopted to guarantee the needed matching among the current sources.

The prototype proposed in this work has been designed in a standard 0.35µm CMOS technology to validate the adopted design solutions for the intended application. A total number of 36 chips have been fabricated and 31 out of them have been assembled on a very simple board and fully characterized to evaluate the DAC performance in terms of offset and gain errors and integral and differential non-linearity errors (INL and DNL respectively). In particular, DNL measurements show that the effects of parameter mismatch has been correctly taken into account and that the desired 8 bit accuracy has been achieved.

X-ray irradiation tests have been also carried out at CERN with different irradiation doses and their results show that the circuit is robust against irradiation induced leakage currents up to 10Mrad. Nevertheless threshold variations induced by irradiation cause sensible shifts in the average currents delivered by the DAC, which indicates that the circuit used to extract the threshold voltage is able to compensate just small V_{TH} variations.

Further post-irradiation measurements show that the DAC accuracy in terms of DNL is poorly affected by irradiation and that the pre-irradiation input-output characteristic can be easily recovered for doses up to 2Mrad varying the reference voltage of the threshold extraction circuit.

II. THE PROPOSED DAC

The proposed DAC has the classic current division configuration [2-4], based on an array of 2^n-1 elementary current sources each delivering the current corresponding to the least significant bit I_{LSB}. The 2^n-1 currents are suitably summed in order to obtain the n "bit currents", scaled as the powers of two. The DAC configuration is set by means of n PMOS deviators which send each bit current to ground or to a summing node, as depicted in figure 1.

Two further circuit blocks are shown in figure 1. The first, namely X_{REF}, is needed to provide the elementary current sources of the array with the suitable bias voltage. Global variations of the MOS threshold voltages are compensated by means of this circuit, which is basically the V_{TH} extractor [5] represented in figure 2.

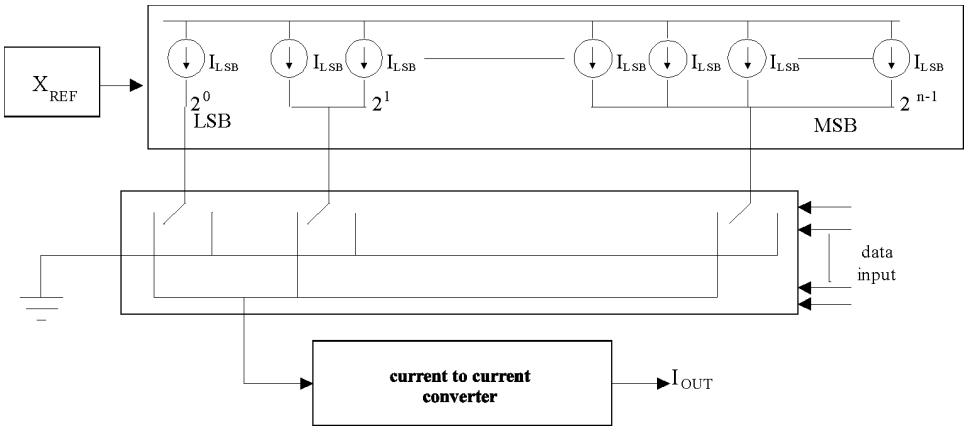

Figure 1: Structure of the proposed current division DAC

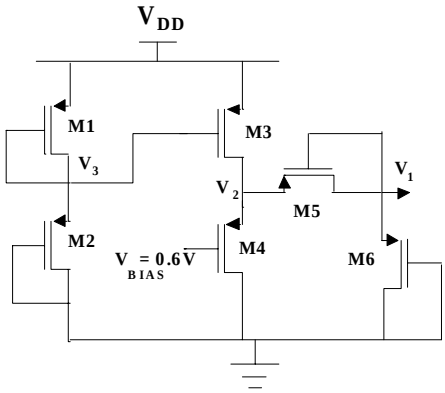

Figure 2: Threshold extractor used to bias the current array

A relatively small current flows in M_5, which is a large W/L transistor working in subthreshold region ($V_{GS5} \cong V_{TH}$). If this current is negligible compared to $I_{D3} \cong I_{D4}$, the output voltage V_1 is given by:

$$V_1 = \frac{V_{DD}}{2} + V_{BIAS} - |V_{TH}| \qquad (1)$$

A $|V_{TH}|$ increase induced by irradiation in the PMOS transistors which compose the current array is thus compensated by a decrease of the bias voltage V_1, resulting in a constant overdrive of the current sources.

The current to current conversion block in figure 1 is needed after the summing node to re-scale the current generated by the array I_{DAC} to the value needed in output I_{OUT}. In fact I_{DAC} is fixed on the basis of considerations related to matching, area occupancy and power available and, in general, is greater than I_{OUT}. The schematic of the current conversion block is reported in figure 3 [6].

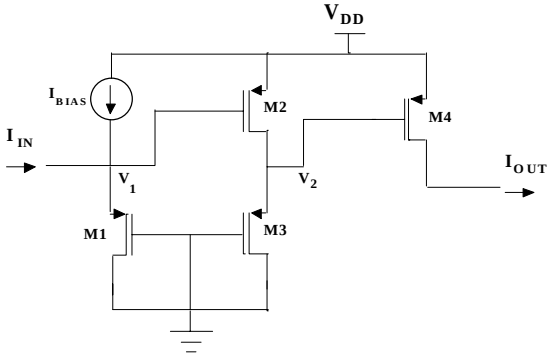

Figure 3: Current to current conversion circuit

I_{BIAS} is the minimum current delivered by the current source array when all the bits of the DAC configuration are zero. If M_2 and M_3 are transistors of the same size, V_{GS4} is equal to V_{GS1}, thus the relationship between I_{OUT} and $I_{DAC}=I_{IN}+I_{BIAS}$ is:

$$\frac{I_{OUT}}{I_{DAC}} = \frac{(W/L)_4}{(W/L)_1} \qquad (2)$$

In our case this ratio is equal to 2/3.

PMOS deviators have been used instead of simple switches to set the DAC configuration, since they guarantee more reliability in presence of leakage currents induced by irradiation.

III. THE CURRENT SOURCE ARRAY

The value assigned to the elementary current source of the array I_{LSB} has been decided considering the power available and the desired output current variation, expressed as a fraction of the average value. Since the power supply voltage is fixed at 2.2V, the total current delivered by the DAC (I_{BIAS} included) is known and the variation desired in output (± 75% of the average value), along with the number of bits, sets I_{LSB}=90nA. The transistors which compose the current source array must be carefully designed to prevent the effects of parameter mismatch on the DAC accuracy. In particular, long channel transistors must be used to achieve reasonably high values of overdrive, needed to limit the effects of threshold mismatch. NMOS transistors are unsuitable, since the "enclosed" layout design [7], mandatory for radiation hardness, would require an unacceptable area occupancy in case of long devices. Consequently the current array is composed by PMOS transistors and their width has been fixed at the minimum value of the technology, i.e. W=0.8μm, to meet the area occupancy specification. The value of the length L and, thus, the overdrive V_{GST} of the PMOSes have been determined considering the matching properties of the transistors employed as a function of W and L, according to the Pelgrom's model [8]. The standard deviation of the current delivered by the DAC has been expressed in terms of the matching parameters of the technology used, and, imposing that its value is less than $I_{LSB}/2$, the minimum length of the elementary current source has been derived, resulting in the following formula:

$$L \geq \sqrt{\frac{\frac{K_P}{2\beta}\left(\frac{A_\beta^2}{\beta^2} + 4\beta\frac{A_{V_{TH}}^2}{I_{LSB}}\right)}{\frac{1}{4\cdot 2^n}}} \qquad (3)$$

with $\beta = \frac{K_P}{2}\frac{W_{MIN}}{L}$. Of course the length of the transistor evaluated using eqn.(3) must be compliant with the area specification, otherwise the number of bits of the DAC must be reduced and a new iteration of the design process must be done. In our case the minimum transistor length provided by (3) is 37μm, which results to be compatible with the area specification. The resulting overdrive V_{GST} is 0.5V.

Extreme care has been devoted to the layout of the current source array. Each bit current is composed by 2^i elementary current sources arranged in a common centroid structure as described in [9]. Dummy transistors have been added on the edge of the current source bank to avoid mismatch due to border effects and the power supply lines have been adequately dimensioned to get rid of errors due to excessive voltage drops.

IV. EXPERIMENTAL RESULTS

The output current of 31 DAC prototypes has been measured for each of the 256 possible configurations using an HP4155A. Five different series of measurements have been taken to obtain an average input-output characteristic for each prototype in order to reduce measurement errors, and the maximum variance of the current values for each DAC configuration is negligible compared to the LSB current.

In figure 4 the average input-output characteristic of the whole sample of measured circuits is represented, along with the one predicted by simulation. It is apparent that the measured current values are apparently lower than the ideal ones, resulting in a appreciable amount of offset and gain errors. This is probably due to real V_{TH} values different from the simulated ones but does not represent a major source of problems for the application of the DAC, since the ideal characteristic can be easily achieved just varying the reference voltage of the threshold extractor V_{BIAS}. Table 1 summarizes the main global features of the DAC.

The integral non-linearity error (INL) has been evaluated considering the end point line method. For each circuit the straight line connecting the first and the last points of the input-output characteristic has been determined and INL has been computed for each configuration as the difference between the measured output current and the corresponding value on the end point line. The average INL for the 31 prototypes is depicted as a function of the DAC configuration in figure 5 and exhibits a typical behaviour, peaking in the central region of the DAC characteristic. The maximum value of the average INL is about 80% of I_{LSB}, while the maximum standard deviation of INL is about 85% of I_{LSB}, which are adequately low values.

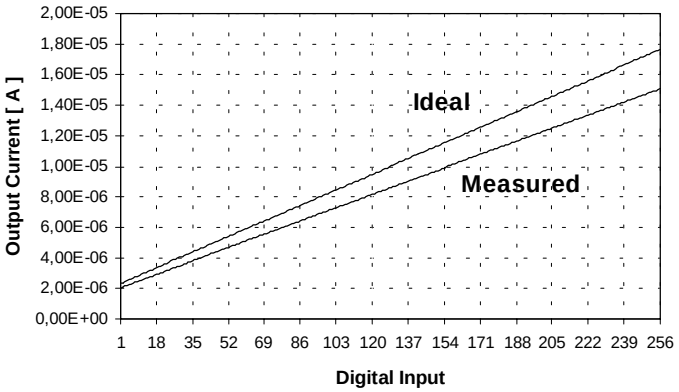

Figure 4: Average input-output characteristic of the DAC compared to the simulated, ideal one

Table 1: Average DAC measured parameters

I_{LSB}	51.055 nA
ΔI_{OUT}	13.019 μA
Offset error	-290.43 μA
Gain error	-2.2810 μA
Area	300 x 300 μm^2
Power dissipation	85 μW

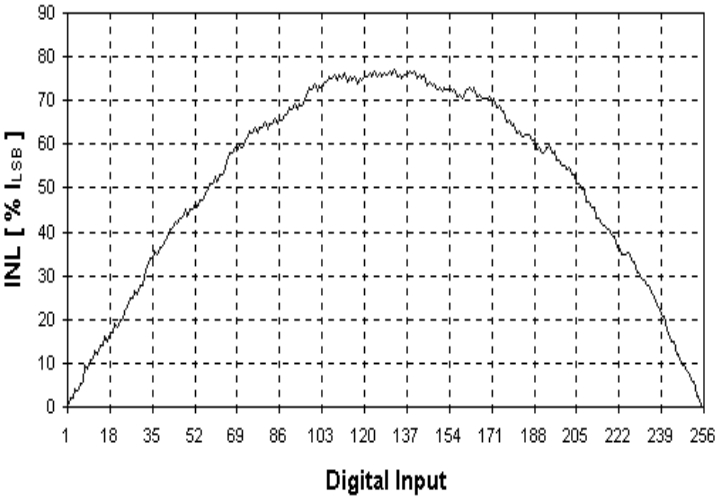

Figure5: Average value of INL for the 31 measured prototypes

The differential non-linearity error (DNL) is defined for the i-th configuration in the following way:

$DNL_i = INL_i - INL_{i-1}$

The value of DNL should be always less than $I_{LSB}/2$, otherwise the variation of the least significant bit of the DAC would not make any sense and the DAC accuracy would be less than the desired 8 bits. Figures 6a and 6b shows respectively the average value and the standard deviation of the DNL as a function of the DAC configuration.

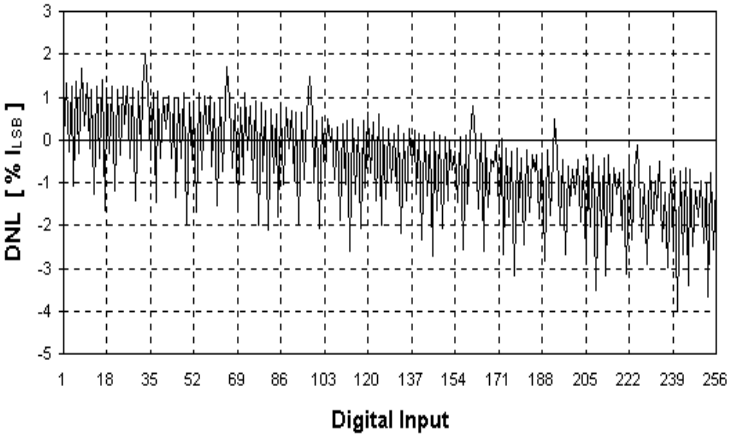

Figure 6a: Average value of DNL for the 31 measured prototypes

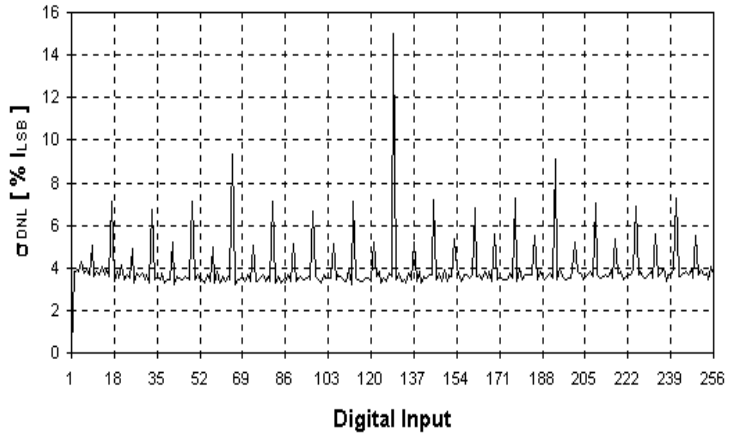

Figure 6b: Standard deviation of DNL for the 31 measured prototypes

As far as the average DNL is concerned, its value is always negligible and does not exceed 4% of I_{LSB}. On the other hand Figure 6b shows that the standard deviation of DNL exhibits peaks corresponding to the configurations in which a remarkable number of elementary current sources are switched on or off. In fact, the highest peak is obtained in the passage from the configuration 01111111 to the configuration 10000000, that is when all the sources which delivers output current in the starting configuration are switched to ground and the complementary set of current sources is turned on to produce next configuration. The maximum DNL standard deviation is about 15% of I_{LSB}, thus the probability that the least significant bit of the DAC is not meaningful is negligible. In fact, the maximum measured DNL for all the 31 measures prototypes is about 37% of I_{LSB}, thus preserving the validity of the LSB.

V. IRRADIATION TESTS

Several irradiation tests have been performed by means of the X-ray tester at CERN. The total irradiation doses considered are 10Krad, 50krad, 300Krad, 500Krad, 2Mrad and 10Mrad and two chips have been tested for each dose. During the irradiation, the DAC has been powered at 2.2V and the total current delivered by the power supply has been monitored. The output terminal has been left floating, thus the measured current includes the contributions of the whole current source array, the bias circuit and part of the output stage.

Figure 7 summarizes the experimental results achieved in terms of total current shift measured after the irradiation as a function of the total dose. The measured current is always decreasing with the irradiation dose, thus no effects of leakage induced by irradiation is observed up to 10Mrad. Since all the devices used are PMOSes, the variation of the total current is caused by the shift of the their threshold voltages, which, in absolute value, increase linearly with the irradiation dose. It can be concluded that the technology used is robust enough, since no leakage was observed, but the threshold extraction circuit is able to compensate just moderate threshold shifts, corresponding to no more than 50Krad of irradiation dose. Thus an improvement of the bias circuit design is mandatory, unless the reference voltage V_{BIAS} is varied .

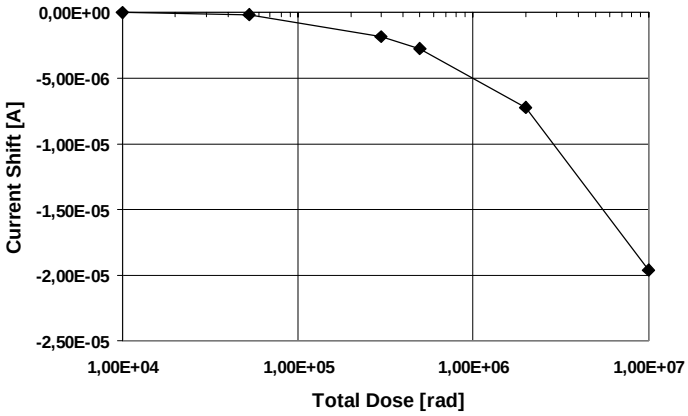

Figure 7: Total current shift as a function of the irradiation dose

Since it was difficult to reproduce the measurement setup needed to obtain the input-output characteristics of the DACs soon after the irradiation tests, assessment of integral and differential non-linearity errors have been carried out in Bari, after few days of annealing at room temperature.

Figure 8a and 8b represent respectively the variations of the average DNL and of the standard deviation of DNL after the irradiation as a function of the total dose.

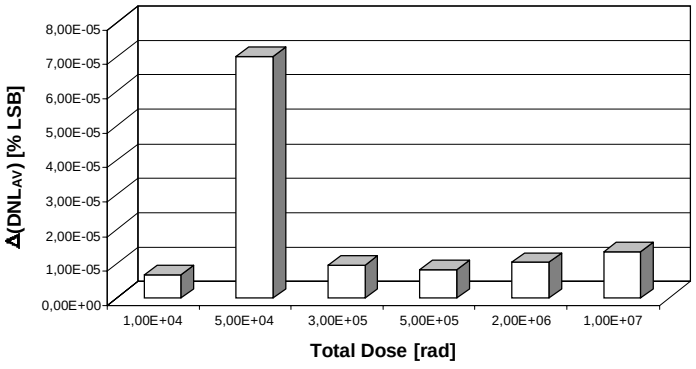

Figure 8a: Variation of the average DNL as a function of irradiation dose

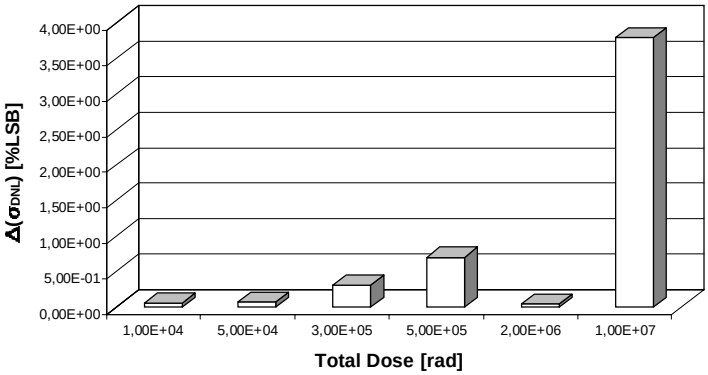

Figure 8b: Variation of the standard deviation of DNL as a function of irradiation dose

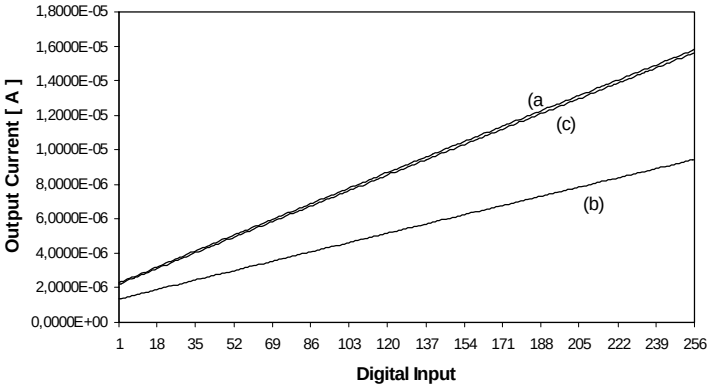

Figure 9: Input-output characteristics for the DAC:
(a) pre-irradiation, V_{BIAS}=0.6V
(b) post-irradiation (2Mrad), V_{BIAS}=0.6V
(c) post-irradiation (2Mrad), V =0.25V

Post-irradiation measurements show that the DAC performance in terms of DNL is not affected in substantial terms by the irradiation: the maximum variation of the average DNL is definitely negligible compared to I_{LSB} (figure 8a) and its standard deviation increases just by 4% of I_{LSB}, with respect to the pre-irradiation value (figure 8b).

The shift in the average current delivered by the DAC as a consequence of irradiation can be compensated by varying the reference voltage of the threshold extractor, V_{BIAS} in figure 2. In figure 9 the input-output characteristics of a DAC irradiated up to 2Mrad have been reported before and after the irradiation with V_{BIAS} at nominal value, i.e. 0.6V. After the variation of the reference voltage to 0.25V, it is possible to restore with a sufficient accuracy the pre-irradiation characteristic, as figure 9 shows. Notice that the V_{BIAS} variation does not affect appreciably the average value of DNL, nor its standard deviation, thus the accuracy of the DAC is preserved.

VI. CONCLUSIONS

A digital to analog converter for application to the slow control of the pixel front-end chip has been designed, realized and fully characterized. The circuit has been designed using only PMOS devices, to avoid the resort to area expensive enclosed NMOS devices for radiation hardness purposes. The circuit structure and the size chosen for the devices allow to achieved the desired 8 bit resolution, as shown by the differential non-linearity error measurements: the average DNL is less than 4% of LSB and its standard deviation does not exceed 15% of LSB. Irradiation tests up to 10Mrad have been carried out and the results show that the DAC accuracy is just slightly affected by irradiation: no leakage current effects have been observed and the only remarkable irradiation effect is the threshold shift of the PMOS transistors. Further measurements indicate that this effect can be compensated by varying the external reference voltage of the bias circuit, which is unable to counteract threshold shifts caused by more the 50Krad of total dose.

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