Monolithic Active Pixel Sensors for High Resolution Vertex Detectors

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Abstract

A novel Monolithic Active Pixel Sensor (MAPS) for charged particle tracking is presented. The partially depleted thin epitaxial layer of a low-resistivity silicon wafer is used as a sensitive detector volume from which the charge liberated by ionising particles is collected by diffusion. The sensor is a photodiode within a special structure allowing the high detection efficiency required for tracking applications. Two prototypes have been designed and fabricated using standard 0.6 and 0.35-micron CMOS processes. Results of the first prototype are presented, which is made of four arrays, each containing 64×64 pixels with a readout pitch of 20 microns in both directions. Extensive tests made with a soft X-ray source (^{55}Fe) and beams of minimum ionising particles (pions of 15 and 120 GeV/c) at CERN have demonstrated the predicted performance. The individual pixel noise of around 12 ENC leads to an extremely favourable signal to noise ratio for minimum ionising particles for which over 1000 electrons can be collected at the peak of the Landau distribution. The new circuit in the 0.35-micron process on a thinner epitaxial layer seems to have similar good performance. These new devices are extremely promising for future high precision vertex detectors as they provide solutions with a very low material budget and with high resolution at relatively low cost due to their fabrication in a standard submicron CMOS technology.

I. Introduction

Monolithic pixel sensors made in a CMOS technology, are used today as an alternative to CCDs for many applications in visible light imaging[1]. The advantages are in particular low cost since they are produced in a standard process and the possibility of random access to each pixel. The use of this technology for the detection of charged particles is challenging since only the very thin epitaxial layer of the silicon is available as sensitive volume. On the other hand, this allows to thin down the substrate to its mechanical limits and to build vertex detectors with an extremely favourable material budget. If desired for an application, the pixel size could be extremely small. The actual pixel size will be constrained by the additional electronics integrated on the pixel, necessary for certain applications. Further, the use of deep-submicron technologies offers intrinsically radiation hard devices.

This paper reports on the first successful application[2] of a monolithic pixel sensor in a standard CMOS technology for the detection of charged particles with 100% efficiency and a few micron spatial resolution. First the principle of operation is briefly described and then the implementation in a 64×64 cell prototype is explained in the following section. Sections IV and V treat the problem of charge collection and absolute calibration of the measured charge. In the last two sections we report on measurements in a high-energy particle beam and in the end we outline possible developments for future colliders.

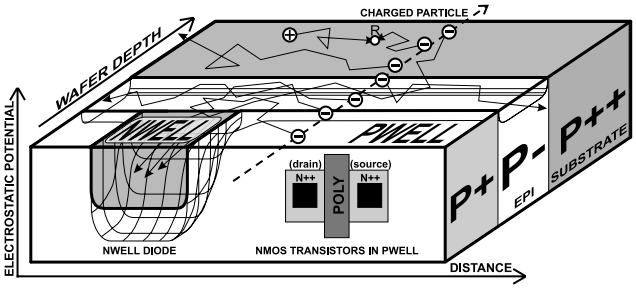

Figure 1: Sketch of the structure of a MAPS for charged particle tracking. The charge-collecting element is an n-well diode (n^+) on the p-epitaxial layer. Because of the difference in doping levels (about three orders of magnitude), the p-well and the p^{++} substrate act as reflective barriers. The generated electrons are collected by the diode.

II. Operation Principal of a MAPS

Fig. 1 sketches the structure of a MAPS: one coordinate along the substrate defining the pixel dimensions and the second coordinate representing the depth of the structure into the epitaxial layer and the substrate of the wafer. The third coordinate indicates qualitatively the electrical potential generated by the

presence of the very different doping concentrations in the p^{++}-substrate, the epitaxial layer and the p^{+}-layer of a twin-tub CMOS-process. The active element is an n-well/p-epi diode imbedded into this structure. Charge carriers are generated by the passage of an ionising particle. The electrons migrate by diffusion mainly within the epitaxial layer where they are confined by the above-mentioned potential barriers until they are absorbed by the collecting diode.

III. ELECTRICAL SCHEMA OF MIMOSA I

The first prototype chip consists of four arrays of 4096 pixels each, of slightly different designs[3]. The circuit was produced in a standard 0.6 µm CMOS process (3M+2P) with an about 14 µm thick epitaxial layer. All pixels measure 20 by 20 microns. The basic detector structure is the n-well/p-epi diode with a very low capacitance of 3.1 fF, the optimum with respect to noise and conversion gain. In the second matrix we use four such diodes in parallel to improve the charge collection speed at the cost of increased electronic noise. Matrix three and four are based on the single diode structure to test a radiation hard layout of the transistors and to investigate the possible suppression of the substrate connection of the NMOS transistors. We concentrate in the following on the first two one- and four-diode pixel designs.

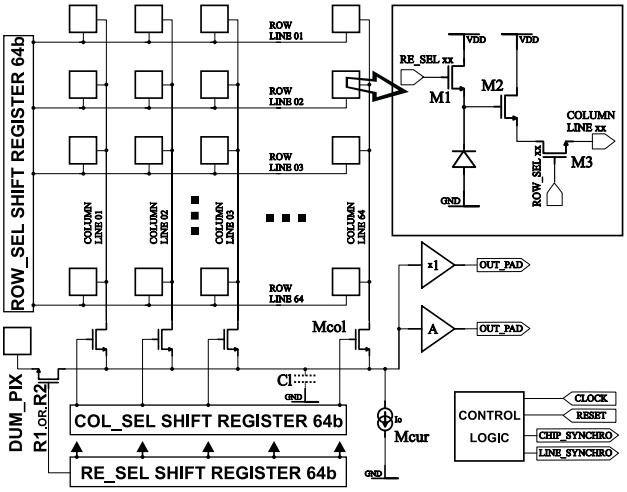

Figure 2: Simplified block diagram of a single array of the MIMOSA circuit. In the inset (right top) is the baseline architecture of a CMOS imager. Transistor M1 resets the photo site to reverse bias, transistor M3 is a row switch, while transistor M2 is the input of a source follower. The source follower current source (common to the entire row) and the column selection switch are located outside the pixel.

The functioning of the cell can be deduced from the schematic of Fig. 2: the photo leakage current of the diode is reset by transistor M1, M2 is the input transistor of the source follower for the read out and M3 is the row selecting switch. All pixels are multiplexed via the row and column shift registers onto a single source follower and an on chip amplifier with a voltage gain of four. A dummy pixel was introduced to reduce the output recovery time after a reset cycle. The necessary reset frequency depends on the diode leakage current. The read-out speed is typically 2.5 MHz and a correlated double sampling (CDS) is performed off-line by the subtraction of two consecutive read-out frames. CDS is an important tool to suppress all correlated noise sources like reset noise from transistor M1 and fixed pattern noise (FPN) from the device non-uniformity. Fig. 3 shows the cell layout of the one- and four-diode pixels.

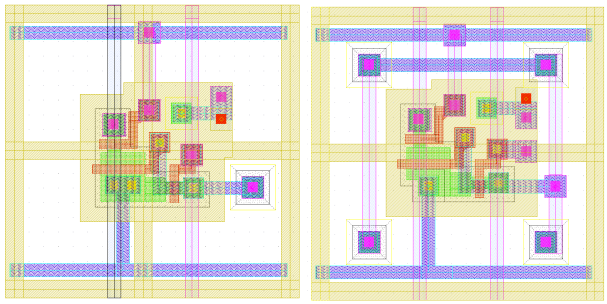

Figure 3: Layout of the one (left) and four (right) diode pixels of MIMOSA I.

IV. CHARGE COLLECTION

The ionisation charge liberated by an ionising particle (about 80 electron-hole pairs per micron for a minimum ionising particle at most probable energy loss) is exclusively transported by diffusion within the low resistive silicon. The charge carrier lifetime depends on the doping concentration[4] which varies strongly between the substrate and the epitaxial layer, 10^{+19} and 10^{+15} cm^{-3}, resulting in lifetimes in the order of 10 ns and 10 µs for the substrate and epitaxial layer, respectively. Only the regions of the substrate close to the boundary to the epitaxial layer can thus contribute to the collected charge.

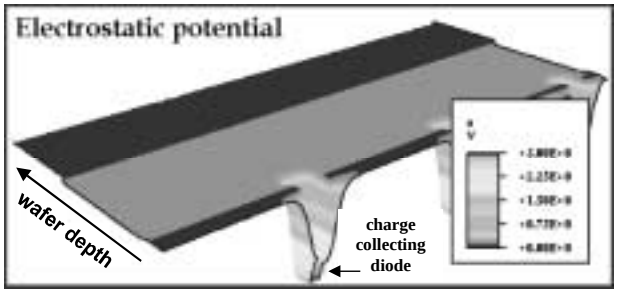

Figure 4: Electrical Potential around the central pixel diode and in the epitaxial layer. One clearly sees the potential well in which the charge carriers (electrons) can drift to the diode.

A. Charge Collection by Diffusion in the Epitaxial Layer

Fig. 4 shows quantitatively the electrostatic potential along the wafer and into the wafer depth with deep

minima at the position of the diodes and the shallow potential well, typical for a twin-tub CMOS-process. The height ΔV depends mainly on the different doping concentrations $N_{substrate}$ and $N_{epitaxial}$ and the operation temperature, $\Delta V = kT/q \ln(N_{substrate} / N_{epitaxial})$

The charge collection dynamics in the epitaxial layer and in the substrate has been simulated in detail. In one approach the ToSCA device simulator was used to calculate the electrostatic potential and then coupled to a three dimensional microscopic Monte Carlo programme to simulate the charge collection by diffusion following the random walk of the charge carriers at thermal velocities[5].

In order to have a complete three-dimensional treatment of the charge collection process and to profit from the use of advanced physical models, the commercially available simulation package ISE-TCAD[6] was used intensely. The simulation uses the approximate doping profiles kindly provided by the VLSI foundry for the epitaxial layer and substrate. A measurement of the doping profile indicates however an important transition region a few microns wide, which has not been included into the simulation. The charge distribution deposited by a minimum ionising particle is described by an analytical parameterisation and the charge collection process is obtained by numerically solving the drift-diffusion equations for the charge carriers (electrons).

In Fig. 5a,b the integrated charge collected is plotted as a function of time for the case of a one- and four-diode pixel, respectively. The particle crosses the pixel volume slightly off-centre and the three curves indicate the total collected charge within a group of one, four and nine pixels around the central one. As expected, the higher density of charge collecting points leads to a faster collection time in the case of the four-diode pixel structure. In this simulation the total charge collected is slightly over-estimated compared to newer calculations presented in the next section.

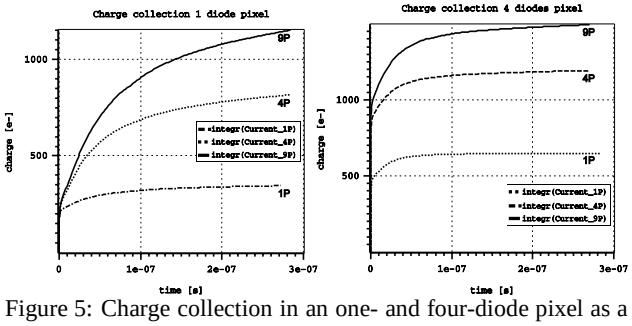

Figure 5: Charge collection in an one- and four-diode pixel as a function of time.

B. Contribution from the Substrate

In order to approximately disentangle the contribution from the substrate and the epitaxial layer, simulations were carried out treating the thickness of the epitaxial layer and the substrate as a parameter[7]. The results are presented in Fig. 6a,b, where the collected charge (90%) within a 3×3 pixel cluster is shown for different values of the thickness of epitaxial layer and substrate. The fast saturation in Fig. 6a of the collected charge demonstrates how the very short lifetime of the charge carriers in the substrate limits its contributing zone to about 5 μm thickness. Roughly between 150 and 200 electrons are collected from this zone which could be translated into a collection efficiency of about 40% for the substrate. This can be compared to an efficiency of about 80% for the epitaxial layer where nearly all of the generated electrons are being collected.

In contrast, as Fig. 6b shows, the charge collected increases continuously with the increase of the epitaxial layer thickness. However, the charge is smeared over more pixels by the diffusion process and the collection time also increases significantly for a 25 μm thick layer.

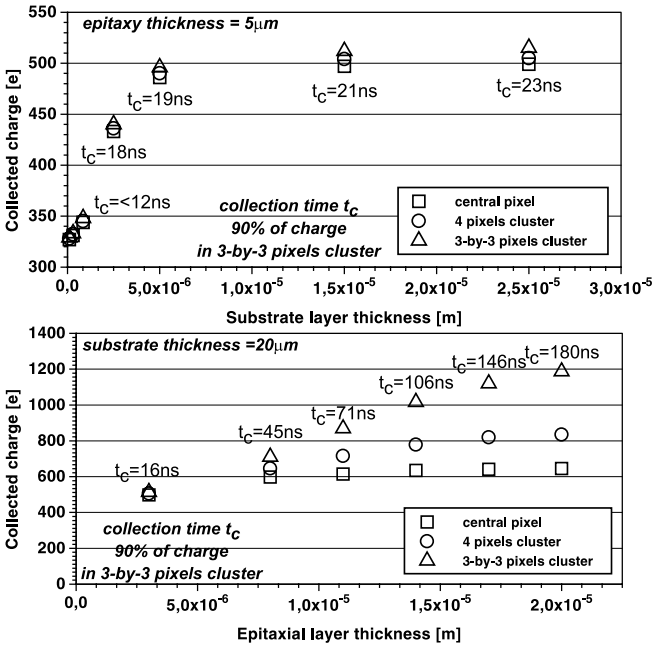

Figure 6: Charge collection as a function of substrate(a) and epitaxial(b) layer thickness.

It should be pointed out that these numbers are only of limited accuracy, as several assumptions in particular on the recombination processes in the substrate and the epitaxial layer are difficult to quantify precisely. Also the transition region of the doping profile not realistically simulated may alter some of the estimates given above. However, within an error band of 25% the contribution of the substrate and the epitaxial layer should be described correctly.

The results on the charge collection time scale obtained by simulations described above, where qualitatively confirmed with a measurement by an infra-read laser beam. A quantitative charge measurement and our calibration procedure using a soft x-ray source and particle beams is described in the next section.

V. Charge Calibration with Soft X-Rays from a ^{55}Fe Source

The conversion of soft x-rays from a ^{55}Fe source generates a very localized charge cluster in the silicon. This permits to measure the charge collection efficiency, if the location of the conversion is known or can be deduced otherwise. The 5.9 keV gammas from the iron source generate 1640 electron-hole pairs. Fig. 7 shows the collected charge of the MIMOSA chip for the case of the one-diode pixel. The first histogram contains only the charge of the central or the highest pixel of a reconstructed cluster with a main maximum at 82.5 ADC counts and a small second peak with only a few entries at 305 ADC counts, which is enlarged in the second histogram. The two lower histograms show how the main peak is shifted to higher values if the charge within a 3×3 or 5×5 cluster is analysed. This increase is just the expected growing charge reconstruction efficiency. The small peak of the one pixel histogram corresponds to a conversion point within the depletion layer of the diode, where 100% charge collection can be assumed. Using the value of 305 ADC counts for this peak, which equals the 1640 generated electrons, and comparing with the mean charge collected from a 3×3 or 5×5 cluster, a 75% and 85% average charge collection efficiency can be deduced for the sensitive volume, which is predominantly the epitaxial layer. This agrees fairly well with the simulation results discussed above (compare Fig. 6a and b).

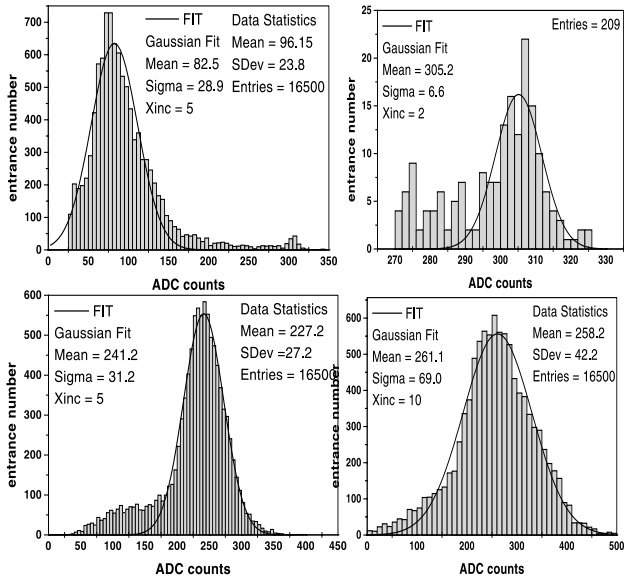

Figure 7: Charge collected in the central pixel of a cluster (top) and within a 3×3 and a 5×5 large area around the peak(bottom).

VI. Tests with Charged Particle Beams

The MIMOSA pixel chip has been tested with pion beams of 15 and 120 GeV/c at the PS and SPS accelerator at CERN[7]. A beam telescope[8] of eight planes of high precision silicon strip detectors was used to define the incoming particle trajectory and the intersection point with the MIMOSA detector. A pair of small scintillation counters provided the trigger for the data readout based on a VME-OS9 processor. The detector was operated around −10°C to reduce leakage currents in order to run with a very low reset frequency of only a few Hz.

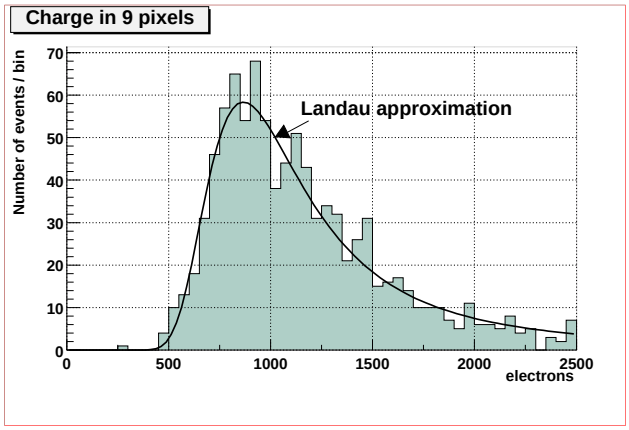

Figure 8: Cluster charge distribution calibrated in electrons for a 120 GeV/c pion beam

A cluster finding program reconstructed the charge deposited in the pixel matrix using the pixel with the highest signal to noise ratio as a seed for the algorithm. As an example we discuss in the following the one-diode matrix only. At the peak of the Landau distribution the reconstructed single cluster charge saturates above 1000 electrons for clusters where at least 13 pixels contribute. Fig. 8 shows the reconstructed cluster charge within an area of 3×3 pixels with about 900 collected electrons for the most probable energy loss which is in fair agreement with the simulation shown in Fig. 6b.

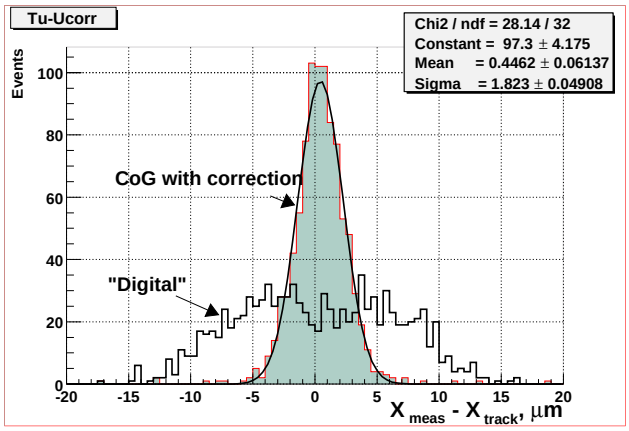

Figure 9: Spatial resolution obtained with the one-diode 20×20 micron wide pixels of MIMOSA I. The grey histogram uses the full analogue information including a correction for the finite size of the pixels, whereas the open histogram gives the resolution if a binary readout had been employed.

For this analysis the calibration obtained with the ^{55}Fe measurement was used. The average noise in a single pixel was found to be 12 ENC during the beam test, resulting in a signal to noise ratio of S/N=25 for the most

probable energy loss in a 3×3 matrix. This very good S/N ratio does not only allow a very high charged particle detection efficiency measured to be as good as 99%, but also allows to reach a very good spatial resolution.

Comparing the centre of gravity for the reconstructed clusters in the matrix with the intersection point of the reference track the results presented in Fig. 9 have been obtained. As explained in the figure caption, the good pulse height resolution of the detector allows pushing the spatial resolution beyond the range of an hypothetical binary readout, if a correction for the finite granularity of the matrix is used. A precision of better than 2 μm has been estimated.

In the four-diode pixel matrix the total, accumulated charge is about 20% higher, however the increased effective noise does more than neutralise this gain.

VII. Recent Developments of Mimosa

This year a second version of the circuit has been produced in a 0.35 μm CMOS process (5M+2P). The thickness of the epitaxial layer in this technology is only between four and five microns. The diode dimensions are $1.7\times1.7\ \mu m^2$ in this technology reducing its capacitance to only 1.65 fF. This decreases its noise contribution and can partially compensate the smaller charge which is available. First preliminary results within a particle beam indicate a similar good performance. Six matrices, each of 64×64 cells, were integrated on the same chip to test different geometries of the pixel matrix with respect to efficient charge collection and to test radiation hard layouts. The single-pixel read-out speed could be increased to be above 10 MHz. Furthermore, in one matrix the diode was replaced by a different active element, a Photo-FET, representing a first amplification stage already at the pixel level. Results will be available soon.

The collaboration considers it an important next step to proceed towards a large detector-like structure that has the potential to be used in a real experiment and which could prove its competitive potential. The fact that the sensitive detector volume is the epitaxial layer, continuous over the entire wafer, offers the interesting possibility of merging adjacent circuits on the wafer into one unique detector module, containing several tens of circuits. If all the readout electronics is placed on the lower circuit boundary, the chips could be effectively merged horizontally over the wafer. If the previous row of reticules placed above has its readout electronics sitting on the top boundary of the circuit, even two complete rows could be merged. Clearly this proposal depends crucially on a very high yield of individual circuits and on the cooperation of the foundry.

One of the greatest attractions for this novel device is the possibility to produce very thin vertex detectors with also small pixel sizes. This would be of extreme interest for the next generation of TeV-colliders. However, also possible upgrades of LHC detectors are complicated but interesting challenges: radiation hardness to several tens of Mrad, charge collection within a limited number of bunch crossings, high particle flux, resulting in large amounts of data which have to be kept until the arrival of the first level trigger and which have to be readout.

The necessary radiation robustness could by achieved using submicron technologies. The main difficulty will be to compromise between a small pixel size and the space for the on-pixel electronics necessary to cope with the large data flow at LHC. Pixels with several charge collecting diodes operating in parallel could allow larger pixel dimensions to accommodate the pixel-electronics and they could also serve to provide a sufficiently fast and efficient charge collection.

Clearly, embedding the proposed structure of a MAPS into the complexity of the present LHC pixel detectors is a challenging long-term project.

VIII. Acknowledgements:

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IX. References

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