# A BiCMOS discriminator interface for the SPD.

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*Abstract*

A prototype chip for the analogue readout of the SPD in the LHCb Calorimeter is presented. The chip has been designed using the 0.8µm-BiCMOS technology of AMS and optimised for minimum size and maximum performance at the required frequency of operation in LHC experiments. It consists of a dual structure formed by two integrators, two track and hold circuits, two substractors, two comparators and a multiplexer. The die size occupied by one discriminator circuit is approximately 1720 µm x 330 µm.

## I. INTRODUCTION

LHCb is dedicated experiment to study CP violation and other rare phenomena in B-meson decays at LHC (Large Hadron Collider at CERN). CP violation is one of the remaining open questions in experimental particle physics and cosmology. On the former field, its goal is perform an experimental precision test of the consistency of the Standard Model. On the later, CP violation is one of the three necessary conditions to generate matter-antimatter asymmetry, but Standard Model does not seem to be able to generate sufficient CP violation so that the universe could be dominated by matter as cosmology claims that it is.

LHCb [1] is a typical fixed target spectrometer. It consists of a vertex detector at the intersection point, a tracking system, RICH counters, a large-gap dipole magnet, a calorimeter system to measure particle energy and a muon system (figure 1). Modern particle detectors have to cope with very high rates of collisions, for LHC the bunch crossing clock is 40MHz, and with a very large

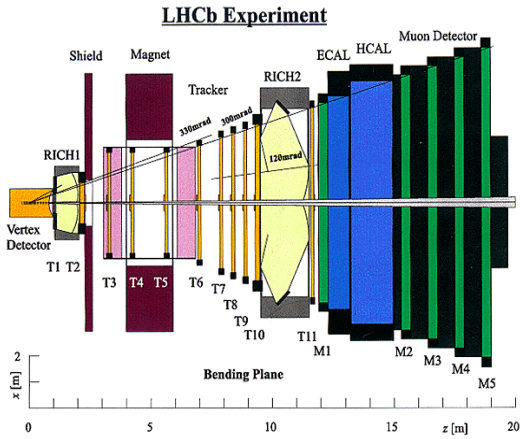


Figure 1: LHCb detector section view.

amount of subdetectors and sensors. About 949000 channels (from 1 to 12 bit of resolution, that means 87 KBytes in total) have to be processed each 25 ns. This implies that information rate is of 3.48TBytes/s. It is obvious that is not possible to record or study such amount of information, for this reason and to select "interesting events" (only at the 0.5% of events there is an useful decay to study CP violation) a trigger system is designed to discard non interesting event. This system is divided in 4 levels, each level using only partial information. First level, called L0 trigger, has to cope with an input rate of 40MHz, so it is a pure hardware processing system, the latency of the system is 4 µs and the output rate is 1MHz. L0 trigger selects particles with large transverse momentum, information provided by calorimeter and muon detectors, and has a pile-up veto. L1 trigger reconstructs partial tracks of particle and has

an output rate of 40KHz. After L2 and L3 trigger, implemented by software, the storage rate is 20Mbytes/s.

In the LHCb, the Scintillator Pad Detector (SPD) is placed just before the Preshower (PS) of the Electromagnetic Calorimeter (ECAL in figure 1). The SPD is designed to distinguish electrons and photons (ECAL and PS can not do it by themselves) at the L0 trigger level. It is a plastic scintillator layer, divided on 6000 cells of (4x4 cm at inner part and 12X12 at outer part cm). Charged particles will produce, and photons will not, ionisation on the scintillator. This ionization generates at the plastic scintillator blue light that is collected and converted in green light by Wave Length Shifting (WLS) fibre that is twisted inside the scintillator cell. This light is transmitted by a clear fibre to a electronic system which is placed on the upper on lower end of the ECAL structure. On the electronic system a 64 anode photomultiplier (Hamamatsu R7600-M64 [2]) converts the light in charge pulses. The analog circuit described here process the signal to determine if it corresponds to a photon or to an electron.

Several effects complicates the signal processing, the main difficulties are: energy "deposited" by photons and statistical signal features. Photons are not charged particles, therefore one should not expect detect them on SPD, nevertheless they do. Photons deposite energy through secondary processes like Compton effect or pair production. The energy spectra of photons (figure 2) shows that most photons do not deposite energy (large peak at zero), but there is a small tail overlapped on the electrons spectra (peak at 2 MeV) which can provoke misidentification. Hence, the analog processing should discriminate photons (background) and electrons (signal). Taken into account that signal has no real separation from background, there is, then, a compromise between trigger efficiency and wrong identification. In order to achieve the maximum efficiencies an individual channel calibration is needed to compensate tolerances of the detection system, like the gain fluctuation between the different channels of the photomultiplier which is of the order of 3. In our system such a calibration can only be performed by an on-line update and control of the discriminator threshold for each channel.

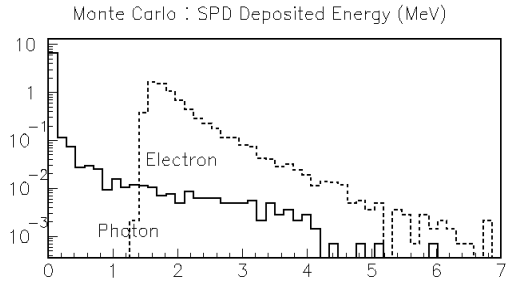


Figure 2: Normalised spectra of deposited energy (in MeV) by high energy photons and electrons obtained by MonteCarlo simulation.

The second problem is related to the statistical nature of a scintillator detector, and mainly to the desexcitation time of the WLS fibre. This kind of fibre captures a blue photon a emits a green one on a time that follows an exponential random distribution with a $\tau$ of about 10 ns. Finally this produces a random signal shape, we can see an example on figure 3. Studies performed by our colleagues of the "Laboratoire of Physique Corpusculaire" at Clermont-Ferrand [3] shows for Minimum Ionising Particle (MIP) a fluctuation of $\sigma$ = 50% on the total integral signal and also that only a 83 ± 13 % of signal is integrated in 25 ns because the rise time of the integral signal is 28.88 ± 7.3 ns. Therefore mean signal lasts more than the maximum integration time allowed: 25 ns (the bunch crossing period). This phenomena has two main consequences on the electronic design: a dual architecture is needed in order to do not have any dead time on integration reset and it will be very probable to have pile-up. Pile-up means that part of the signal of the event n is detected on the event *n+1*, and there is no way to distinguish from the signal detected on the event *n+1*. Although it can not be avoided it is possible an statistical compensation: a 17% of the integral signal of the event n is subtracted from the integral signal of event *n+1*.

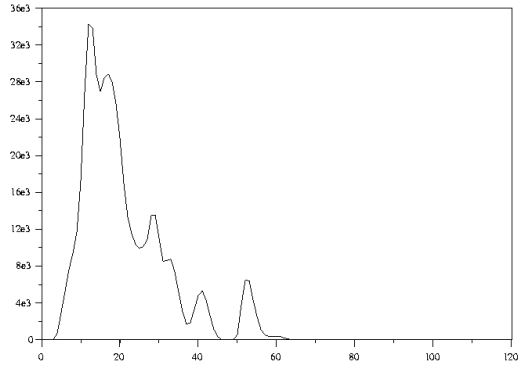

Figure 3: Example of MonteCarlo photomultiplier output signal. X axis: time in ns. Y axis: charge in electrons.

## II. DISCRIMINATOR INTERFACE

Because of the high frequency of the signals in the experiment (40MHz) and the large number of channels (6000), speed and cost are decisive. This mandates to make a minimum size design of each channel and use bipolar or BiCMOS technology. BiCMOS technology has the advantage that for analog circuits, bipolar devices offer a transconductance higher compared to MOS devices, leading to, for a given area, higher speed and gain. On the other hand, MOS transistors offer simple analog switches with zero dc offset voltage, high impedance charge storage nodes and, complemetary transistors.

The structure of the discriminator presented here is shown in figure 4a. In order to reduce noise the design is

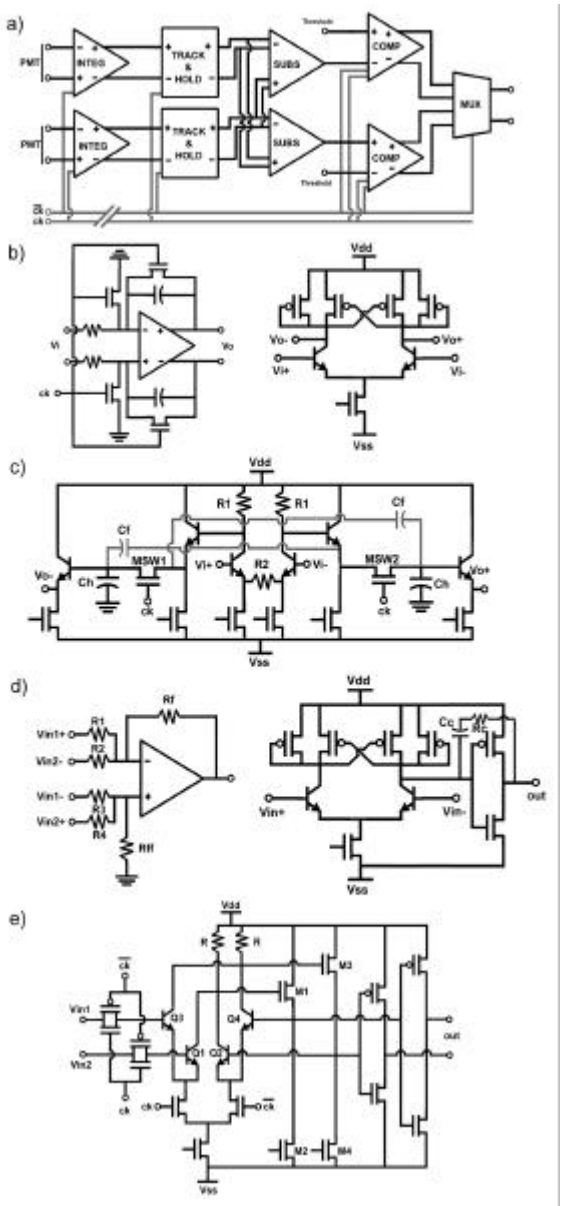


Figure 4: a) Structure of the discriminator circuit. b) Integrator (left) and differential amplifier used in the integrator circuit (right). c) Transistor-level schematic of the track and hold. d) Analog substractor (left) and single-ended amplifier for the substractor (right). e) Comparator circuit.

completely differential. Because of the jitter of the input signal and its non-reproducible shape, the signal coming from the photomultiplier has to be integrated rather than considering its maximum value [3]. So, the input device of the discriminator is an integrator circuit. On the other hand, as commented before, to avoid dead integration time (the integrator has to be reset between two consecutive integrations), a double channel has been chosen. Each channel of the discriminator is controlled by an opposite clock phase of period 50ns (the double of the bunch crossing frequency). Possible pile-up is corrected then by subtracting a factor $\alpha$=17% of the integrated signal in the clock *n* from the signal being integrated in the clock *n+1*. To do this, the signal integrated in the clock *n* has to be stored in a track and hold. After the subtraction has been performed, the signal is compared with the value established in the comparator. Finally, after the comparators, a multiplexer is added to select the channel from which the signal is read.

So, each channel of the discriminator is controlled by an opposite clock phase and consists on an integrator, a track and hold, a substractor and a comparator. All the blocks of the circuit are biased between +2.5V and –2.5V.

## III. BUILDING BLOCKS

The first block of the discriminator circuit is a continuous time integrator (figure 4b left). It is formed by a large bandwidth and high gain differential amplifier, and the integration capacitors and resistors. The nmos switches are included to control the integration-reset sequence. It is clear that integration is performed when the clock is high. The value of the capacitors and resistors is 300fF and 5K$\Omega$.

The structure of the differential amplifier used is presented in figure 4b (right). It consists of a differential bipolar pair with pmos active load. The crossed pmos transistors give the necessary path for current flow to allow high gain without degrading the large bandwidth obtained with the differential bipolar pair. Another advantage is that no compensation capacitors are needed because this amplifier is a single-stage one. Simulated data show a dc gain $A_v$= 52.7dB, a bandwidth $f_c$=1.38MHz, and a phasemargin PM=82.57º for unity gain frequency $f_u$=589MHz. The total current through the amplifier is 250$\mu$A.

The design of the track and hold block (T&H) is based on reference [4]. A fully differential architecture allows to reduce the typical artifacts of T&H circuits, i.e., pedestal (change in the output voltage during the transition from track to hold mode), drop rate (decrease of output voltage when in the hold mode), and feedthrough (influence of the input signal on the output in the hold mode). The two first are reduced as a consequence of the fully differential design, while the last needs additional compensation. An additional key point of the T&H is the need of only one clock phase, thus being reduced problems related to clock generation and routing.

The scheme of the T&H presented here is shown in figure 4c. As in reference [4], it consists on an input buffer of unity gain, nmos switches, hold capacitors ($C_h$ in figure 4c) and output buffers. With respect to reference [4], in the present design, the bipolar switch has been replaced by an nmos switch in order to increase the possible range of the input signal and to simplify the design. Moreover, the differential input buffer is only formed by a degenerated differential pair (two bipolar transistors and the resistor R2) loaded with resistors R1. The ratio R2=2R1 gives the unity gain condition of the input buffer needed for a track and hold application.

Usually the load of each bipolar transistor of the differential pair is a series connection of a diode and a resistor in order to obtain high linearity. For our application the diodes can be omitted. Finally, hold mode feedthrough has been compensated by a feedthrough capacitor ($C_f$) connected as shown in figure 4c.

The operation of the T&H is as follows. During ck=high the T&H is in the track mode, i.e., switches MSW1 and MSW2 are on and $C_h$ is being charged. When ck=low, the T&H is in the hold mode and there is no connection between the emitter follower drived by the input buffer and the hold capacitor. In this mode the charge in the hold capacitor determines the voltage at the base of the emitter follower output buffer and, thus, the output voltage.

The values used in this T&H are $C_h$=2pF, R1=3KΩ, R2=2R1=6KΩ, and $C_f$=23fF. The current flowing through the input buffer and through the two emitter followers is 250μA. With these values the simulated characteristics of the T&H for an input signal of 1V are a pedestal of 3.1mV, drop rate DR=80μV/ns, and no hold mode feedthrough. A rail-to-rail input range can be obtained by adjusting the resistances and the current in the input buffer. Between the input signal and the output there is always a delay of 1.6ns, corresponding mainly to the intrinsic delay of the input buffer. The T&H can operate up to sampling frequencies ~500MHz.

The structure of the analog substractor is presented in figure 4d (left). It is needed in this block to convert the differential signal coming from the T&H to single ended signal. Thus, the substractor is composed by four input resistances, two feedback resistances and, a single-ended amplifier. The structure of the amplifier (figure 4d right) is very similar to that presented in figure 4b (right), but an output buffer has been included in one of the outputs. In order to compensate the coupling between the input differential stage and the inverting output stage, a series RC network ($R_c$=0.5KΩ and $C_c$=500fF) across the second gain stage provides the frequency compensation. The simulated characteristics of the amplifier are a dc gain $A_v$= 61.8dB, a bandwidth $f_c$=493.9KHz, and a phasemargin PM=52.14º for unity gain frequency $f_u$=539MHz.

The operation to be made is $S=(V_{in2+}-V_{in2-})-\alpha(V_{in1+}-V_{in1-})$. In order to take into account the factor $\alpha\approx17\%$ the values of the resistors in the circuit of figure 9 are $R_f=R_{ff}=R_2=R_4=5k\Omega$, and $R_1=R_3=29.5K\Omega$.

The schematic of the comparator circuit is shown in figure 4e. An additional input preamplifier can improve the performance of the comparator but has not been implemented because it is not needed for this application.

The core of the comparator is the well known latched comparator [5]. The latch is clocked by means of a MOS differential pair. When clock=high the circuit is in the acquisition phase. In this case the latched comparator behaves simply as a differential amplifier (Q1 and Q3 loaded with resistances R) for the differential input $V_{in1}$-$V_{in2}$. When ck=low the comparator is in the regeneration phase. In this case Q1 and Q3 are off and Q2 and Q4 are conducting. Again Q2 and Q4 together with the load resistances, form a differential pair. It is in this phase when the comparator exploits the positive feedback to reach the desired output levels. In the positive feedback path there is a buffer formed by the MOS transistors M1 and M2 for Q2 and M3 and M4 for Q4. The two output CMOS inverters appearing in figure 4e are scaled in order that the output levels are ±2.5V.

The current flowing in the lached comparator and in the buffers is 120μA. The propagation time of the latched comparator is only of ~2ns, which corresponds to a maximum operation frequency of 500MHz. Because simulation data are only available it has no meaning to talk about input offset and maximum resolution.

The final block of the discriminator is a differential 2:1 multiplexer circuit with open drain outputs. There are not special demands on the characteristics of this circuit as their inputs result from a previous latch.

The die size of the functional blocks of the discriminator circuit are presented in table I. The design was sent to the AMS foundry on March 2000.

Table I: Die size occupied by each block. The discriminator size includes the current sources, the clock generator circuit, and interconnections between blocks.

| Block | Die size |
|---|---|
| ***Integrator*** | 185μm x 100μm |
| ***Substractor*** | 275μm x 200μm |
| ***Track & Hold*** | 205μm x 120μm |
| ***Comparator*** | 150μm x 152μm |
| ***Multiplexer*** | 90μm x 110μm |
| ***Discriminator*** | 1720μm x 330μm |

## IV. RESULTS AND CONCLUSION

The complete circuit has been simulated using Spectre as electrical simulator. Figure 8 shows an example of the operation of the discriminator circuit. *Clock* signal is the 20 MHz (half the bunch crossing frequency) channel clock which gates the integrators for 25 ns and controls the internal switches. When *Clock* is high the sequence of signal processing works as follows:

· *Integrator 1* is integrating the input signal and *Integrator 2* is discharging its feedback capacitors.

· *Track & hold 1* follows *Integrator 1* signal and *Track & hold 2* holds *Integrator 2* signal.

· The output signal of *Substractor 1* (*sum 1*) is the input signal of *Comparator 1*, and the value of this signal is: "*Track* & *hold* 1" - 0.17 * "*Track* & *hold* 2".

· *Comparator 1* compares its input signal (*sum 1*) with *Threshold 1*, giving at the output (*Comparator 1)* the transient result of the comparison which will be latched on the next *Clock* period (when this clock falls to the low level).

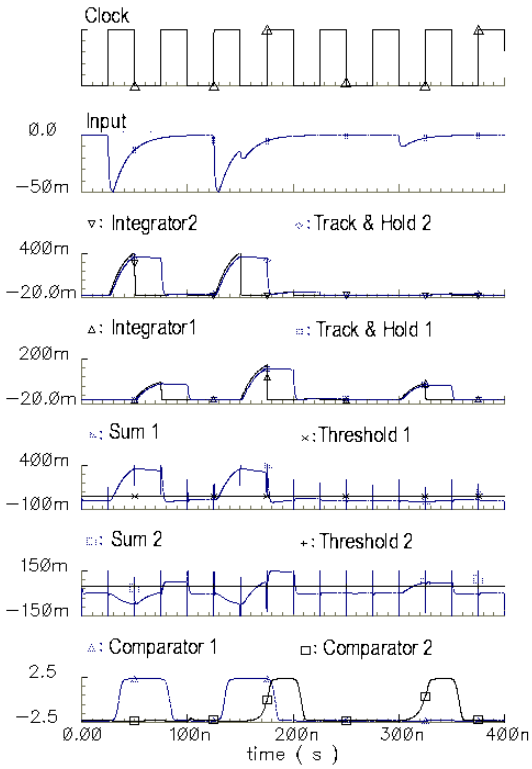


Figure 5: Simulation of the complete discriminator.

· *Comparator 2* is in ”latch” operation holding at his output the result of the previous comparison, which is transmitted to the output of the channel through the multiplexer.

A symmetric situation occurs when *Clock* is low.

On this simulation we combine two signals that corresponds to the opposite tails of the statistical fluctuation of the PMT signal. The conditions to define PMT signal are: 1 MIP signal is equivalent to about 35 photoelectrons, the high voltage is set to 900 V and the load resistor at the output of the tube is 100. These signals are approximated by exponential pulses of 50 mV and 10 mV with a time constant of about 12 ns. Threshold is set to detect signals of the smallest amplitude. Three different situations are simulated:

1. At t=25 ns (period 2 2), a pulse of maximum amplitude is integrated. After following all the processing chain a high level on the *Comparator 1* output (period 3) indicates that a charged particle has been detected. Therefore, the delay of the processing chain is one cycle. Although the amplitude of the tail of the signal at period 3 is high (*Integrator 2* signal at period 3) the compensation of 17 % of the signal hold at *Track & Hold 1* output avoids that input *Comparator 2* signal (*Sum 2*signal at period 3) exceeds *threshold 2.* The tail is not taken as new 1 MIP signal although its integral value (*Integrator 2* signal at period 3) is of the same order of the integral (*Integrator 2* signal at period 13) of the 10 mV signal that has been used to adjust Thresholds.

2. At t=125 ns (period 6) we have a 50 mV amplitude pulse and on the next bunch crossing (period 7) (half of *Clock* signal period) a pulse of 10 mV amplitude is overlapped to the tail of the large one. Both signals are detected: the big one at the *Comparator 1* output at period 7 and the small one at the *Comparator 2* output at period 8.

3. At t=300 ns (period 13) a 10 mV small amplitude pulse arrives and it is detected.

As a conclusion, the proposed systems seems to full-fill the initial specifications demanded in the LHCb experiment.

## ACKNOWLEDGEMENTS

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