View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by CERN Document Server

Custom chips developed for the trigger/readout system of the ATLAS end-cap muon chambers

Kano,H.*, Fukunaga,C.
Tokyo Metropolitan University, 1-1 Minami-Osawa,Hachioji 192-0397
Ikeno,M., Sasaki,O.
KEK, 1-1 Oho, Tsukuba 305-0801
Ichimiya,R., Kurashige,H.
Kobe University,1-1 Rokkodai-cho,Nada,Kobe 657-8501
Nishida,S., Sakamoto,H.
Kyoto University,Kitashirakawa-Oiwake-cho,Sakyo,Kyoto 606-8502
Hasegawa,Y.
Shinsyu University,3-1-1 Asahi,Matsumoto,390-8621
Hasuko,K., Katori,Y., Kobayashi,T., Niki,T.,Toya,D.
University of Tokyo,7-3-1 Hongo,Bunkyo-ku,Tokyo 113-8654
*Correspondent: ka8no@comp.metro-u.ac.jp

Abstract

Three custom ASICs are now being developed for the trigger/readout system of the ATLAS end-cap muon chambers. Each chip is the master component in three subparts of an on-detector system. Beside the standard circuitry as an ATLAS subsystem, several implementations have been devised in each chip, which are required from various physical and boundary conditions as an electronics system for the end-cap muon chambers. We discuss the implementation of the level 1 muon identification logic as well as these customarily developed data handling technology on ASICs.

I. INTRODUCTION

In the ATLAS experiment [1], we construct a level 1 trigger system (LVL1) [2] based on two signal sources of the calorimeters, and the muon detectors. The huge number of detector channels must be processed within a predefined time of about 1μs in order to establish a trigger signal, and thus various methods for parallel and distributed processing must be taken for this purpose.

Since we have to process large numbers of channels and install many identical circuits for parallel processing, an idea to implement fundamental parts of the systems into ICs is quite natural. Actually several ICs are designed and developed for both calorimeter and muon LVL1 trigger systems. Functionalities of some prototype chips are already evaluated in test benches. Development of custom ICs will have also an advantage to control own radiation hardness or tolerance condition relatively easily.

ATLAS has two independent sub-detectors for generation of muon triggers. One is Resistive Plate Chambers (RPC) for the barrel region and the other one is Thin Gap Chambers (TGC) for the end-cap region [3]. Several ICs will be implemented in the trigger/readout electronics systems for both muon sub-detectors independently.

Muon end-cap trigger system will foresee to have three kinds of custom chips. These ICs will be installed in a system, which will be mounted directly on a chamber surface because of a signal processing condition. Since ATLAS TGC has not enough strength to bear heavy electronics stuff, we must reduce weight and power consumption of the system as much as possible in order to make a light and compact system. Thus we have to confine almost all the functional blocks except power supply into the custom chips. A unit of system must be divided into several partitions, and we actually plan to install one IC on each partition. Another issue for muon end-cap IC design is, hence, system interconnections among partitions, i.e. For a trigger information exchange, rapid and efficient data transfer must be done from an IC to other. In this paper we discuss the design and development of three custom ICs. We report how to realize various boundary conditions or issues in the design, some of which are special for our purposes in the following sections.

Although in the section 2 we discuss an overview of muon end-cap trigger and readout system, Ref.4 should be referred for more detailed discussion about the system. In section 3, we discuss the ICs that are now developing. And finally we discuss the problems and issues currently we have for the development as well as actual status of the IC production in section 4.

II. END-CAP MUON TRIGGER ELECTRONICS

ATLAS has two sub-detector systems of so-called RPC and TGC for the LVL1 muon trigger. RPC covers the barrel region ($\eta < 1.05$) and TGC covers the end-cap region ($1.05 \leq \eta < 2.70$). Although the ultimate purpose of two sub-detectors is the same and is to provide a highly efficient muon trigger of• p_T greater than 6 GeV/c, we construct two independent trigger and readout (TDAQ) systems. In this section we discuss the overview of end-cap muon TDAQ system.

Triplet and doublet chamber systems of TGC are put at the both edges of the ATLAS detector 13 and 14.5m away from the interaction point. Inner and outer radii of a TGC end-cap disc are approximately 2m and 12m. Anode wires and strips sense a track entered in a chamber. Wires are arranged in the

azimuthal direction and provide signals for r, while cathode strips orthogonal to the wires provide signals for ϕ information. Anode wires are ganged in a group with six to twenty wires. A wire group, thus, covers 11 to 36mm of r-region. The width of a strip is 4mrad, and 8mrad for forward region of $\eta < 1.92$. Signals for both wires and strips are amplified, discriminated and shaped through our custom ASD chips [5]. Binary information for hits is supplied to upper stream of the TDAQ system.

Low p_T tracks ($p_T \geq 6$ GeV/c) will be identified with coincidence conditions to signals of either the triplet or the doublet solely. High p_T tracks ($p_T \geq 20$ GeV/c) will be identified with the low p_T results of both the triplet and doublet.

The low p_T coincidence conditions for the triplet are 2-out-of-3 logic for wire signals and 1-out-of-2 (OR) logic for strip ones. The trigger conditions of both wires and strips for the doublet low p_T and overall high p_T tracks are taken algorithmically the same one, and that we realize it with a coincidence matrix (CM) technique.

The CM operation is performed with a signal matching of a pivot plane (which is the outer most plane (chamber)) and a reference plane. A virtual line is extrapolated from a signal location on the pivot plane to the interaction point. If signal candidates are found in a neighborhood (window) around a intersecting point of the extrapolated line on the reference plane, a trigger condition is considered as fulfilled. For implementation of this idea, we assume a matrix in which a signal coordinate of the pivot (reference) assigns the row (column) index. Two signals specify an element in the matrix. Then if the distance of the element from the closest diagonal element is within a certain tolerance, we regard two signals of the row and column as the trace of a track. This distance indicates the displacement (Δ) of a coordinate between two planes.

Based on the low-p_T trigger information, we also try to find high p_T tracks with the same CM technique. The pivot and reference plane in this case are the doublet and the triplet, respectively. With this high p_T coincidence operation, r, ϕ, Δr and $\Delta\phi$ values are re-evaluated independently. The information taken with two stage trigger is sent to the sector logic (SL) installed in USA15. The SL makes merging the information of r and ϕ to reconstruct tracks in space and selects several highest p_T tracks. The SL calculates the absolute r,ϕ coordinates of final track candidates. The resulting information of the SL is then sent to the Muon Central Trigger Processor Interface (MUCTPI), which is a part of the ATLAS LVL1 central processing facility. The total latency of the system is estimated as 1.20μs.

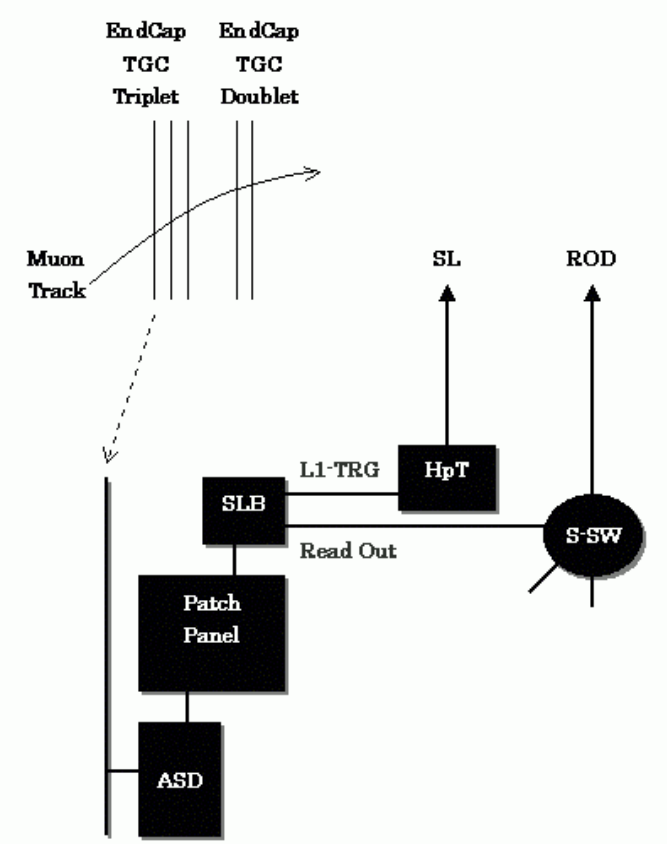


Figure 1: Overview of on detector party of Muon End Cap Trigger and Readout system

The physical realization of an on-detector part of the total system is illustrated in Fig.1. A unit of the on-detector part comprises three parts: a patch panel (PP), a slave board (SLB), and hi-pT(HpT) board. ASD processed signals are input to a PP where the bunch crossing identification will be done, and these synchronized signals are further sent to an SLB which has two-fold tasks, one is to operate the coincidence logic for low p_T track triggers and another one is to process hit information as usual read-out data à la ATLAS DAQ using a level 1 buffer and a derandomizer [6]. The read out data will be sent to an ROD (Read Out Driver) via a star switch system (SSW) [7] with its own hardware protocol. The ROD is dedicated for the end-cap muon data processing. The data once stored in this system will be sent to the central DAQ read out buffer. The trigger results processed by the SLB are transferred to an HpT board. The HpT board performs the coincidence matrix operation for both wires and strips for high p_T track identification. While a PP and SLBs (two SLBs are needed to process one PP) are put together closely and attach on the back of a chamber, an HpT board will be away about 15m from an SLB and put on the outer rim of a chamber.

Every board of a PP, an SLB and HpT has an independent IC, and the task of each board is almost confined in a single chip. The detailed functionality and characteristics of each chip will be discussed in the next section.

III. DEVELOPED ICS

A. Patch Panel ASIC (PPIC)

A patch panel (PP) has two facilities; a CAN bus node for DCS (Detector Control System) operation and an ASD signal receiver and adjuster for TDAQ processing. As a TDAQ processor, utilizing signals of encoded TTCrx signals and hit data (pattern) from ASD boards, a PP outputs delay adjusted and bunch identified ASD signals, modified or unmodified TTCrx signals, and test pulses for ASD timing adjustment.

Most of the TDAQ tasks are put into an IC of so-called PPIC. The hit signals from an ASD board are modified in the IC as

1. converted from LVDS level to TTL,
2. adjusted delay timing with precision less than 1ns,
3. synchronized with independently delay adjusted bunch crossing signal (bunch crossing identification; BCID), and
4. output with single ended TTL for further processing in an SLB.

A PPIC has also other facilities to adjust phase of received TTCrx clock (bunch cross signal) with the precision less than 1ns, and to generate test pulses and provide them for ASD boards in order to calibrate signal delay timing of a path from ASD output to input of the BCID block in PPIC.

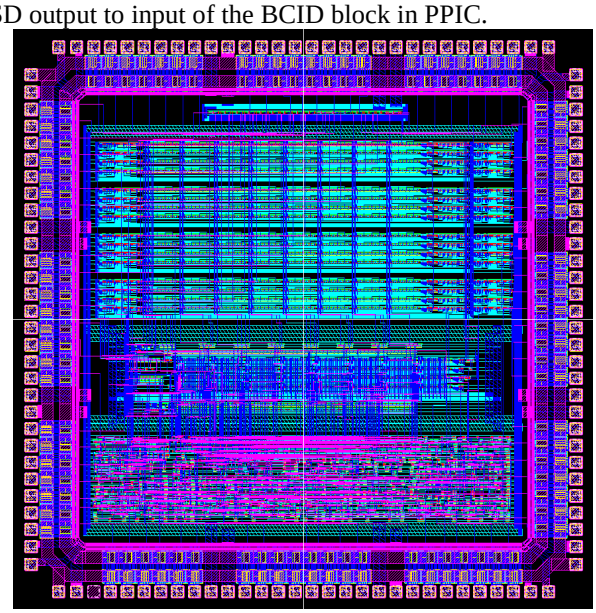


Figure 2: The mask pattern of a PPIC

As described above, main task of PPIC for TDAQ is timing adjustment for both ASD input hit signals and bunch crossing signal of TTCrx. The precise delay control for these signals are indispensable to synchronize the hit signals over the whole TGC TDAQ system. Hence a PPIC implements the sub-nanosecond delay controls for both timing and hit signals using a DLL circuit. The detailed strategy for the timing adjustment for not only a PPIC but also the overall system specific for TGC TDAQ system is reported in ref. 8. Fig.2 shows a mask pattern of a PPIC latest fabricated (prototype -1). In the upper half of the core of the mask pattern shown in the figure, we can find DLL blocks for total 16 channel ASD inputs. The timing of 16 channels are controlled with 780ps accuracy.

B. Slave Board ASIC (SLBIC)

Two SLBs are directly connected to a PP. An SLBIC is a core processor of an SLB and has also almost all functions which an SLB should hold. Only serializers for output are put outside the IC.

Input to the IC are bunch crossing synchronized hit patterns of either wires or strips. The IC has two functional blocks;

1. to identify low p_T muon tracks using hit patterns of the triplet or the doublet exclusively, and
2. to readout hit and trigger information with the ATLAS standard DAQ chain of a level 1 buffer and a derandomizer.

In the following subsections, description of the blocks are given.

1) Trigger Block

We can handle total four different trigger schemes with one IC by supplying signals to select wire/strip and triplet/doublet to corresponding external pins. Characteristics of these triggers, number of input channels, covered length by an SLBIC in actual TGC space are given in Table 1.

TGC	Hit	Input	trigger	Covered length
doublet	wire	88x72	CM	400 - 1500mm
doublet	strip	64x64	CM	1900mm($\eta \geq 1.92$) 3800mm ($\eta < 1.92$)
triplet	wire	36+36+36	2-out-of-3	400mm
triplet	strip	32+32	1-out-of-2 (OR)	1650mm($\eta \geq 1.92$) 3300mm ($\eta < 1.92$)

Table 1: Covered length for input hit patterns to an SLBIC with the trigger scheme. CM means Coincidence Matrix

Fig.3 shows a functional block diagram around a CM of the doublet. The block structure is common for both wire and strip inputs. Input hit patterns of a pivot and reference planes are matched in the matrix block. The matrix block consists of two identical blocks. Track candidates are selected from each block independently. The displacement information (Δr or $\Delta\phi$) of matched track candidates are sent to a primary encoder where a track with the highest p_T is selected in each block. Thus two tracks are finally output from an IC. The result of the primary encoder is fed back to the matrix block, and r or ϕ of the corresponding track measured at the pivot plane is sent to the decluster block. If hits are distributed over several wires or strips, only one of the central point is output. The displacement data (Δr or $\Delta\phi$) 5 bit and coordinate data 4 bit are packed in a 9 bit as a track data.

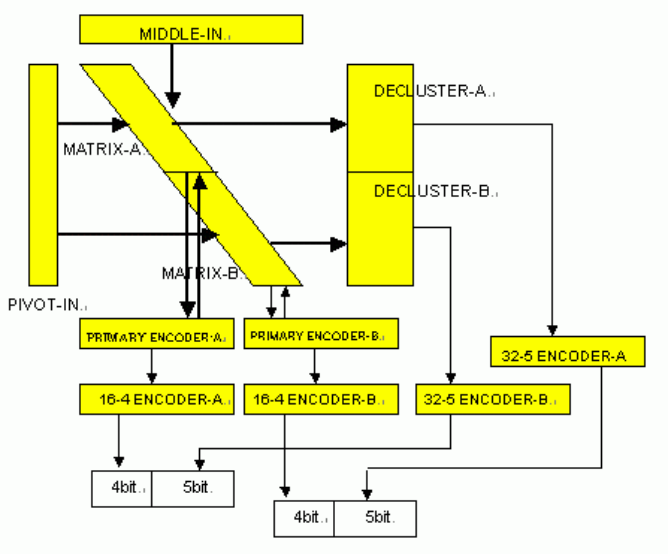


Figure 3: Block diagram of SLBIC Coincidence Matrix

Triplet wire (strip) trigger part inputs 36 (32) channels from every (two out of three) plane(s) and forms 108 (64) input blocks. A block has a logic to make a trigger if any two (one) from total three (two) channels contain(s) hit signals. r,ϕ of maximum three (two) track candidates which satisfy this condition are output. Since only inner and outer planes of the triplet has strip sensors, we have to form a trigger logic with two instead of three for strip signals. Because an SLBIC implements two identical trigger logics for the triplet strip coincidence, r,ϕ of total four candidates are output from an IC.

2) Readout Block

The data path from a PP input has two branches. While one is going to the trigger block, the another one is connected to the readout block. The specification of this block is followed the standard scheme of the ATLAS DAQ [6]. The block comprises mainly two sub-blocks of an level 1 buffer and a derandomizer. Input hit patterns, the trigger block output which are to be also sent to a HpT board and bunch crossing number are all input to the level 1 buffer and kept stored in the buffer during the trigger latency of about 2.5μs. The buffer is a pipe line memory of which the number can be programmatically adjustable with the latency.

The data stored in the buffer is then copied to a derandomizer if the corresponding event is marked as the LVL1 accepted. This buffer is an FIFO with depth of 16, and used to just an interface buffer for the next processing stage. When the data are copied in this buffer, the LVL1trigger number (event number) is also added in the event record. The data just one bunch before and after of the L1A event are also put in the derandomizer.

The data are then converted to the so called local slave link protocol which consists of four lines of a clock, synch, and 2 bit data [7] in the IC. At this stage the data are output from the chip. Then data are serialized and converted to LVDS and are sent eventually to an SSW with the category 5 cable.

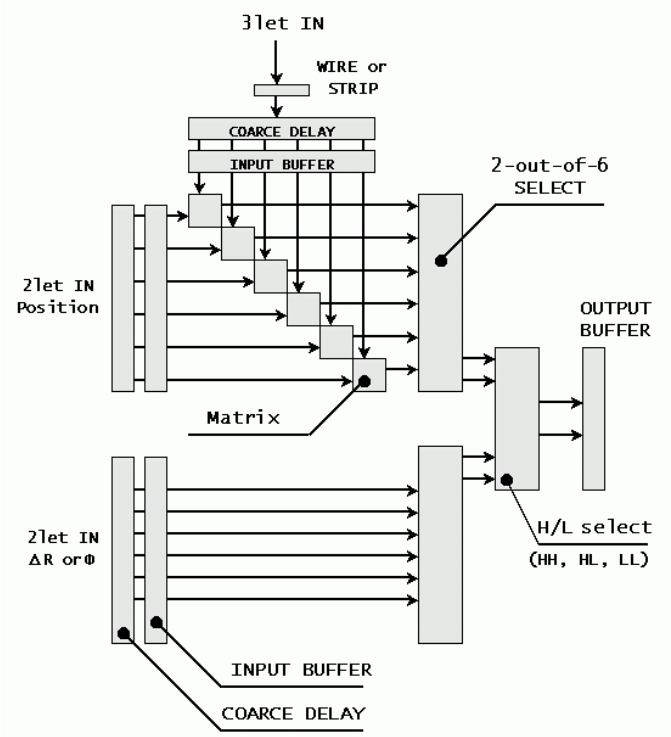
C. Hi-pT Board IC (HpTIC)

While PPs and SLBs are attached to the surface of a TGC directly, HpT boards are put as a 9U VME module in a crate which is installed at the outer rim of a TGC. The distance between an SLB and a HpT crate will be about 7,8m. An SLB and HpT are connected with 15m length category 5 cable with LVDS, which is the same manner as the data transmission of the readout. A core IC of the board, HpTIC contains again almost all essential tasks required for an HpT board. Functions which are put outside of the IC on a board are input/output LVDS deserializers and serializers with level or optical converters.

The IC processes coordinate data (r or ϕ) which are sent from SLBs to recognize High p_T tracks of $p_T \geq 20$ GeV/c as is inferred from the name. One HpTIC accepts the hit information from maximum three SLBs (four for triplet wire case). The recognition of a track is performed in principle with the same algorithm as implemented in an SLBIC for a low p_T trigger with the doublet. For HpTIC, since a track matching is done with both triplet and doublet TGC systems, the triplet hit pattern specifies the column, and the doublet one specifies the row index of the matrix respectively. An IC can cope two inputs of wires or strips by supplying an external signal. The block diagram of an IC is shown in Fig.4.

From information supplied from SLBs, position data (r or ϕ) for both the doublet and triplet are input to the Matrix block which has partitioned in six independent blocks. A block consists of a hit detector (coincidence logic) and a primary encoder so that only a track candidate with the highest p_T is output from each block (total at most six for an IC). In the block of 2-out-of-6 as indicated in Fig.4, two highest p_T tracks are selected from six candidates in order to compact a data volume to be sent over long distance to the SL. This data compress will not introduce against any trigger bias because it is rare to find more than two true muon candidates in an HpTIC according to a trigger simulation study. This 2-out-of-6 blocks has been optimized with special attention for logic design to reduce processing time as small as possible. We found time consumption for this block as 3.5 ns from design simulation while a conventional double stage primary encoder should take at least two clocks (50ns).

The displacement data of Δr or Δϕ from SLBs are simply passed towards the 2-out-of-6 block. These data are only output when no high p_T candidate is found otherwise an HpTIC adopts own displacement value found in its CM.



Fgure4: The whole block diagram of HpTIC

IV. DEVELOPMENT STATUS AND DISCUSSIONS

We have fabricated twice the prototype PPIC (-2 and -1). The technology we have used is 0.6μm full CMOS with full custom process. The prototype-2 has installed only DLL based delay adjustment block. The purpose for this fabrication is to check how accurately actual DLL in an IC reproduce the SPICE simulation. The delay time adjustment is done by control voltage. We found discrepancy between measurement and SPICE simulation for voltage dependence of delay time for prototype-2.

Then the prototype-1 has been fabricated with full specification with the same technology. Logic scale of this IC was estimated as about 10K gates. Prototype-1 has been then carefully designed the layout of DLL. But since we made a simple logic bug in the control block of DLL, we could not re-evaluate the characteristics, although other blocks of the IC have been confirmed to work. The next chip of prototype-0 which fix the bug will be ready by October,2000.

HpTIC has been fabricated for prototyp-1with 0.6μm 9x9mm full custom CMOS process. Number of gates is about 20K. Almost all logic components has been tested for this prototype-1 and confirmed their operation. Total processing time from input to output takes two clocks. Since buffering of data at input and output anyway consumes two clocks, this time means not more than a few ns is spent in the chip. The next fabrication (prototype 0) will be done with 0.35μm 6x6mm CMOS gate array process for the same circuit with small refinement. An IC with this gate array technology will consume lower power and be built with lower cost and thus appropriate for mass production

We have not fabricated the full specification of SLBIC yet. We have so far separately designed the trigger and readout blocks. We will merge two designs and will submit for the prottype-1 fabrication till end of 2000. Since logic scale is relatively large and is 200K gates, and at least 230 pins are needed for external I/O pins, choice of technology or device for fabrication of this IC is limited. We are currently excogitating the best suitable fabrication process.

These ICs will suffer radiation damage but level of total dose or neutron fluence will not be anticipated as so serious. Hence we will not apply any radiation tolerant technology for IC production. We install fault-tolerant register access circuits especially in PPIC to avoid single event upset (SEU) effect, which we estimate the occurrence of once/day.

Prototype 0 of all three ICs will be ready by summer,2001.

REFRERNCES

[1] ATLAS group, ATLAS Technical Proposal, CERN/LHCC/94-43 (1994)

[2] ATLAS Level 1 Trigger group, ATLAS First-Level Trigger Technical Design Report, CERN/LHCC/98-12 (1998)

[3] ATLAS Muon group, ATLAS Muon Technical Design Report, CERN/LHCC/97-22 (1997)

[4] K.Hasuko et al., “First-Level End-Cap Muon Trigger System for ATLAS”, presentation in this conference.

[5] O.Sasaki and M.Yoshida.,” ASD IC for the thin gap chamber in the ATLAS experiment”,IEEE TNS Vol.46 (1999) 1871, and
http://online.kek.jp/~sosamu/ASD-PRR.pdf

[6] ATLAS TDAQ steering group, “ATLAS Trigger & DAQ Interfaces with Front-End systems Requirement Document”, ATLAS Internal Note DAQ-NO-103, June 1998

[7] H.Sakamoto et al., “A Star Switch Readout Architecture for ATLAS Muon TGC”, proceedings of 4th LEB workshop, Rome, Italy, 1998, pp280-284

[8] K.Hasuko et al., “Strategy for Timing Adjustment of ATLAS End-cap/Forward Muon Trigger System”, proceedings of 5th LEB workshop, Snowmass/Aspen, Co., USA, 1999, pp.331-335.