Development of a 24 ch TDC LSI for the ATLAS Muon Detector

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Abstract

A prototype TDC LSI for the ATLAS precision muon tracker (MDT) has been developed. The LSI was processed in a 0.3 µm CMOS Gate-Array technology. It contains full functionality required in the final TDC.

To get a high resolution around 300 ps, an asymmetric ring oscillator and a PLL circuit are used. All the I/O signals, which are active during measurement, have LVDS interfaces. A JTAG interface is used for boundary scan and internal register setup. All the memory and control bits have parity bits so that a SEU can be detected. Radiation tolerance for Gamma ray and Neutron are also confirmed.

I. Introduction

ATLAS precision muon tracker (MDT) requires high-resolution, low-power and radiation-tolerant TDC LSIs (called AMT: ATLAS Muon TDC). Total number of TDC channels is about 370 kch.

To study basic circuit elements and radiation tolerance, a test element group chip (AMT-TEG) was fabricated in 1999 and reported in the last LEB workshop [1]. After the success of the AMT-TEG chip, we have developed a prototype chip (AMT-1) which has full functionality for the experiment. Here we report about the design and test results of the AMT-1 chip. System tests with front-end chip, chamber and readout modules are being scheduled.

AMT-1 chip was processed in a 0.3 µm CMOS Gate-Array technology (Toshiba TC220G). It contains 24 input channels, 256 words level 1 buffer, 8 words trigger FIFO and 64 words readout FIFO. It also includes trigger-matching circuit, which selects data according to the trigger ID. The selected data are transferred through 40~80 Mbps serial lines with DS-Link protocol.

To get a high resolution and stable operation, an asymmetric ring oscillator and a Phase Locked Loop (PLL) circuit are used. All the input and output signals which are active during measurement has LVDS interfaces. A JTAG interface is used for boundary scan and internal register setup. Built-In Self-Test for memories is also activated through the JTAG interface. All the memory and control bits have parity bits so that a Single Event Upset can be detected.

Although the technology is gate-array, we have made intensive analog simulation and paid much attention to cell layout to achieve a sub-nano second timing resolution. Several macro cells are developed for time critical and analog parts. Careful floor planning are done to minimize route of the time critical signals.

Photograph of the AMT-1 chips is shown in Fig. 1. The chip is packaged in a 144-pin plastic QFP with 0.5 mm pin pitch and about 110k gates are used.

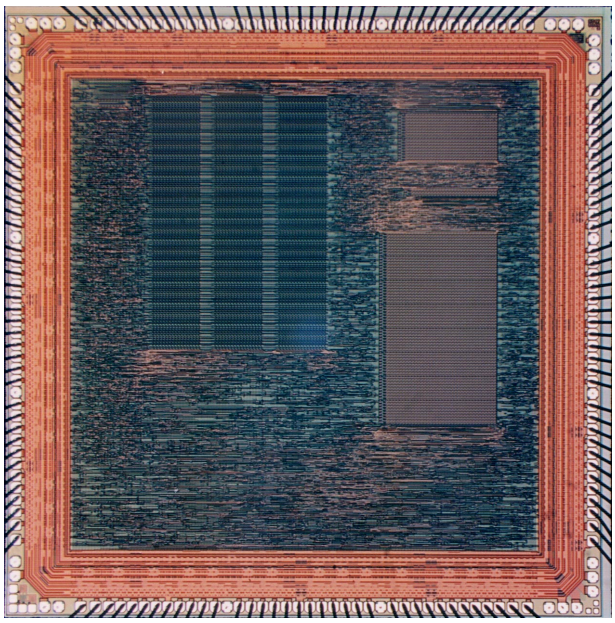

Fig. 1 Photograph of the AMT-1 chip. The die size is about 6 mm by 6 mm.

II. MDT Front-End Electronics

Block diagram of the MDT front-end electronics is shown in Fig. 2. Three ASD (Amp-Shaper-Discri) chips [2] and one AMT chip are mounted on a small multi-layer printed circuit board (mezzanine board), which plugs into a MDT end plug PCB.

Two modes of operation will be provided in MDT measurement. In one mode the ASD output gives the time over threshold information, i.e. signal leading and trailing edge timing. The other mode measures leading edge time and charge. The Wilkinson ADC serves as a time slew correction and also provides diagnostics for monitoring chamber gas gain. It operates by creating a gate of ~20ns width at the leading edge of the signal, integrating charge onto a holding capacitor during the gate, and then running

down the hold capacitor at constant current (the maximum rundown time is of order 200ns). The discriminator also generates artificial dead time to avoid multiple hits.

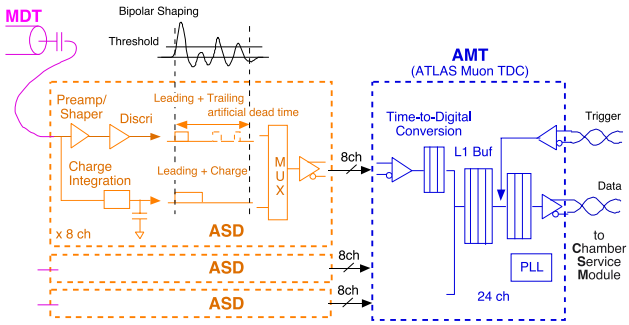

Fig. 2 MDT front-end electronics. AMT chip receives timing signal from three ASD chips and sends data to a Chamber Service Module.

III. AMT-1 Circuit Description

Block diagram of the AMT-1 chip is shown in Fig. 3, and main specification of the chip is summarized in Table. 1. Most of the circuits except time critical parts are written in Verilog code and logic synthesis are used. Since the detailed description of the chip is available in other documents [3, 4], only brief explanation is presented here.

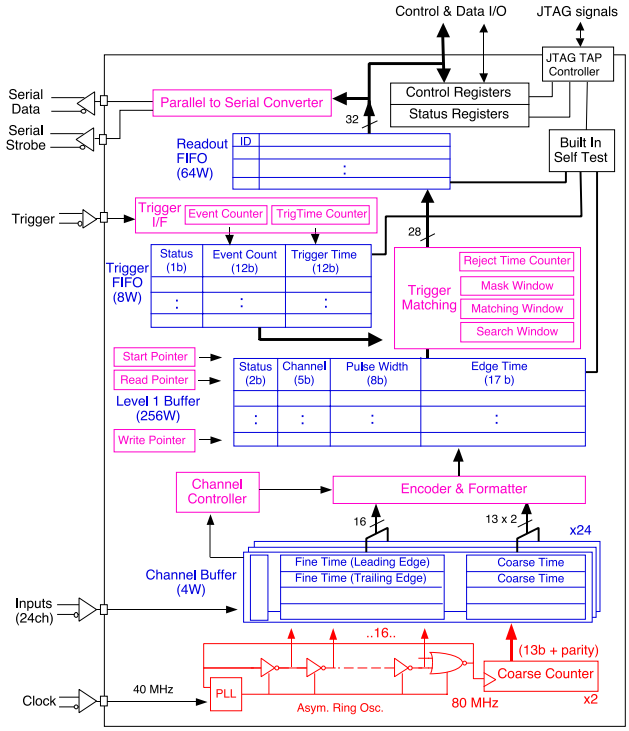

Fig. 3 Block diagram of the AMT-1 chip.

Table. 1 AMT-1 Specification (@40MHz System Clock)

Least Time Count	0.78125 ns/bit
Time Resolution	300 ps RMS
Dynamic range	13 (coarse) + 4 (fine) = 17 bit
Max. Trigger Latency	16 bit (51 µsec)
Int./Diff. Non Linearity	< 80 ps RMS
No. of Channels	24 Channels
Level 1Buffer	256 words
Read-out Buffer	64 words
Trigger Buffer	8 words
Double Hit Resolution	<10 ns
Hit Efficiency	100% @400 kHz(single edge) >99.8%@400kHz(two edge)
Hit Input Level	LVDS
Power	3.3+-0.3V, ~500 mW
Process	0.3 µm CMOS Sea-of-Gate
Package	144 pin plastic QFP

A. *Timing signal*

Accurate timing signals are derived from an asymmetric ring oscillator [5] which is stabilized with a Phase Locked Loop (PLL) circuit. The structure of the asymmetric ring oscillator (Fig. 4) is well fit to the gate-array structure and it generates even number of equally separated timing signals.

The PLL produces a double frequency clock (80 MHz) from a LHC beam clock (40MHz). By dividing the 12.5 ns clock period into 16 intervals a time bin size of 0.78 ns is obtained. Placement and route of this part is done manually, and fine adjustments of load capacitance are done for each output nodes.

System clock for other parts are 40 MHz, and it is generated from the 80MHz clock. The entire system clock tree is automatically generated to reduce clock jitter.

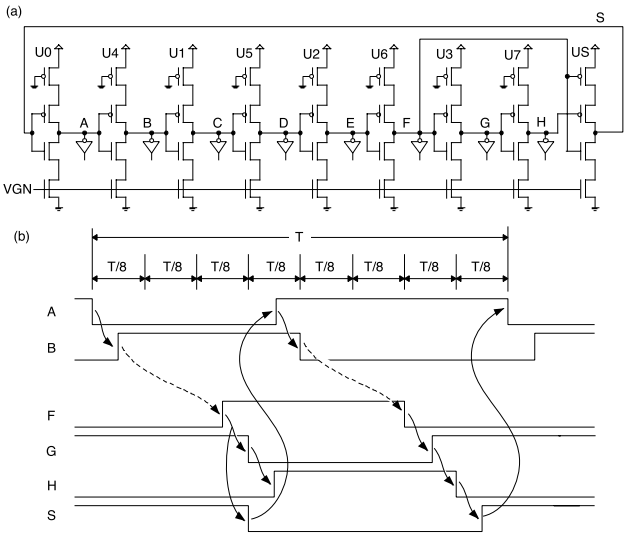

Fig. 4. (a) Schematics of an asymmetric ring oscillator (8 stages) and (b) timing diagram. Oscillator in the AMT-1 consists of 16 stages.

B. Buffers

A hit signal is used to store the fine time and coarse time measurement in individual channel buffers. The fine time measurement is obtained from taps along the asymmetric ring oscillator. The time of both leading and trailing edge of the hit signal (or leading edge time and pulse width) can be stored. Each channel has a 4-word buffer where measurements are stored until they can be written into the common level 1 buffer.

When a hit has been detected on a channel the corresponding channel buffer is selected, the time measurement is encoded into binary form, the correct coarse count value is selected and the complete time measurement is written into the L1 buffer together with a channel identifier.

The L1 buffer is 256 hits deep and is written into like a circular buffer. Reading from the buffer is random access such that the trigger matching can search for data belonging to the received triggers.

C. Trigger matching

Trigger matching is performed as a time match between a trigger time tag and the time measurements them selves. The trigger time tag is taken from the trigger FIFO and the time measurements are taken from the L1 buffer. Hits matching the trigger are passed to the read-out FIFO. To prevent buffer overflow and to speed up the search time an automatic reject function can reject hits older than a specified limit when no triggers are waiting in the trigger FIFO.

The trigger matching can optionally search a time window before the trigger for hits which may have masked hits in the match window. A channel having a hit within the specified mask window will set its mask flag. The mask flags for all channels are in the end of the trigger matching process written into the read-out FIFO if one or more mask flags have been set.

All data belonging to an event is written into the read-out FIFO with a header and a trailer (optional). The header contains an event id and a bunch id. The event trailer contains the same event id plus a word count.

D. Control and status registers

There are two kinds of 12 bit registers, "Control" and "Status" registers. Contents of these registers are shown in Table. 2. The control registers are readable and writable registers which control the chip functionality. The status registers are read only registers which shows chip statuses.

Table. 2. Control (CSR0-15) and Status (CSR16-21) registers bit assignments.

bit	11	10	9	8	7	6	5	4	3	2	1	0
CSR0	global_reset	error_reset	disable_encode	enb_errrst_bcrevr	test_mode	test_invert	enb_direct	disable_ringosc	clkout_mode		pll_multi	
CSR1	mask_window											
CSR2	search_window											
CSR3	match_window											
CSR4	reject_count_offset											
CSR5	event_count_offset											
CSR6	bunch_count_offset											
CSR7	coarse_time_offset											
CSR8	count_roll_over											
CSR9	strobe_select		readout_speed		width_select			-	tdc_id			
CSR10	enb_auto_reject	nb_l1occup_radout	enb_match	enb_mask	enb_relative	enb_serial	enb_header	enb_trailer	enb_rejected	enb_pair	enb_trailing	enb_leading
CSR11	enb_rofull_reject	enb_l1full_reject	enb_trfull_reject	enb_errmark	enb_mark_rejected	nb_ermark_rejected	enb_errmark_ovr	enb_l1ovr_detect	enb_mreset_code	enb_resetcb_sepa	enb_mreset_evrst	enb_setcount_bcrst
CSR12	enb_sepa_readout	enb_sepa_bcrst	enb_sepa_evrst	enb_error								
CSR13	enb_channel[11:0]											
CSR14	enb_channel[23:12]											
CSR16	rfifo_empty	rfifo_full	control_parity	error								
CSR17	l1_empty	l1_nearly_full	l1_over_recover	l1_overflow	l1_write_address							
CSR18	tfifo_empty	tfifo_nearly_full	tfifo_full	running	l1_read_address							
CSR19	coarse_counter	tfifo_occupancy			l1_start_address							
CSR20	coarse_counter[12:1]											
CSR21	0	0	0	0	0	0	rfifo_occupancy[5:0}					

There are 15 control registers and 6 status registers. These registers are accessible from 12-bit I/O bus or through JTAG interface. Since a SEU (Single Event Upset) in the control registers may cause important effect on the chip operation, a total parity of the control registers are stored in the status register. If a bit in the setup register changes without normal write operation, a parity error is caused and notified through an Error signal or an Error packet.

E. JTAG and BIST

The chip has JTAG boundary scan circuit, which is used to scan I/O pins, the control and status registers, internal circuit registers for debugging purpose, and BIST (Built-In Self-Test) for the level 1 buffer and FIFOs. The channel buffer and the level 1 buffer have a parity bit for each word to detect SEU.

IV. Measurement Results

The chip was successfully operated and tested, though some small bugs are found. Further systematic tests combined with the ASD, readout module, and a MDT chamber are scheduled in near future. Here some of the test results are shown.

A. PLL

Jitter of the ring oscillator was measured by measuring relative time distribution to input clock. Fig. 5-(a) shows the jitter dependence to the oscillating frequency. The jitter around operating point (80MHz) is less than 150 ps. This value is sufficiently low as for the required resolution of 0.5 ns in the MDT.

Fig. 5-(b) shows the jitter variation to the power supply voltage (Vdd). This also shows good stability around the operating point (3.3V).

In the AMT-TEG chip [6], time jitter was about 140 ps and time resolution of 305 ps was obtained in which quantization error contributes 225ps. Both the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) were small (<80 ps RMS).

There is no major change in the PLL and ring oscillator parts, so similar performance is also expected in the AMT-1 chip.

B. Serial Readout

The AMT-1 chip has a serial data interface in addition to a 32-bit parallel data interface. The serial interface supports both DS-protocol and simple data-clock output. The data transfer speed is selectable between 10 MHz to 80 MHz, and 40 MHz will be used in the MDT.

An example of waveform, which is driven by LVDS drivers, is shown in Fig. 6. Packet of the data consists of a start bit, 32 bit data, a parity bit, and a stop bit.

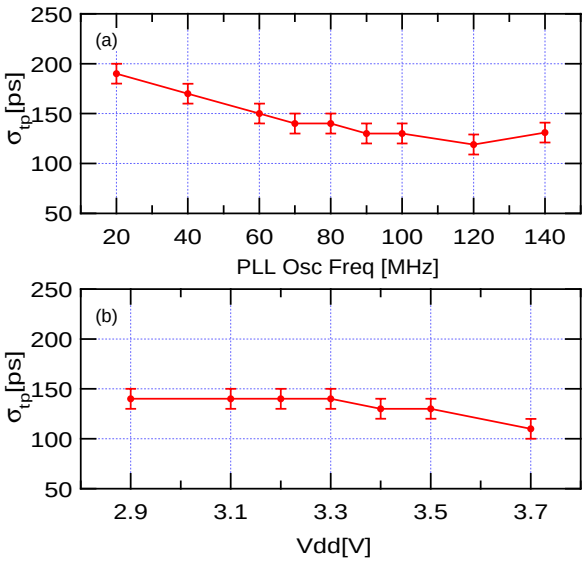

Fig. 5 PLL jitter variation relative to input clock. (a) Frequency dependence (Vdd=3.3V), (b) Voltage dependence (PLL Osc = 80 MHz).

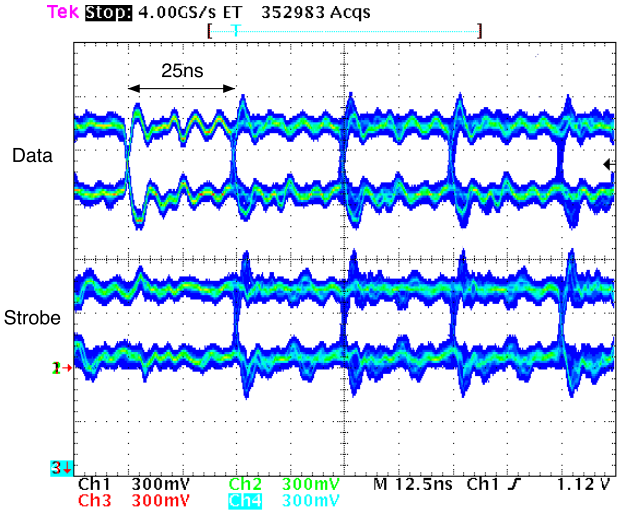

Fig. 6. LVDS serial output (DS protocol) wave form at 40Mbps. Upper lines show data line and bottom lines show strobe signal.

C. Power Consumption

Total power consumption of the chip is measured at expected operating condition and we observed about 500 mW power dissipation. Most power consuming part is LVDS receiver at present design from the circuit analysis. Although the power consumption is marginal, further reduction of the power is planned by optimizing the LVDS receiver circuit.

D. Radiation tolerance

Total dose expected for worst location of the MDT electronics is 11 krad for 10 years LHC operation with a safety factor of 4. Radiation tolerance for gamma ray and neutron was measured in the AMT-TEG chip and

reported in reference 1 and 6. Present CMOS process shows adequate radiation tolerance for use in MDT environment.

Furthermore we also irradiated the AMT-1 chip to gamma ray at Tokyo Metropolitan University with a Co^{60} source. The irradiation rate was about 76 rad(Si)/sec, and total dose irradiated was 30 krad(Si). During the irradiation power and clock are supplied to the chip. To study post-radiation effects, measurements were also done after annealing (1 week at room temperature and 1 week at 100 degree C) following the "ATLAS Policy on Radiation Tolerant Electronics" procedure [7].

We have measured variation of PLL oscillation and increase of leakage current. There is no obvious change observed up to the 30 krad(Si) irradiation.

V. Summary

A prototype TDC chip (AMT-1) was developed for ATLAS MDT detector. The chip was fully functional and showed adequate performance. After thorough system test with other electronics and chambers, a production chip will be designed with minor modifications to the present chip. Mass production is scheduled around the end of year 2001.

Acknowledgements

I would like to thank to O. Umeda, I. Sakai, K. Tsukamoto and T. Takada (Toshiba Co.) for their technical support. I also thank to T. Kondo (KEK) for his continuous encouragement.

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