The new ATLAS TRT read-out system

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Abstract

The ATLAS TRT detector [1] is very demanding in terms of electronics performance because of the high occupancy of the detector. A new version of the full read-out system, including two new ASICs and the new back-end modules, has been designed and tested successfully at 40 MHz clock rate and high trigger rate on a detector prototype. A description of this system will be given, as well as test results and plan for future scaling.

I. SPECIFICATIONS AND REQUIREMENTS

There are two groups of specifications. The one related to dataflow and control; this is common for all ATLAS subdetectors; and the other one, related to the TRT specific needs.

A. General specifications

The scheme for data processing, event selection and TTC (Timing Trigger and Control) adopted in ATLAS requires continuous data flow from subdetectors with maximum trigger rate of 100 kHz. This implies the use of the pipelined architecture and fully synchronous system. To extract the required amount of data (20 Tbit/s) the use of the high speed links is mandatory. The data sent to trigger L2 must follow the ROI (Region of Interest) format. On top of this, there are general requirements for low power electronics which is radiation hard.

B. TRT specific requirements

Due to the nature of the detector (gaseous, thin 4 mm diameter coaxial structure, 40 cm to 1 meter long) there are specific requirements for analog electronics. Straw tube forms a transmission line structure; in order to get as much as possible of signal energy in as short as possible time, the input impedance of preamplifier should have a specific value. This value differs slightly from high frequency characteristic impedance of the straw but is rather set to the value which matches the straw impedance at the frequency range where the signal has the maximum energy.

Long ion tail of the signal requires very good ion tail cancellation circuitry because of very high occupancy. On top of this, Xenon gas mixture used in this detector for capturing Transition Radiation (TR) photons shows non-standard behaviour. Instead of simple 1/(t+t0) dependence, the trailing edge of the signal from the straw can be best matched by superposition of 3 exponentials.

The electronics should be able to register both the MIP and a Transition Radiation photon and distinguish between them. As the MIP creates the extended ionization in the straw with 2 keV mean energy and TR photon causes point like ionization with much higher energy, the obvious way to achieve their identification is to employ the fast shaping technique followed by two discriminators at low and high threshold. The hit in low threshold discriminator indicates the particle crossing the straw while the simultanious hit in high threshold indicates also a TR photon.

In order to achieve good spatial resolution, the drift time measurement technique is used. The circuit called transient digitizer was developed; it samples the output of the low threshold discriminator each 3.125 ns, thus providing the full information on the start and the end of the signal.

II. SYSTEM OVERVIEW

The readout and TTC distribution is described on TRT endcap example [2] (barrel part is very similar) - figure 1. TRT endcap wheels are served with TTC signals (clock, trigger, ID reset, etc.) in φ direction in order to be able to adjust the timing on the detector for differences caused by time of flight and cable delays. Each endcap side and each barrel side forms one TTC partitions, so there are 4 TTC partitions in total. The data readout must follow the Region of Interest (ROI) organization defined by trigger level 2, so all the data belonging to one ROI are readout in 'z' by 3 RODs and thus are concentrated in corresponding 3 ROBs (trigger level 2 buffer). This ensures an easy access to ROI data. One TTC modules serves three RODs modules and is also responsible for parameter loading for frontend electronics.

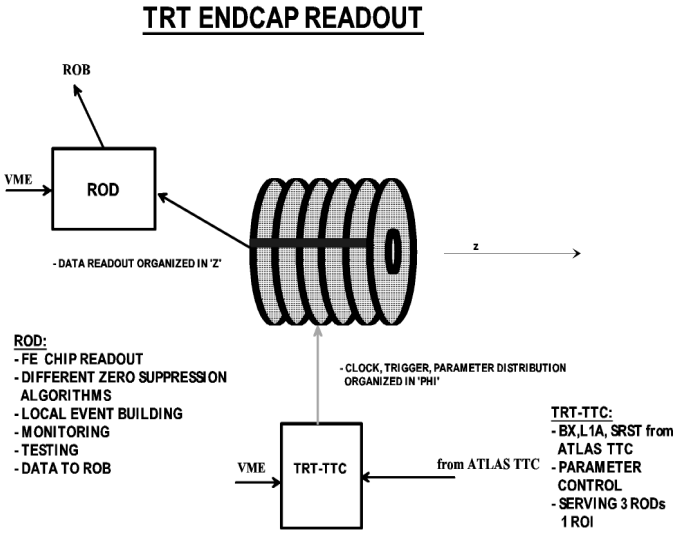

Figure 1: The example of the endcap readout

Simplified functional block diagram emphasizing the readout channel for one straw is shown in fig.2. Signal from the straw is processed in preamplifier and shaper. Semi-gaussian output signal is compared in 2 discriminators. The high threshold output is stored directly in the pipeline and the low threshold output is sampled each 3.125 ns time slice within 25 ns clock cycle thus effectively forming transient digitiser - the circuit which stores the level of the input line in 8 sampling points in 25 ns. The eight bits from transient digitizer are also stored in the pipeline. The depth of the pipeline is sufficient for storing the events until the trigger level one decision. Upon trigger Level 1 Accept signal, trigger decision logic selects 3 time slices defined by Bx clock and stores them into the derandomizer. The readout via the output serial line starts automatically as soon as at least one event is stored in the derandomiser. Custom miniature individually shielded twisted pair lines are used for extracting the data from the detector. 104 such a serial lines are concentrated at the level of the patch panel, where the signals are refreshed with active LVDS repeaters and sent through a 28 AWG twisted pairs to the backend electronics. The links from three patch panels serving one region of interest (ROI) are connected to three backend modules (ReadOut Drivers - ROD) responsible for local data reformatting, event fragment building, error checking and sending the event to the Readout Buffers (ROBs) which are the buffers for global event building. The three RODs are served by one TTC module, which provides them with L1A (trigger level 1 accept), BCID (bunch crossing identification), L1ID (trigger level one identification) and TriggerType info through a custom backplane (J3 on VME). The TTC module is also responsible for timing, control and parameter signals distribution on the detector and for downloading the configuration data to the readout chips.

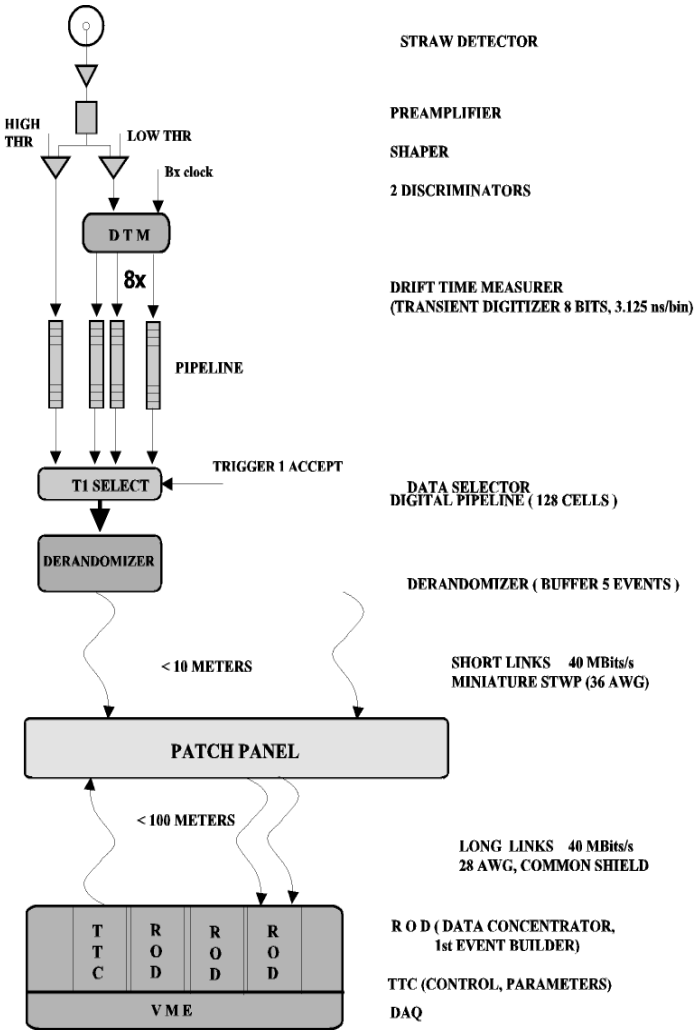

Figure 2: Simplified dataflow

III. SYSTEM COMPONENTS

A. *chips*

There are two frontend chips

1) ASDBLR chip (Analog)

This is an 8 channel, bipolar chip produced in DMILL technology. It contains the preamplifier, shaper, ion tail cancellation circuit and the base line restorer. There are two discriminators with hysteresis which guarantees the minimal output pulse width to be ~5ns. In order to avoid high amplitude swing signals close to the sensitive inputs, small amplitude current differential output has been chosen with ternary encoding of information from both high and low threshold comparators. Lower current value (100 μA) indicates a hit only in low threshold discri, higher current value (200 μA) indicates hit in both discriminators. The equivalent noise charge is at the level of 2200 electrons for 10pF input capacitance. The pulse width is 15 ns at the base. The chip was packaged in 68 pin PQFP.

2) DTMROC chip (digital)

This 16 channels chip receives ternary signals from ASDBLR. As the chip runs synchronously with Bx clock a latching mechanizm is provided at the input of the DTMROC in order to be able to catch signals which could be as short as 5 ns. The line corresponding to the low threshold discriminator on ASDBLR is sampled with 3.125 ns step in 25ns clock period. The eight samples are written into the pipeline as well as one bit corresponding to the high threshold output of ASDBLR. Thus there are 9 bits stored into the pipeline for each channel and time slice. The pipeline has 132 cells. Upon receiving the L1A signal, the data corresponding to the 3 time slices are written to the derandomizer for each channel. The derandomizer can store up to 13 events. The readout is organized on one serial link running at 40Mbits/s. Apart the data, the chip is providing also 3 bits of L1ID and 4 bits of BCID counters.

There are 4 DACs for generating the threshold voltage for ASDBLR as well as test pulse generation for testing the analog frontend with programmable amplitude and delay. On the chip there are also some test and channel mask facilities.

The chip was produced in DMILL technology and packaged in 100 pin PQFP [3].

B. frontend boards

The smallest TRT readout module is serving 64 straws. There is a separate analogue board with eight ASDBLRs. On top of it is plugged the DTMROC board with four DTMROC chips. The services cables are connected to the roof board (figure 3).

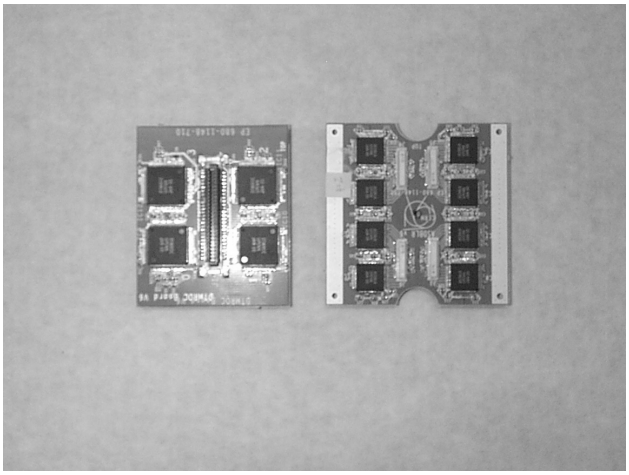

Figure 3: The analogue and digital fronend boards

C. patch panel

The prototype of patch panel two (calorimeter crack) with all the functionality has been designed, produced and tested. It contains the LVDS repeater for data signals as well as signal equalizer, repeater and doubler for TTC lines. For system tests the regulators for power supplies has been included (figure 4).

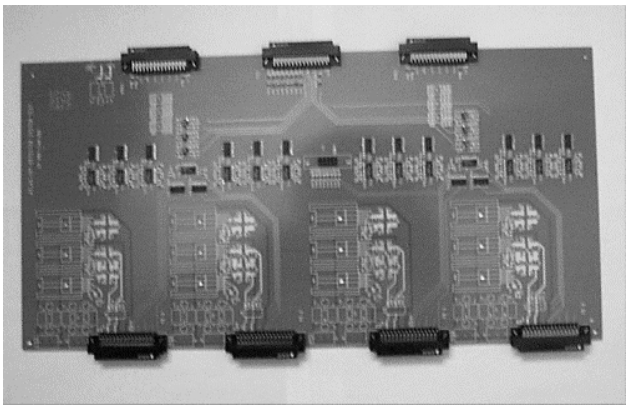

Figure 4: The prototype of the patch panel

D. cables

The copper cables are the baseline transmission lines in TRT readout. The custom cable was developed for connecting the frontend to patch panel two (inside ATLAS detector). It is size 36 AWG individually shielded TWP, tested for 40MBits/s speed and up to 10 meters length. The measured bit error rate is less the 10^{-14}.

Another custom cable was developed for connecting the patch panel two to the backend electronics. It is size 28 AWG common shield TWP, tested 40MBits/s up to 100 meters with passive equalizer.

Both prototypes were used in system tests and test beams. They are standardized and available at CERN store.

E. Back End miniROD (fig. 5)

The full ROD was designed in 1998 but only a scaled down version miniROD was produced. It serves 26 input lines (instead of 104), it contains VME buffer for monitoring and test beam purposes. The zero suppression part was left out as well as S-link buffer (no S-link). It builds the header and event fragment which are accessible through VME bus together with monitoring data. It also contains the checking and error identification tools. More detailed description can be found in LEB98 document [4].

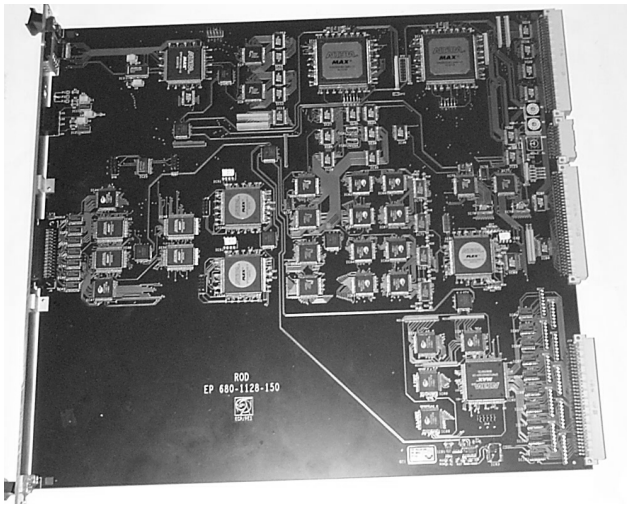

Figure 5: MiniROD VME module

F. Back end -TRT TTC module (fig. 6)

This module is used to implement TTC [5] and TRT specific commmands functions and parameter loading for frontend electronics. It receives one TTC optical line from TTCvi module [6] via TTCrx chip [7]. From this line it extracts the clock, L1A, BCR and SRST commands and receives trigger type informations. Through the custom lines it downloads parameters to the frontend electronics from DAQ, on board database or local TRT readout processor. It distributes the clock and commands both to the frontend electronics and ROD modules. All lines to the frontend electronics have adjustable delay. For test beam and system tests purposes it can receive commands from the front panel (NIM). It also measures the phase between the physical trigger and Bx clock, which is needed for drift time measurements in SPS type of beam.

It is a 9U VME board produced in 2000 and used in both SPS and LHClike (25ns structure) test beams.

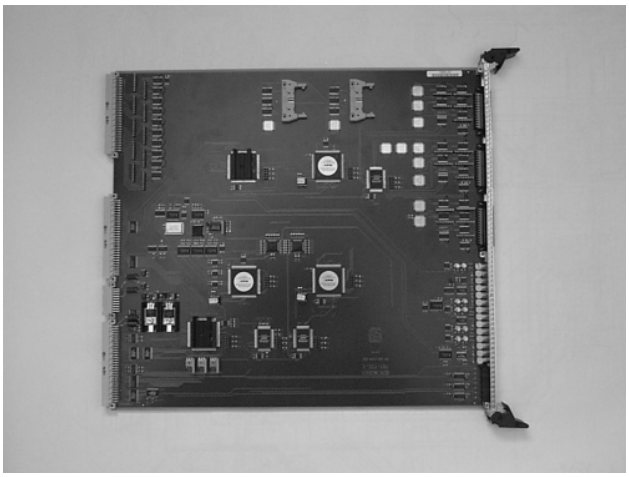

Figure 6: TRT-TTC 9U VME module

IV. TEST BEAM

The new readout system has been used at the SPS accelerator (CERN) test beam with the prototype of the detector which corresponds to the azimuthal section of the TRT endcap wheel type A (figure 7). The construction of the detector followed the TRT rules and guides for grounding and shielding [8]. Mounted analogue ASDBLR frontend board is on figure 8.

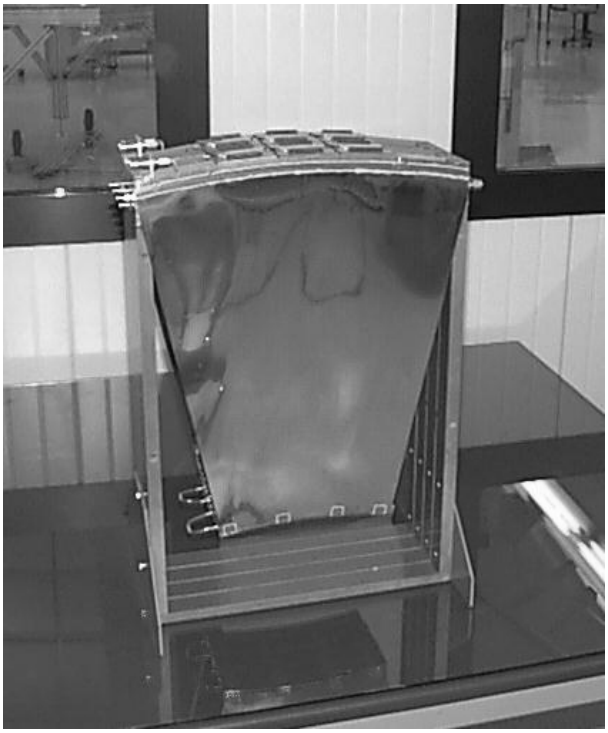

Figure 7: TRT endcap sector prototype

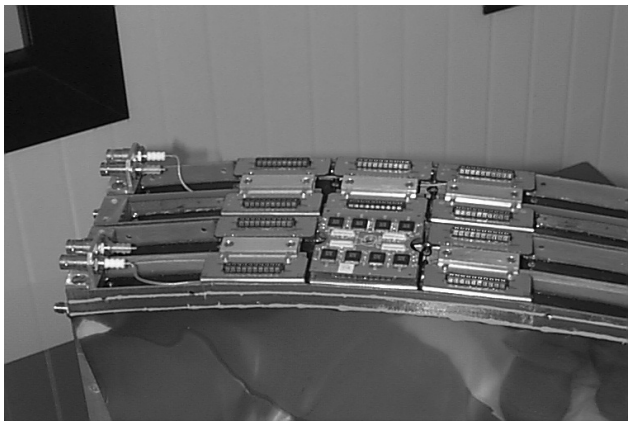

Figure 8: The detail of sector prototype with ASDBLR analogue board installed. Also the aluminium cooling structure is visible.

The system was tested both with the 'standard' SPS beam and LHC-like beam with 25ns bunch structure. The synchronous operation of the readout has been achieved. The maximum trigger rate for continous operation is 100kHz without extra CAMAC and silicon detector readout until filling up the VME buffer. The VME readout does not provide sufficient bandwidth for continous operation with maximum trigger rate.

The system noise level was equivalent to 40eV , low threshold channel on frontend electronics was possible to set to 200eV with reasonable noise counting rate <100kHz.

The measured r-t dependence proves the functionality of drift time measurement circuit. Figure 9.

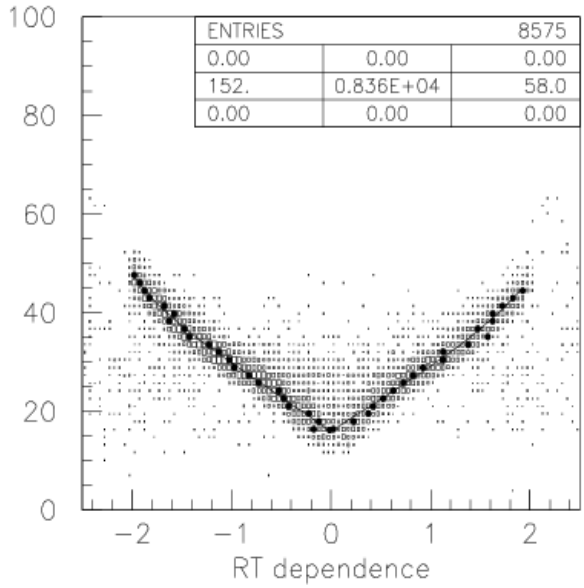

Figure 9: R-t dependence of single straw.

The positional resolution was measured as a difference between tracks from refence silicon tracker and TRT straw detector. Figure 10.

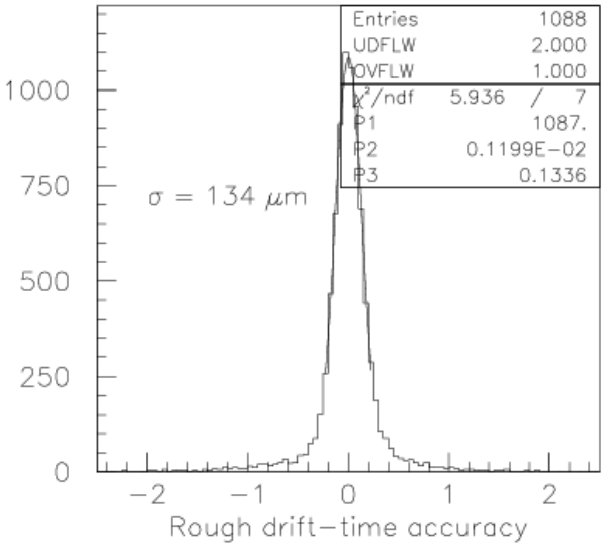

Figure 10: Spatial resolution for the single straw

The efficiency for 2 .5 sigma road was measured better then 88% - figure 11.

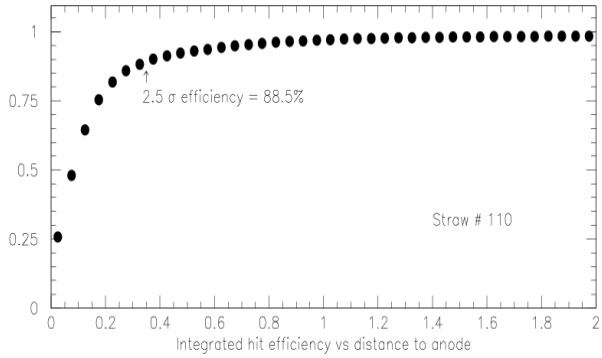

Figure 11: The efficiency of a single straw for 2.5σ road.

V. CONCLUSIONS AND PLANS

We have demonstrated a new (the 3rd generation) working LHC like electronics for TRT readout. The TRT readout architecture has been verified in few successful test beams since 1993 [9][10][11] and the last version has run also with 25ns LHC-like beam. The performance of the system is promising. We have achieved a low noise operation with system clock 40 MHz, tracking performance was better then 140 um with efficiency 88% (road 2.5 σ) at low rate, TRT provides electron identification and the system operates without the dead time with trigger rate up to 100kHz.

At the end of 2000 we plan to do a large scale system test (1/2 of TRT wheel A) with ~3000 straws to test the operation with final TRT detector. The application specific frontend chips need only a minor modifications and the flex-rigid frontend board for signal distribution on the detector has also been designed and partially tested. For the back end modules, we plan to produce halfROD at the end of 2000; this module should have the full functionality, reduced number of channels. The final TRT-TTC and ROD modules should be finished in 2001. There are plans for testing the system with full functionality with significant fraction of the TRT detector.

VI. REFERENCES

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