# TIMING, TRIGGER AND CONTROL DISTRIBUTION AND DEAD-TIME CONTROL IN ATLAS

Per Gällnö, CERN, Geneva, Switzerland
(email: per.gallno@cern.ch)

*Abstract*

The RD12 TTC system [1] is the backbone for the timing, trigger and control distribution in ATLAS. The last developments of TTC modules as well as their use in ATLAS are presented.

The strategy for dead-time control of the experiment is also presented.

## INTRODUCTION

### *Timing, trigger and control*

The different sub-detector Front End (FE) and Read Out systems of the ATLAS experiment all require timing, trigger and control information, such as the bunch crossing signal (BC), the trigger level-1 accept signal and various control and calibration parameters. Reset signals for the Bunch and Event Counters are also needed for system synchronisation purposes by the Front End and Read Out elements.

This information comes normally from the LHC machine, the Central Trigger Processor (CTP), the Data Acquisition system and the Detector Control System.

A multipurpose fibre optic based distribution system, the TTC, has been developed for this purpose within the framework of the RD12 project. Accepted triggers, trigger information, event count, various calibration, control, reset and test commands can be sent over the TTC network.

### *Dead-Time Control*

The data flow in the ATLAS sub-detector acquisition systems needs to be controlled in order to prevent information losses in the case the data buffers in the Front End, Read Out Drivers (ROD) or Read Out Buffers (ROB) get saturated.

Three different mechanisms to control the data flow will be implemented:

- By ***Back pressure*** using a XON/XOFF protocol on the read-out links between the ROD's and the ROB's.
- By ***Throttling*** to slow down the level one (LVL1) trigger rate from the CTP when the ROD data buffers are nearly filled.
- By ***Prevention*** introducing a constant dead-time combined with one set by a pre-programmed algorithm in the CTP in order to avoid buffer overflow in the Front End. The constant dead-time is chosen to be 4 BC's after each LVL1 and the algorithm, called "leaky bucket", limits the number of LVL1 to 8 in any window of 80µs.[2]

The introduction of a dead-time by a *throttling* mechanism is based on a ROD busy signalling scheme informing the Central Trigger Processor about the state of the ROD data buffers as each ROD is able to produce a ROD-Busy signal when its buffer is filled up. The busy signals from each ROD are summed and monitored in ROD-Busy Modules connected in a tree structure to finally produce a veto signal for the CTP. The ROD Busy signalling scheme and associated hardware will be described in this context.

## THE TTC SYSTEM

### *System Description*

The TTC system is a unidirectional optical fibre based transmission system, where two information channels, A and B, are Time Division Multiplexed (TDM) and Bi-Phase Mark (BPM) encoded using the LHC Bunch Crossing (BC) clock (40.08 MHz) as the carrier frequency. One channel (A) carries exclusively the LVL1 trigger accept (L1A) information and the other (B) carries packaged address and data information for the sending of various reset commands or calibration, control and test parameters.

The LHC BC clock is used as the TTC system master clock and is distributed to all destination systems by the receivers extracting it from the BPM encoded signal.

The data packages sent on the B-channel can either be of short format (8 data bits), used for broadcast commands or of long format (14 address, 8 sub-address and 8 data bits) for individually addressed commands or data transfers. Error correction coding is implemented by adding standard Hamming code, 5 respectively 7 bits, to the two data formats. Commands may either be transmitted asynchronously or in a fixed timing relation to the LHC BC Clock and Orbit signals.

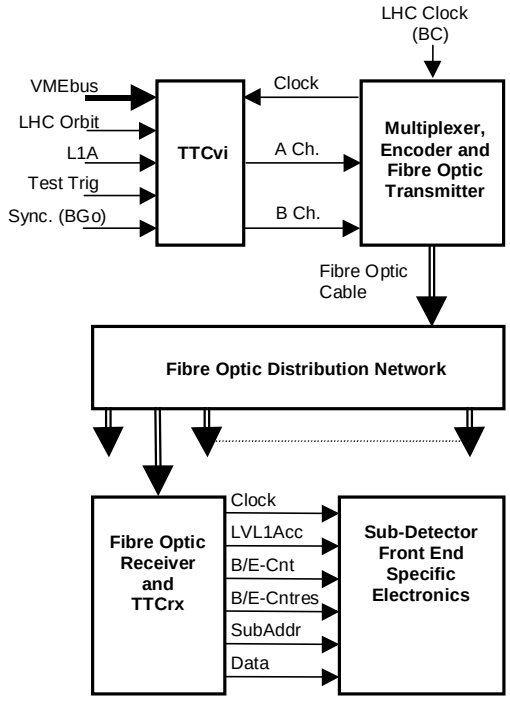


*Figure 1. The TTC system block diagram*

A final system integrated in the experiment will comprise the following hardware components:

- The LHC Clock and Orbit signals receiver/fan-out crate, TTCmi
- The VMEbus interface module, TTCvi
- The modulator (TDM + BPM) and optical fibre laser transmitter unit
- The tree structured optical fibre distribution network
- The photo detector diode and the TTC receiver ASIC[1], TTCrx
- The FE or Read-Out system specific modules carrying the TTCrx

## *New developments for TTC*

The design of the original TTCvi module has been revised and an enhanced version, the TTCvi - MkII, is now delivered to the users.

Two types of laser transmitter modules have been developed by RD12 for TTC signal distribution within the LHC experiments.[2] Both modules have a 6U/4TE form factor, ie. standard VME format, and use standard VME supply voltages.

The TTCex contains two encoders driving each five optical outputs. The TTCex may be configured to drive all ten outputs as one TTC partition. Further fan out of each optical output may be achieved using an optical tree coupler.

The TTCtx supplies a total of 14 optical outputs derived from an already encoded electrical signal. Possibility exists to configure the module to drive two groups of 7 optical outputs from two different external encoders.

# VMEbus INTERFACE - TTCvi

## *The TTCvi MkII Module*

The original TTCvi module was designed in 1997. Since then 40 modules have been produced and delivered to users. A questionnaire was distributed in 1999 to the TTC users in order to collect their feedback. Based on this survey an improved version of the TTCvi was designed, ie. the TTCvi MkII. A subsequent preliminary design review (PDR) was performed in April 2000.

## *TTCvi MkII new features*

The following improvements and modifications have been introduced:

1. It is now possible to select the internal counting of ***either*** the event triggers ***or*** the LHC orbit pulses. A bit in the Control Register-1 controls the selection.

2. The internal event/orbit-counter may be reset by a VMEbus generated function.

3. The address, sub-address, size bit and int/ext bit of the event/orbit-count/trig-type B-channel transfers are now fully programmable from the VMEbus.

4. The event/orbit-count/trig-type B-channel transfers may be disabled.

5. A feature to allow for the generation of a delayed calibration TRIGGER triggered by an external pulse on one of the B-Go inputs. The delay is programmable in the same way as the INHIBIT delay.

6. Two LED indicators have been added to show the activity on the A and B channels.

7. A scheme for sending command bursts triggered and timed by the Inhibit signal has been developed on request by the LHC Beam Instrumentation Group. This feature will be implemented as standard on future modules.

8. Some discovered bugs have been corrected.

The updated version of the TTCvi technical manual may be found on the RD12 - TTC homepage [4]. A summary of required changes to the driver software is found in the manual appendix.

[1] Application Specific Integrated Circuit

### *Status*

A batch of 20 TTCvi MkII modules has recently been fabricated of which all modules have already been allocated to users.

Negotiations are under way with external manufacturer regarding the future production and support of TTCvi modules.

The milestones for the ATLAS requirements are a final design report in September 2000 and final version of TTCvi in June 2001.

## READOUT DRIVER BUSY HANDLING

### *System Description*

The Read-Out Drivers (ROD), of which there will be several hundred in the ATLAS experiment, buffer, process and format the data from the Front End electronics before being sent to the Read-Out Buffers (ROB).

If the data buffers in the ROD are close to get filled up the Level-1 trigger rate must be reduced. A way of achieving this is to send a busy flag to the CTP to introduce a dead-time.[5]

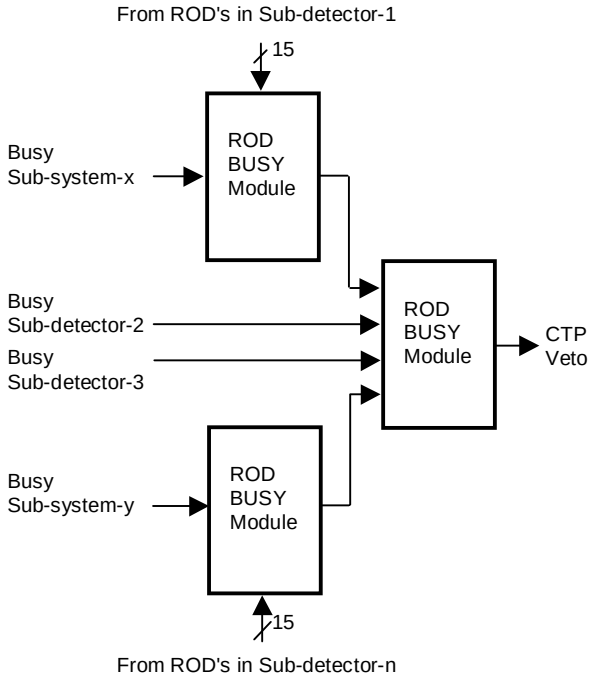


*Figure 2. The ROD -Busy tree structure*

Each ROD produces a Busy signal, which is sent to a ROD-Busy module together with Busy signals from other ROD's in the same sub-system. The ROD-Busy module sums the incoming Busy signals to produce one Busy signal of the particular sub-system. In turn the sub-system Busy signal is summed with other sub-system Busy signals in another Busy module to form a sub-detector Busy signal. Finally all sub-detector Busy signals are gathered to form a Busy input to the CTP.

## THE ATLAS ROD-BUSY MODULE

### *Module Description*

The ROD-Busy module [6] has been design to perform the following functionality:

1. Collect and make a logical OR of up to 16 Busy input signals.
2. Monitor the state of any input Busy signal.
3. Mask off any input Busy signal in the case a ROD is generating a false Busy state.
4. Measure the integrated duration any Busy input is asserted for a given time period.
5. Store a history of the integrated Busy duration for each input.
6. Generate an interrupt if any Busy input is asserted for longer than a pre-set time limit.
7. Generate a Busy output serving as an input for a subsequent ROD-Busy module in the tree structure or as a veto for the CTP.

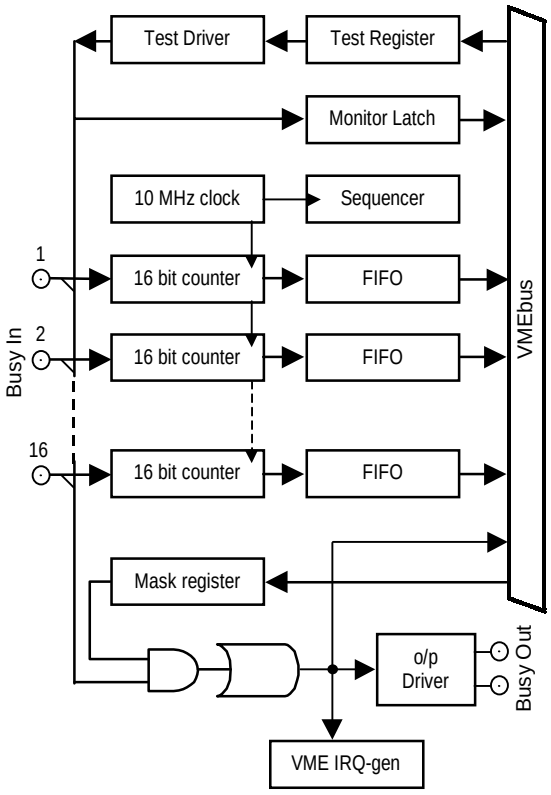


*Figure 3. ROD -Busy module block diagram*

### *Status*

The design of the ROD-Busy module is well under way and a prototype will be available for evaluation during the first half of 2001. The prototype will be packaged in a 6U/4TE form factor VME module. A conversion kit for implementation on larger VME boards is also foreseen.

### *Modular VHDL blocks*

The code for the different functional blocks has been written in VHDL and may be obtained on request in the case a designer wants to implement the Busy module functions directly in a ROD module.

The following VHDL entities will be made available:

1. Input monitoring, masking, stimulating and summing.
2. Quad 16-bit up-counter.
3. FIFO read/write sequencer.
4. VME slave and interrupter interface.
5. Busy time-out service requester to drive interrupter.

## CONCLUSION

The extensive use of the different TTC components in a variety of different test and evaluation set-ups has confirmed the efficiency and success of the TTC system.

The implementation of the ROD-Busy modules and their associated tree structured signal gathering scheme makes it possible to efficiently control the dead-time in the experiment and to easily detect faulty ROD modules introducing excessive dead-time.

## REFERENCES


[1] B.G. Taylor: "RD12 Timing, Trigger and Control (TTC) Systems for LHC Detectors" http://www.cern.ch/TTC/intro.html

[2] R. Spiwoks: "Dead-time Generation in the Level-1 Central Trigger Processor", ATLAS Internal Note

[3] B.G. Taylor: "Laser transmitter modules for TTC distribution at the LHC experiments" http://ttc.web.cern.ch/TTC/TTCtxSpecs.pdf

[4] Ph. Farthouat and P. Gällnö: "TTC-VMEbus Interface (TTCvi - MkII)" http://www.cern.ch/TTC/TTCviSpec.pdf

[5] ATLAS Level-1 TDR Chapter 20 http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/tdr.html

[6] P. Gällnö:"The ATLAS ROD Busy Module" ATLAS ROD Workshop, University of Geneva, Nov. 1998 http://mclaren.home.cern.ch/mclaren/atlas/conferences/ROD/programme.htm