OVERVIEW OF ATLAS LAr RADIATION TOLERANCE

C. de La Taille, LAL, Orsay, France (email: taille@lal.in2p3.fr)

Abstract

This document reviews the various developments pursued by the liquid argon (LAr) community in order to ensure the radiation tolerance of its front-end electronics.

1. INTRODUCTION

The LAr front-end electronics is located right on the cryostat in dedicated front-end crates [1]. These house four different species of boards :

- Front-end boards (FEB) which bear preamplifiers, shapers, analog memories, ADCs and optical outputs.
- Calibration boards to generate 0.2% accuracy calibration pulses
- Tower builder boards (TBB) which perform analog summation and re-shaping for LVL1 trigger
- Controller boards which handle TTC and serial link (SPAC) control signals

All these boards have been produced in several exemplars in order to equip module 0 calorimeter and extensively used in the testbeam for the last two years. Their performance has met the requirements in terms of signal, noise, density at the system level on several thousands of channels [2]. However, they make use of many COTS, in particular FPGAs that are not radiation tolerant.

Since then, several developments have been realised in order to design the "final" ATLAS boards, based on the same architecture but completely radiation tolerant. A milestone has been set to get the first boards by mid-2001 and a full crate by the end of 2001. The full production should be launched in 2002 (at least for the FEBs) and the installation would take place in 2004.

The radiation levels anticipated at the Lar crate location is 50 Gy in 10 years and 1.6 10^{13} N/cm^2 [3]. Taking into account the safety factors required by the rad-tol policy [4] , they must be qualified up to 0.2-3 kGy (20-300 krad) and 1-5 10^{13} N/cm^2, depending on the process as explained in [5] of these proceedings.

These developments will now be exposed, board by board, with a particular attention to the single event effects (SEE), their impact at system level and their mitigation.

2. FRONT-END BOARDS [6]

The various components used on the module front-end boards (FEB0) are shown in Figure 1.

2.1 Preamplifiers and shapers

The preamplifiers (0T) are hybrids built around discrete high F_T bipolar transistors. They have been irradiated several times (alone or with the shaper below) and have not shown any change of performance after 2 kGy and 5.10^{13} N/cm^2 [7]. For the hadronic end-cap, GaAs monolithic preamps are used inside the LAr and have withstood 10^{14}N [8].

The shapers are monolithic 1.2 µm BiCMOS circuits for which the radiation tolerance has been attempted at the design phase by using mostly the fast NPN transistors. The MOS are used mainly as overdriven static switches [9]. Notwithstanding, they have passed numerous irradiation tests without experiencing changes in gain or peaking time, as can be seen in Figure 2. The shaper also incorporates a simple logic to deactivate noisy channels in the trigger sums, for which SEU is not critical. Furthermore, a possible sensitivity to latch-up was feared, although never observed in 10 MeV neutrons tests at CERI. For safety, an anti-latchup resistor has been added in the logic power supply line.

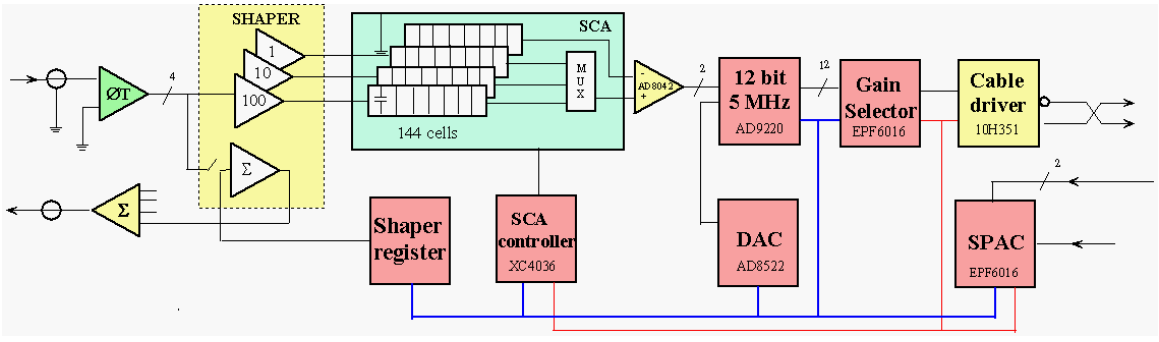

Figure 1 : *Synoptic diagram of the Front-end board used in module 0 test beam*

Date	Dose	Duration	# channels
May 97	2 10^{13} N	2 days	2 ch
Oct 97	2 kGy	4 days	2 ch
Jul 98	10^{14} N	1 day	8*3
Sept 98	2 kGy	4 days	16*3
Jul 99	2 kGy	2 months	32*3
Oct 99	2 10^{13} N	2 days	32*3

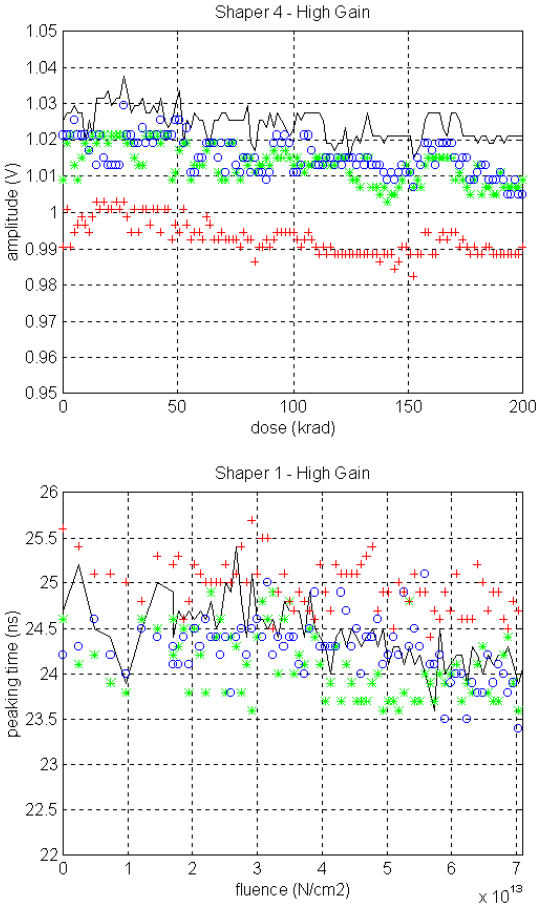

Figure 2 : *Shaper amplitude and peaking time under gamma and neutron irradiation.*

2.2 Switched Capacitor Arrays (SCA)

The analog pipelines (SCA) which follow the shapers have been designed from the start in DMILL radiation hard technology. They make use only of the CMOS components and of full custom logic running at 40 MHz. Several prototypes have been realized in DMILL in the last 3 years, as well as in radiation soft technologies (AMS 0.8 µm, HP 0.6 µm) with similar electrical performance. These results and the irradiation results can be found in these proceedings [10]. The latest batch has suffered from a very low yield (10%) due to a few randomly distributed leaky switches. This process defect has subsequently been understood and fixed in a later batch. The chip will undergo preproduction run by the end of 2000.

2.3 SCA controller

The read and write addresses necessary to operate the SCA with no dead time are generated by a SCA controller. In module 0 FEB, these functions were implemented in a XC4036 Xilinx, based on 0.35 µm technology [11]. This component has been tested for radiation tolerance and has shown a significant supply current increase after 400 Gy, as shown in Figure 3.

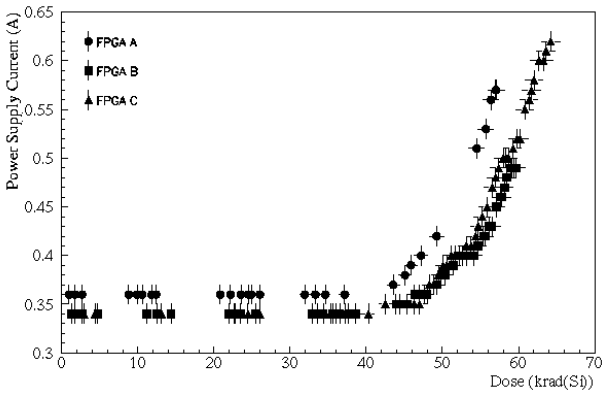

Figure 3: *Supply current after gamma irradiation for the Xilinx XC4036*

It has then been decided to migrate this element into DMILL. However, the chip complexity and critical timings have turned out to be marginally achieved and resulted in a very large chip area (100mm^2) for which the yield is likely to be rather small (20%). Besides, due to the large area, it has not been possible to include any error correction mechanism, leaving the SEU problem open. For such chip, the SEU effects are rather serious as read or write pointers could get systematically wrong. A possible fallback in 0.25 µm technology is now being designed, including SEU error correction logic.

2.4 ADC and gain selector

The SCA is followed by a 12 bit 5 MHz ADC. For FEB0, AD9220 was used but has also failed total dose tests. We therefore plan to use the AD9042, which has been qualified by CMS [12].

Two ADCs feed a gain selector chip that chooses the correct gain and formats the data for the subsequent RODs. As the chip stores two thresholds per channel for the gain selection, SEU have been mitigated with a Hamming correction code. It results in a 20 mm^2 ASIC, to be submitted to DMILL in september 2000.

2.5 Optical output

The formatted digital data are sent out after LVL1 trigger through an optical fiber. Five samples of each 128 channels are multiplexed at 40 MHz, resulting in 2.6 Gbit/s output rate. The baseline option was using HP Glink, but extensive irradiation studies [13] have shown that although the link exhibited very good total dose tolerance up to 43 kGy and 10^{13} N, it was sensitive to SEU, 0.05 error/link/hour with ATLAS spectrum. In particular, energetic neutrons could induce synchronization errors, bringing the link down up to 10 ms.

Several options have been studied in order to circumvent this problem and can be found in these proceedings [14]. One consists in using two Glinks and a "smart switch" at the receiving end, whereas another is based on GaAs link and sending twice the data. Slightly after the conference, the choice has been made to stay with the single Glink for cost reasons.

Another digital chip (MUX) is then necessary to turn the 32bit 40 MHz data into 16bit 80 MHz Glink input format. This chip has been submitted in DMILL in may 2000.

3. CALIBRATION BOARD [15]

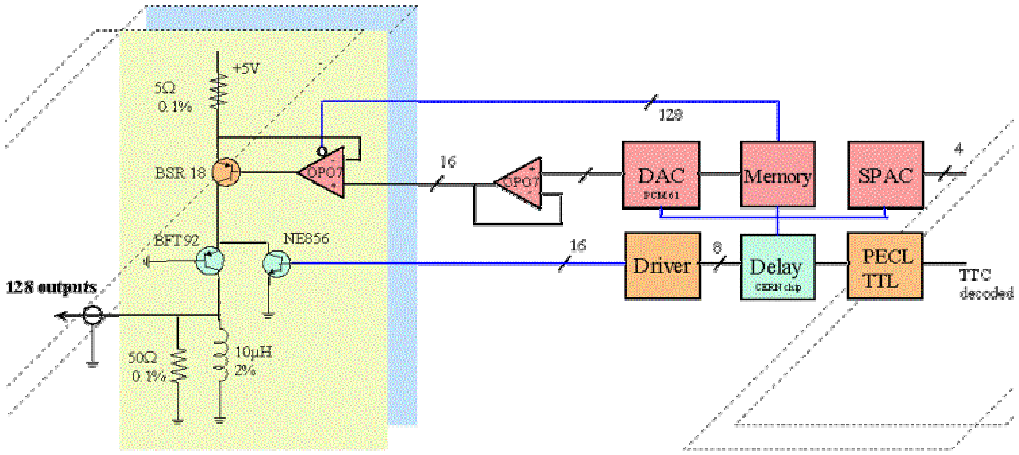

Figure 4 : *Synoptic diagram of the calibration board used on Module 0 tests.*

3.1 Low offset opamps and 16bit DAC

As shown in Figure 4, the precision current source is built around a low offset opamp and a 0.1% precision 5 Ohm resistor. The opamp offset should not be larger than the DAC LSB=16µV. In previous prototypes, OP07 were used and several similar opamps have been tested [16] to 2 kGy and 2.10^{13} N/cm^2, as shown in the table below. None has been good enough to be qualified for ATLAS.

Type	V_{off} before	V_{off} after	I_{bias} before	I_{bias} after
OP 113	7-60 µV	4-160 µV	0.35 µA	2 µA
OP 177	30 µV	4-160 µV	0.7 nA	70-90 nA
AD 829	60-200 µV	130 µV	3.5 nA	4.5 µA
LT1097	1-12 µV	1200 µV	0.1 nA	100 nA
OP 77	10-20 µV	70-190 µV	1 nA	100 nA
LT 1028	5-10 µV	70-360 µV	10-25 nA	5-80 nA
OP 27	1-10 µV	40-100µV	1-50 nA	0.7-0.9 µA
OP 07	5-15 µV	0.1-0.5mV	0.1-0.4 nA	0.2-0.3 µA

It has therefore been decided to develop a full custom rad-hard circuit to perform this function. Two approaches have been pursued :

- A static low offset opamp based on centroid bipolar transistors and fuse trimming
- An auto-zero opamp [17] in which the offset is stored in a 10 nF capacitor.

Prototypes of each version have been realized in AMS 0.8 µm BiCMOS, before being translated into DMILL. The static opamp has been submitted in may 2000, whereas the autozero could be submitted early 2001. The retained architecture will be chosen upon irradiation test results.

A 16bit DAC with 10-bit accuracy is necessary to cover the full dynamic range of ATLAS, but two COTS tested have seen the offset rise to 5 mV after only 20 Gy. Therefore, a 16 bit R/2R ladder DAC has been made with 16 switched identical current mirrors and external precision resistors (0.1%). To reduce the sensitivity to Vbe mismatch and variations with temperature the emitters of the current sources are strongly degenerated. This ladder DAC has been developed and tested successfully in AMS 0.8 BiCMOS and submitted to DMILL in may 2000, with improved temperature stability (1 µV/K).

3.2 Control logic

The calibration boards used on module 0 were controlled by an elaborate digital circuitry which allowed to load on board a full calibration sequence (ramping the DAC, changing patterns…). Although practical and very time efficient this circuitry was based on memories and numerous FPGAs which would not operate reliably in the high radiation environment.

It has thus been decided to simplify the control logic and load through the SPAC serial bus the run parameters (DAC value, delays, and pulsing patterns). These parameters are decoded from I^2C local bus and stored in registers, which have again been designed in DMILL. No particular SEU mitigation has been included, as the calibration board is idle 99% of the time and SEU results only in a wrong calibration pulse, which can be discarded in the RODS.

4. TOWER BUILDER BOARD

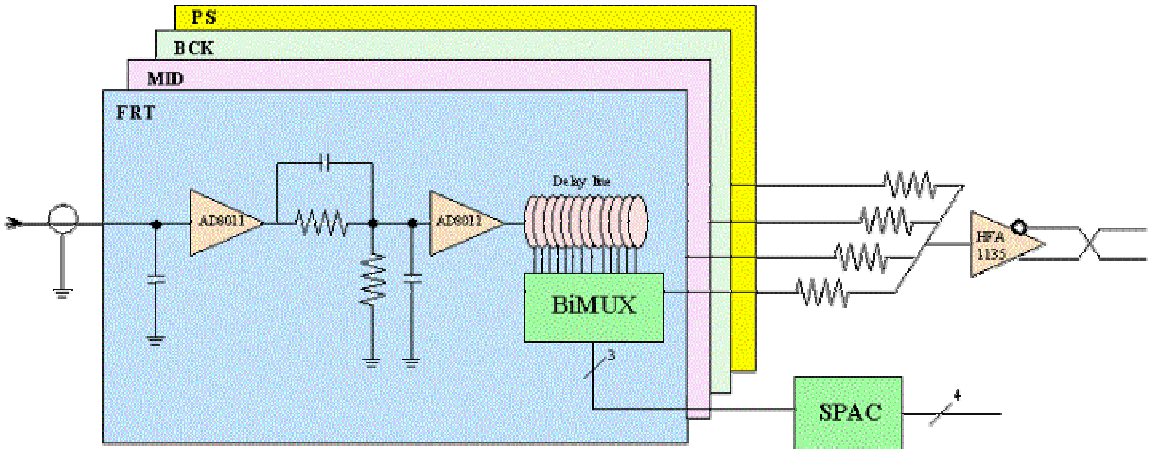

Figure 5: *Synoptic diagram of the tower builder board.*

The tower builder board is used to perform the analog sum of the different sampling depths of the calorimeter in order to get the total energy in a 0.1x0.1 tower. This signal is then sent through shielded twisted pairs to the LVL1 trigger processor. As the signals from the calorimeter exhibit different shapes across the calorimeter (due to different detector capacitance), a pole-zero unit is used to compensate for it and to uniformize the waveforms so that they can be summed. Furthermore, an anlog delay line is used to align the waveforms in time and compensate for different cable lengths or particle time of flight.

An analog multiplexer is used in order to select the correct tap on the delay line. Following negative tests on previous commercial multiplexers (DG358) which failed at 170 Gy, a DMILL chip has been developed in 1998. This chip called BiMUX includes 8 large CMOS switches (200/0.8 µm) and a simple address decoder to activate them. It has been fabricated in 1999 with a yield of 85% and tested successfully, including to radiation doses up to 2 kGy and 3 10^{13} N/cm^2.

Finally, the board makes use of commercial fast opamps (HFA1135, AD8011) which have also been tested successfully up to 2 kGy and 3 10^{13} N/cm^2, but additional tests against SEE are foreseen.

5. CONTROLLER BOARD

Every half crate is controlled by a controller board which receives optically the TTC signals (clock, LVL1, BCR…) and the serial link (SPAC) to write and read parameters on the various boards. These signals are translated to electrical signals and distributed to all the other boards, point to point for TTC and on a G10 bus for the SPAC. For reliability all the SPAC lines are doubled (including the incoming optical fibers) and the selection of the active line is performed in the control room.

On each board (including the controller) the SPAC signals are decoded by a SPAC slave chip which has also been realized in DMILL in may 2000. This chip is described in these proceedings [18].

6. CONCLUSION

The liquid argon calorimeter front-end electronics has been finalized and tested successfully in test beam. The analog front-end elements (preamp, shapers, analog pipelines) have shown radiation tolerance in excess of the ATLAS requirements, including the safety factors. The digital circuits (FPGAs) have failed such tests and have now been migrated into DMILL ASICs. The use of this radiation hard technology will largely alleviate the burden of the radiation tests. In total, almost 10 new DMILL chips will be necessary, as summarized in the table below :

Chip	Area (mm^2)	Number needed	Number produced	Subm. proto
SCA	30	54,400	80,000	98,99,00
SCA contr.	100?	3,400	20,000	Nov 00?
Gain select	21	13,800	20,000	Sept 00
Config contr	20	3,400	5,000	Sept 00
MUX	18	1,700	2,500	Sept 00
SPAC slave	27	2,200	3,300	May 00
Opamp	1.8	16,900	30,000	May 00
DAC	6.3	130	200	May 00
Delay	6.5	260	350	99
Calib logic	16	910	1500	May 00
BiMUX	4.6	8,320	11,000	99

Among these chips, the SCA controller is now the most critical and problematic in DMILL, a backup solution in 0.25 um is being considered.

Although avoided as much as possible, some COTS remain necessary (fast opamps, ADCs) for which the procurement plan and radiation qualification need to be finalized to minimize the associated risks.

The goal is now to produce the first final (radiation tolerant) ATLAS front-end board by mid 2001 and have a full crate (all board types) by spring 2002.

7. REFERENCES

The transparencies can be found on : http://atlasinfo.cern.ch/Atlas/GROUPS/LIQARGON/CONFERENCE/electalk.html

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