A Mixed−Signal ASIC for the Silicon Drift Detectors of the ALICE Experiment in a 0.25μm CMOS

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Abstract

A mixed−signal integrated circuit developed for the front−end of the Silicon Drift Detectors (SDDs) is presented. The chip contains 32 channels and 16 analogue to digital converters. Each channel is made of an amplifier and an analogue pipeline with 256 cells. One ADC is shared by two adjacent channels. The circuit has been optimized to match the specifications of the SDDs of the ALICE experiment, where large dynamic range and low power consumption are key issues. The input noise is calculated to be 200 e^- rms for a total input capacitance of 3pF and a detector leakage current of 10nA. The average power consumption is 4mW per channel.

I. Introduction

Silicon Drift Detectors [1] offer the advantage of a two−dimensional position measurement while requiring a reduced amount of processing electronics. These detectors are well suited for experiments in which a very high particle density is coupled with relatively low event rates, as is the case for heavy−ion experiments. For example, SDDs will be used in the two intermediate layers of the Inner Tracking System of the ALICE experiment.

In ALICE, the constraints on material budget, power consumption and noise make the design of the front−end electronics for the SDDs particularly challenging [2]. In fact, to achieve the required resolution (30μm in both coordinates) the noise should be limited to 250 e^- rms. The average power consumption (including also the digitization of the data) should be kept below 5mW per channel. Drift detectors are actually very sensitive to temperature variations and low power consumption is mandatory to have an efficient thermal stabilization with a minimum of refrigerant.

In order to improve the separation of close tracks, the shaping time of the amplifier should be less than 60 ns. Both computer simulations and experimental measurements have shown that in this case a sampling frequency of at least 30 MHz should be used [2]. In complex systems an early conversion of the data into a digital format is of course an advantage. Therefore in the SDD project it has been decided to embed the analog to digital conversion on the front−end chip and to perform any further signal processing in the digital domain. The tight constraint on power consumption prevents the use of a fast ADC immediately after the amplifier. Hence the amplifier's output must be sampled at the required rate by a low−power circuit; the stored analog samples are then digitized only if a trigger signal is received.

Table 1: Specifications of the front−end chip for the SDD[2]

Maximum input signal	32 fC
Target noise	250 e^- rms
Sampling frequency	40 MHz
Dynamic range	10 bits
Maximum read−out time	1 ms
Power dissipation	5mW/channel

This paper presents an ASIC developed to meet the requirements (summarized in table 1) of the front−electronics of the ALICE drift detectors. The chip provides amplification of the input signals, temporary storage of the analogue data in a 256 cell pipeline[1] and 10 bit analogue to digital conversion. The operations of the memory and of the ADC are controlled by a digital unit integrated on chip. The ASIC has been implemented in a commercial 0.25μm CMOS technology, using a radiation tolerant layout. This should guarantee immunity to radiation damage at least up to a total dose of 10Mrad (SiO_2), which is well beyond what is foreseen is ALICE (20krad in 10 years of operation). Section 2 of this paper describes with some details the different building blocks inside the chip. Section 3 presents the first experimental measurements, while conclusions are drawn in section 4.

II. Chip Architecture

The chip contains 32 front−end amplifiers. Each amplifier is connected to a row of the analogue memory. A 10 bit ADC converts the data stored in two rows of the pipeline into a digital representation. The choice of an ADC every two channels is a compromise between the modularity of the architecture (which makes the system more robust) and the area occupied on silicon. The chip is powered from a single rail 2.5 V supply.

[1] The number of cells in the pipeline is determined by the maximum drift time of the detector (6μs) divided by the period of the sampling pulse (25ns). Some more cells have been foreseen in order to accommodate possible variations of the parameters of the detector.

A. The amplifier

The scheme of the amplifier is depicted in fig. 1. In the circuit a classical two−stage topology has been used. Transistor M_f and capacitor C_f act as the integrating loop of the preamplifier. The pole introduced by this loop is canceled by the network formed by M_z and C_z [3]. The accuracy of the pole−zero cancellation relies on the matching between M_f and M_z and C_f and C_z, respectively. Hence, particular attention has been paid to this aspect. C_z and M_z are actually obtained by connecting in parallel a suitable number of copies (20 in our case) of C_f and M_f. Moreover, M_f and M_z should operate with the same DC voltages at their terminals. The voltages at the drains of M_f and M_z are determined by the main amplifiers A_1 and A_2. Therefore, to make the two voltages nearly equal, the same architecture has been chosen for both circuits.

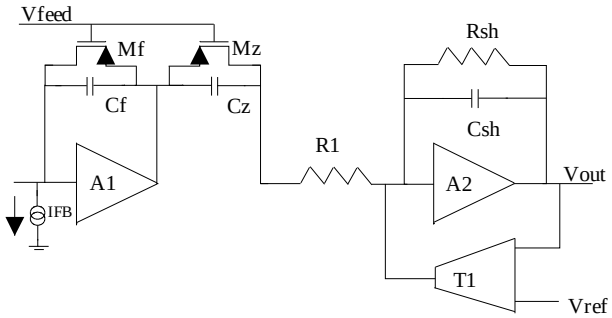

Figure 1: Block diagram of the front−end amplifier.

The topology used for the main amplifiers is shown in fig. 2a. For the purpose of explanation a conventional folded cascode is depicted in fig. 2b.

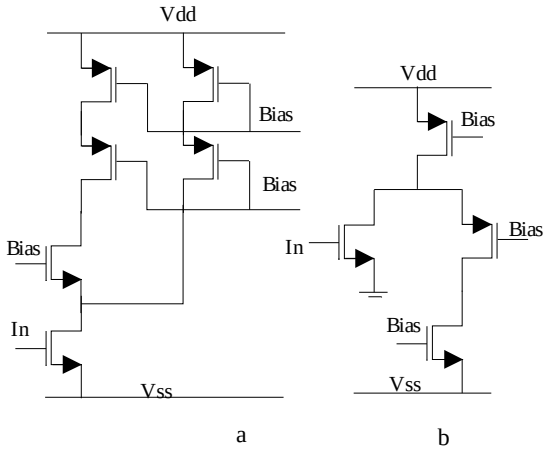

Figure 2: Circuit used (a) versus folded cascode (b).

The chosen architecture consists of a direct cascode with an additional branch for the biasing of the input transistor. This scheme offers two advantages with respect to the circuit of fig. 2b:

- The source of the input device can be connected directly to Vss and does not required any additional reference ("gnd") voltage. In principle, this could be done also for the conventional folded cascode. However, the input device would operate with an high drain−source voltage, making it sensitive to high field effects (e.g. hot carrier degradation).
- The current flowing into the input transistor is the sum (rather than the difference) of the current flowing in the two branches. Hence the structure of fig. 2a is more power efficient than the one of fig. 2b.

The use of the architecture of fig. 2a makes non trivial the implementation of a replica biasing scheme like the one proposed in [3] to fix the gate voltages of M_f and M_z in order to determine their operating points. This problem has been addressed by forcing a DC current into Mf via the current source IFB [4,5]. In this approach the gate voltage of M_f and M_z (indicated as Vfeed in fig. 2) becomes less critical, since it merely determines the DC output voltage of the preamplifier. The drawback is that the presence of the current source IBF at the input of the amplifier increases the parallel noise. In our case the contribution of IBF to the parallel noise has been calculated to be 50 electrons rms.

Two feedback loops have been implemented around the second stage. The first feedback loop is accomplished by the transconductor T_1 and acts at very low frequency. Its purpose is to fix the DC output voltage to the desired value, determined by the reference Vref. This loop compensates also for any DC contribution induced by the first stage, included the one due to the leakage current of the detector. The amplifier is, in fact, DC coupled to the sensor, whose leakage current flows into M_f and leaves the drain of M_z amplified by the ratio $(W/L)_{Mz}/(W/L)_{Mf}$=20. This current is absorbed by T_1 and does not offset the output of the overall amplifier. The second feedback loop is implemented by the resistor R_{sh} and the capacitor C_{sh} and introduces a real pole in the transfer function. A second real pole is created by resistor R_1 and capacitor C_z. The designed peaking time and gain of the amplifier are 35 ns and 40 mV/fC, respectively.

One of the key components in the amplifier is the output driver, which has to deliver large voltage swings

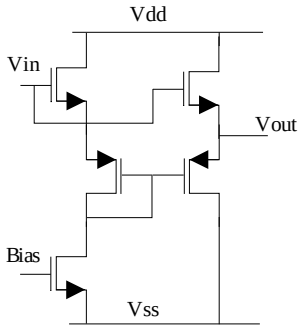

Figure 3: Class AB output buffer.

(ideally 1.4 Volt, the full scale range of the ADC). Moreover, the buffer must drive the capacitance of the analog pipeline (roughly 5 pF) with a minimum of power. Thanks to the availability in the chosen technology of zero threshold NMOS devices the output stage could be implemented as an elementary class AB source follower (see fig. 3). Despite its simplicity, the circuit has a voltage

swing in excess of 1.5 Volt and dissipates only 400 µW. The nominal power consumption of the overall amplifier is 1.8 mW/channel.

B. The analog memory

The output signal of the amplifier is sampled at a frequency of 40 MHz by a 256 cells analog pipeline. The pipeline is an evolution of a design we had previously developed in the framework of the RD49 collaboration and described in detail in [6]. The RD49 design has been adapted to this project by increasing the number of cells from 128 to 256 and the number of channels from 8 to 32. The schematic diagram of the memory is shown in fig. 4.

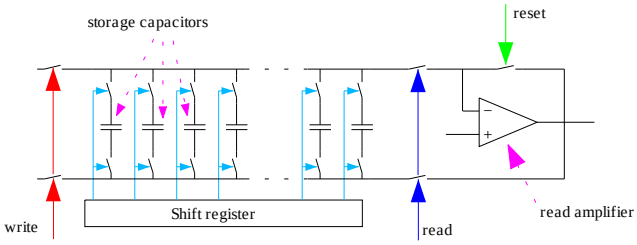

Figure 4: Analog memory schematic.

The sampling capacitors have been implemented as high density MOS capacitors. To minimize the impact of the poor linearity of the MOS structure, the information is processed in the pipeline only in the voltage domain. One plate of the capacitor is formed by the polisilicon normally used in the gates of standard transistors, whereas the other plate is the nwell. The device works in the accumulation region and the CV curve is optimal (i.e. the voltage dependence is minimal) above 1 V. In order to use as much as possible the linear region, the DC value of the baseline of the front−end amplifier is set to 1.9 V [2] and the signals are written from this value downwards. In this way, the smallest signals, which are more critical, are stored in the more linear region.

C. The analog to digital converter

The ADC, whose block diagram is shown in fig. 5, had been previously developed as a single component in the context of RD49 [7]. In the converter a successive approximation scheme has been used [8]. This architecture has been selected because it offers an excellent compromise between power consumption, area and resolution. The circuit is based on a switched capacitor DAC and an offset compensated comparator. The capacitors in the DAC are binary weighted, in order to generate binary fraction of the reference voltage VREF, which are compared to the signal to be digitized.
The main goal in the design was to keep the DAC within a reasonable size, suitable for the integration of many channels on a single die. In this kind of circuit, in fact, the size of the DAC doubles for any extra bit of resolution required and becomes cumbersome for resolutions above 8 bits. The known solution to overcome the problem is to scale down the voltage on the bottom plates of the terminating capacitor, providing further division of the reference voltage [9]. We have implemented this concept using a second charge redistribution DAC, as shown in fig. 5. The second DAC is connected directly to the first one and is used to determine only the two last bits. In this approach, of course, the second DAC loads the main stage, so that the termination capacitance, instead of C, is the series combination of C and the total capacitance of the second DAC. The result is a loss in linearity, which however can be kept irrelevant at the 10 bit level by an adequate oversizing of the sub−DAC.

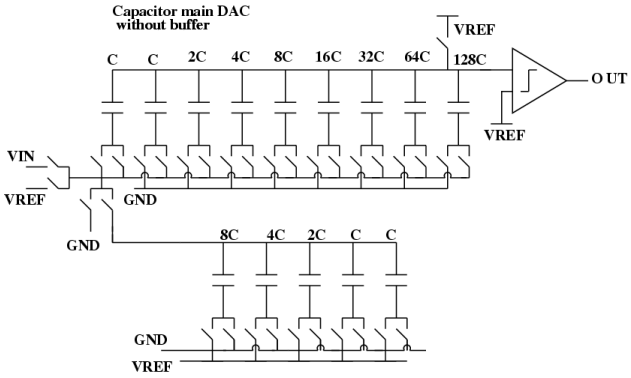

Figure 5: ADC schematic.

The ADC decides one bit per clock cycle. Hence the time needed for one conversion is ten clock cycle plus the time required to sample the input signal. In the first prototype full functionality was achieved up to a clock frequency of 20 MHz, while few codes were missing at higher frequencies. The resistivity of the reference lines has been identified as the limiting factor and care has been paid in this version to improve the distribution of the reference voltages [7].

The maximum full scale range of the ADC is about 2/3 of the power supply voltage (that in our case is 2.5). This condition can easily be deduced by imposing that the voltage at the interface between the DAC and the comparator never exceeds the power supply rail during operation. The amplifier, however, provides useful signals in the range 1.9 V − 0.5 V. The upper limit is defined by the analog memory and the optimum bias of the second stage of the amplifier. The lower limit is fixed by the output driver and corresponds to the level at which the output PMOS device switches off. The output dynamic range of the amplifier is therefore close to the maximum full scale range of the ADC. In order to efficiently use the dynamic range of the converter two solutions are possible. The first option is to perform a voltage translation before the ADC. The second one is to operate the converter with a dual reference voltage, setting the terminal indicated as VREF in fig. 5 to 1.9 V and the terminal indicated as "GND" to 0.5 V. Both configurations are possible in the present chip.

All the signals needed to control the ADC as well as the memory can be supplied either by the internal control unit or by an external pattern generator.

[2] This value, infact, allows the cascode load of the main amplifier (see fig. 2a) to work properly in saturation with a reasonable safety margin.

III. Experimental results

In order to facilitate the tests, the building blocks in one channel can be accessed directly, so that they can be measured individually. At the time of writing the tests are in a early phase and only preliminary results on these circuits are available. The first measurements, however, already demonstrate that important design goals have been achieved.

A. Results on the amplifier

As we have seen in the previous section, one of the critical aspects in the design of the amplifier was to achieve an output swing adequate to exploit as much as possible the dynamic range of the converter. The useful output range of the amplifier is defined as the interval in which the nonlinearity is less than 5% and is shown in fig. 6. As can be seen from this picture, the amplifier can deliver a maximum signal in excess of 1.3 V, in good agreement with Spice simulations.

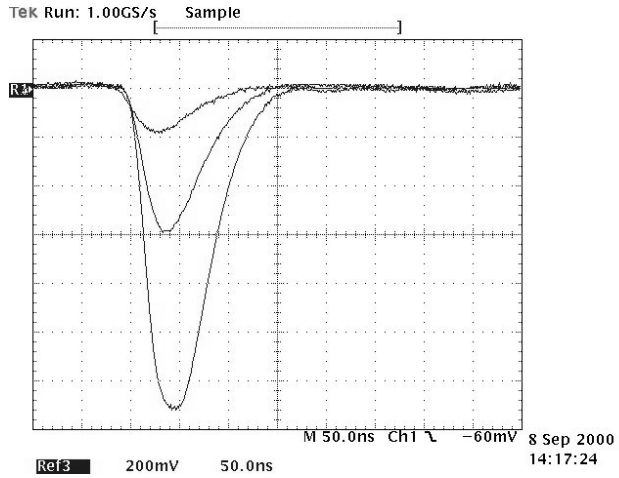

Figure 6: Output dynamic range of the amplifier

The return to the baseline is fast and without remarkable overshoots or tails also for the biggest signal. This is an indication of the good performance of the pole−zero cancellation network. The measured shaping time is 37 ns and the gain is 41 mV/fC.

The baseline settles very close to the predicted value. With a reference voltage of 1.9 V the simulated DC output is 1.899 V. The measured values range in the interval 1.895 − 1.897 V. The spread is due to the offset in the differential input stage of the low frequency transconductor and can be reasonably understood on the basis of matching considerations. An idea of the DC behavior of the baseline is given in fig. 7, where the output signal is DC coupled to the oscilloscope[3]. The zero Volt is indicated by the marker in the lower part of the figure. The two traces in fig. 7 correspond to the same input signal measured with two different values (0 V and 1 V) of the feedback voltage Vfeed (see fig. 1). As expected, the big change in this bias voltage has only minor effects on the output, since the feedback elements are biased in current. First noise measurements show a noise of 260 electrons rms at 3pF input capacitance.

All the measurements have been performed with the nominal bias and hence the nominal power consumption (1.8 mW/channel).

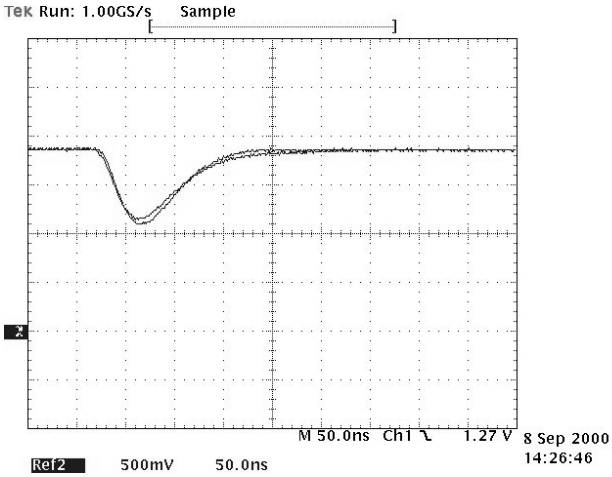

Figure 7: Output of the amplifier for different values of Vfeed

B. Results on the ADC and the analog memory

The test strategy is to perform first a detailed characterization of the ADC and then to measure the analog memory through the converter itself. Hence, only qualitative tests have been carried−out on the pipeline to verify the basic functionality[4] of the circuit.

The test set−up for the ADC is based on an arbitrary waveform generator and a logic state analyzer. In the test procedure, a full−scale sinewave has been sent to the converter. The output data have been stored in a computer and analyzed with the FFT method and the histogram method. As an example, fig. 8 shows a typical DNL pattern. In this case the input was a 5.5 kHz sinusoid and the reference voltages were adjusted to 1.9V and 0.5 V.

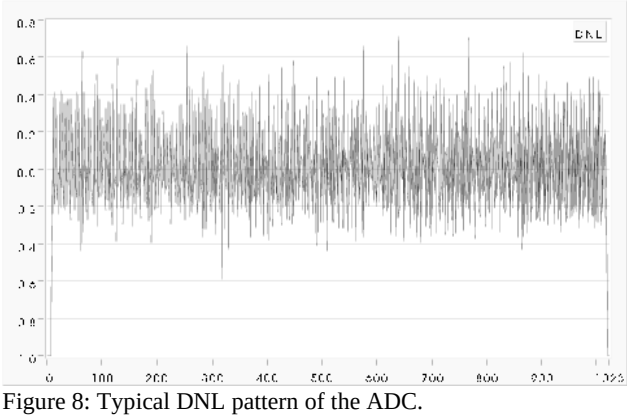

Figure 8: Typical DNL pattern of the ADC.

The clock frequency was 30 MHz and the signal was sampled at a rate of 1.5 Megasample/s, which would allow to read the analog memory in 380 µs.

The DNL is 0.6 LSB and the ADC has no missing codes. The integral nonlinearity (INL) is 4 LSB or 0.4%

[3] A unity gain commercial buffer is used to drive the connection to the instrument.

[4] By " basic functionality" we mean here that the pipeline responds correctly to the control signals and the power consumption is in the predicted range.

of the full scale range. The measurements have been performed with all the 16 ADCs working simultaneously. The ADC provides a 10 bit resolution up to a frequency of 35 MHz. Beyond this value, the last bit of the code becomes non significant. However is not clear at the moment if this degradation in performance is due to the converter or to parasitic effects in the set−up (e.g. inductive noise on the reference lines) which may come into play at those frequencies.

IV. Conclusions

A complete front−end chip for the Silicon Drift Detectors of the ALICE experiment has been designed and produced. The ASIC has been implemented in a commercial 0.25μm CMOS process using a radiation tolerant layout approach. In an area of 6 x 7 mm^2 the chip integrates 32 analogue channels (amplifiers + pipeline) and 16 ADCs.

First tests on the individual building blocks have been carried out and show that all the parts are functional. More accurate measurements have been performed on the front−end amplifier and on the analog to digital converter.

The amplifier features a peaking time of 37 ns, an output voltage swing of more than 1.3 V and an excellent return to the baseline. The gain is 41 mV/fC.

The ADC exibits a 10 bit resolution up to a clock frequency of 35 MHz, which allows to read−out the memory in 380 μs.

The chip is powered from a single rail 2.5 V supply and dissipates an average power of 4 mW/channel.

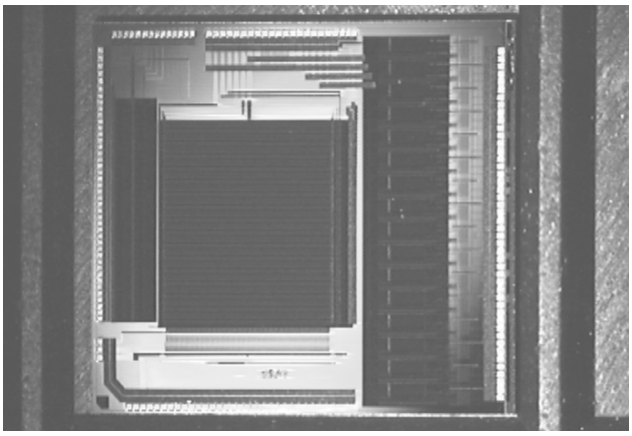

Figure 9: Picture of the developed ASIC

V. References

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