The CMS Tracker APV25 0.25 µm CMOS Readout Chip

M.Raymond[a], G.Cervelli[b], M.French[c], J.Fulcher[a], G.Hall[a], L.Jones[c], L-K.Lim[a], G.Marseguerra[d], P.Moreira[b], Q.Morrissey[c], A.Neviani[c,d], E.Noah[a]

[a]Blackett Laboratory, Imperial College, London, UK
[b]CERN, 1211 Geneva 23, Switzerland
[c]Rutherford Appleton Laboratory, UK
[d]INFN, Sezione di Padova, and Universita di Padova, Italy

Abstract

The APV25 is the readout chip for silicon microstrips in the CMS tracker. It is the first major chip for a high energy physics experiment to exploit a modern commercial 0.25µm CMOS technology. Experimental characterisation of the circuit shows full functionality and excellent performance before and after irradiation. Automated probe testing of many chips has demonstrated a very high yield. A summary of the design, detailed results from measurements, and probe testing results are presented.

I. INTRODUCTION

The CMS tracker contains approximately 10^7 channels of AC coupled silicon microstrips read out by 128-channel APV25 chips. The APV chip series has included versions in both Harris [1] and DMILL [2] technologies. The APV25 is fabricated in a 0.25µm CMOS process, the thin gate oxide together with special layout techniques ensuring radiation tolerance [3].

Two versions of the APV25 have now been fabricated. Because of the requirement to expedite the development to meet the experiment construction schedule, it was decided to opt for a full-size chip in the first iteration, integrating all the features required for the CMS tracker. Although this strategy has some associated risks, much experience had been gained from designing previous versions of the chip in other processes, and while testing building blocks of a design in isolation does yield detailed knowledge of their operation, more subtle problems (usually layout related) reveal themselves only when sub-circuits are integrated together.

Delivered in October 1999, the APV25s0 was found to demonstrate very good performance in all aspects of the design and the radiation tolerance exceeded requirements. Minor deficiencies were found to be uniformity of the on-chip generated calibration signal, lower overall gain than that designed for, and an internal digital timing error which was completely transparent to the user. The noise performance was satisfactory but non-uniform, showing a dependence on channel number. This was identified as arising from non-negligible metallisation resistance, where tracks from input pads at the bottom edge of the chip had further to go to reach their respective preamplifier inputs than those at the top.

Approximately 500 chips from 4 wafers were available for probe testing from the APV25s0 chip version. An automatic test facility has been developed which will allow wafer screening of die during the production period. This is described in section V, where results illustrating uniformity and yield characteristics of the process are included.

Figure 1 shows the layout of the APV25s1, the second version of the chip, delivered in September 2000. Only a few chips have been tested so far, but the performance has already been verified to be consistent with that exhibited by the s0 version, except for the areas in which it has improved. The results in sections III and IV of this paper are exclusively from the new APV25s1 version of the chip.

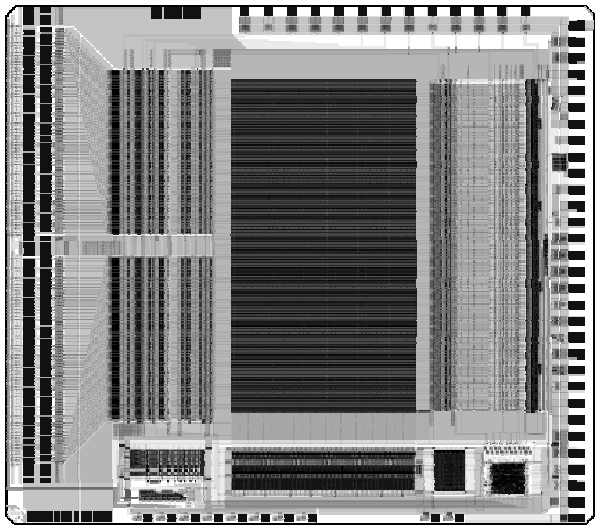

Figure 1. Layout of the APV25s1 chip

II. APV25 DESIGN FEATURES

The APV25s1 chip dimensions are 7.1 mm from top to bottom edge (as viewed in figure 1), and 8.1 mm from front to back. The 128 input pads are split into two groups of 64, with power pads at the top, bottom and between the two groups. Power can also be provided from pads on the top and bottom edges, if it is not necessary to achieve minimum separation between chips on a hybrid. The remaining pads on the top and bottom edges are for test purposes and are not required to be bonded. Most of the pads on the back edge of the chip are required to be bonded for normal operation, and for details of dimensions and pad assignments see the user manual [4].

Details of the design of the APV25 have been previously published [5] so only a brief description will be given here. Each channel consists of a preamplifier (preamp) coupled to a shaping amplifier (shaper) which produces a 50 ns CR-RC pulse shape. A unity gain inverter is included between the preamp and shaper which can be switched in or out such that the polarity of signals at the shaper output is the same for either polarity of detector signals.

The shaper output of each channel is sampled at 40 MHz into a 192 cell deep pipeline. The pipeline depth allows a programmable level 1 latency of up to 4 μs, with 32 locations reserved for buffering events awaiting readout. If the chip is triggered the appropriate pipeline cell columns (time slices) are marked for readout, and not overwritten until this is completed. Each channel of the pipeline is read out by a circuit called the APSP (Analogue Pulse Shape Processor) which can operate in one of two modes. In *peak* mode only one sample per channel is read from the pipeline (timed to be at the peak of the analogue pulse shape). In *deconvolution* mode three samples are sequentially read and the output is a weighted sum of all three. The deconvolution operation results in a re-shaping of the analogue pulse shape to one that peaks at 25 ns and returns rapidly to the baseline.

After the APSP operation is completed the output is sampled/held and fed to the multiplexer. This 128:1 stage operates at 20 MHz and uses a nested architecture to save power (only the final 4:1 stage runs at full speed), resulting in a non-consecutive channel order for the analogue samples.

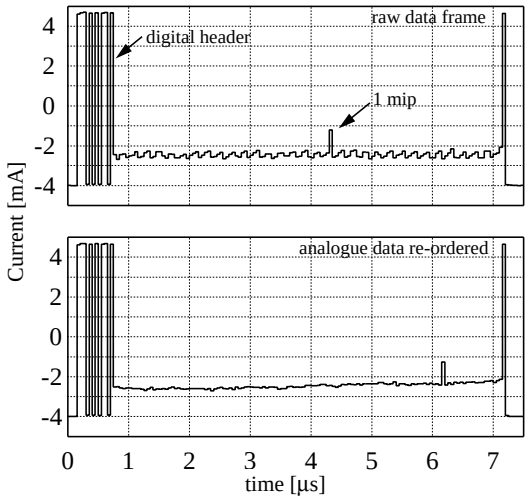

Figure 2. APV25 output data frame

Figure 2 shows the APV25s1 output data stream following a trigger. The output is a differential current, figure 2 showing the positive output only. The upper plot shows the raw data frame after digitisation. The overall frame length is 7 μs, comprising a 12 bit header followed by 128 50 ns analogue samples. A 1 mip (24,000 electrons) signal is injected into one of the chip inputs. The 12 bit header comprises 3 start bits, an 8 bit address of the pipeline column from which the data originates, and one error bit. The lower plot in figure 2 shows the same frame but with the analogue data in channel order (from the bottom to top of the chip as viewed in figure 1). In this plot a slight pedestal gradient can be seen which is likely to be due to a power supply droop across the chip.

The digital header is designed to occupy approximately an 8 mip range. The analogue baseline can be adjusted using the slow control interface to lie anywhere within that range, allowing a reasonable signal dynamic range (~ 5mips) plus headroom to accommodate common mode effects.

The 40 MHz clock and trigger (T1) signals to the chip use the LVDS standard. A single '1' on the T1 line is interpreted as a normal trigger, which are required in CMS to be separated by a minimum of 2 clock cycles. Making use of this trigger rule the chip interprets two triggers separated by only one clock cycle ('101') as a synchronous reset, and two triggers with no separation ('11') as a calibration request.

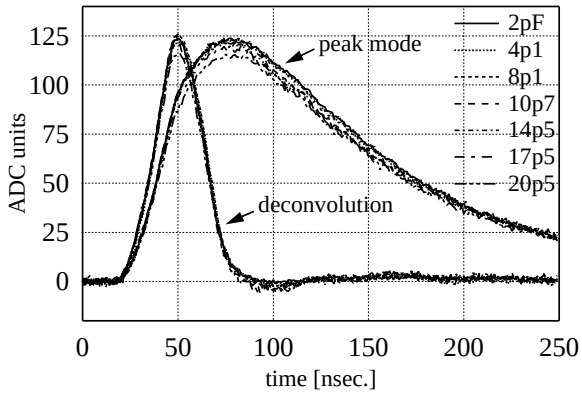

Figure 3. APV25s1 amplifier pulse shape in peak and deconvolution modes, for a range of input capacitance

III. APV25s1 PERFORMANCE

A. Analogue pulse shape and linearity

Figure 3 shows the amplifier pulse shape measured for a bonded out channel as a function of input capacitance, in both peak and deconvolution modes. The pulse shape is mapped by sweeping the time of charge injection with respect to a fixed T1 time. The peak mode pulse shape closely approximates to an ideal CR-RC pulse shape with a 50 ns time constant, and consequently the deconvolution mode pulse shape is close to ideal. The independence of pulse shape on input capacitance is achieved by minor adjustment of shaper amplifier biases to compensate for preamplifier risetime effects.

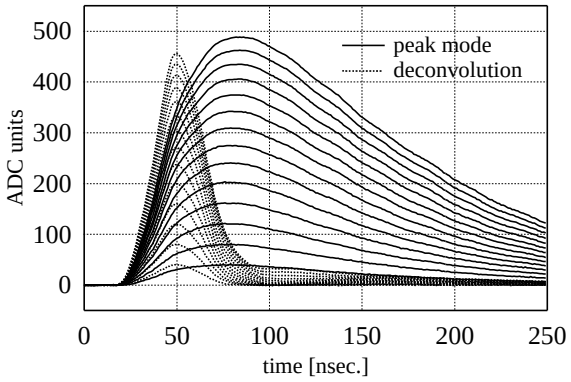

Figure 4. APV25s1 pulse shape dependence on signal amplitude in both peak and deconvolution modes

Figure 4 illustrates the pulse shape dependence on signal amplitude in both peak and deconvolution modes. The input signal varies between 0.5 and 7 mips in 0.5 mip steps. No major distortion is evident for signals in this range. The dependence of the peak pulse heights from figure 4 on input signal amplitude is shown in figure 5, where the output signal amplitude has been normalised to the input signal amplitude at the 1 mip point. Good linearity is achieved for signals up to 3 mips with a gradual fall off beyond.

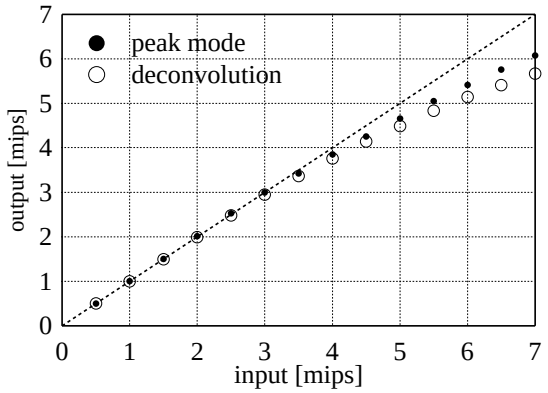

Figure 5. APV25s1 linearity

B. Internal calibration and gain uniformity

The deconvolution mode approach to pulse shaping relies on the bare amplifier pulse shape being a close approximation to the ideal CR-RC shape. The internal calibration circuit allows the pulse shape to be periodically monitored over the lifetime of the experiment, so that any necessary adjustments can be made. An on-chip pulse generator can be enabled to inject charge with programmable amplitude into all inputs in groups of 16 channels. Coarse resolution pulse shape mapping can be achieved by stepping the calibration request signal in 25 ns increments with respect to the subsequent trigger. Finer resolution is available using an on-chip delay circuit which can be programmed in steps of 3.125 ns.

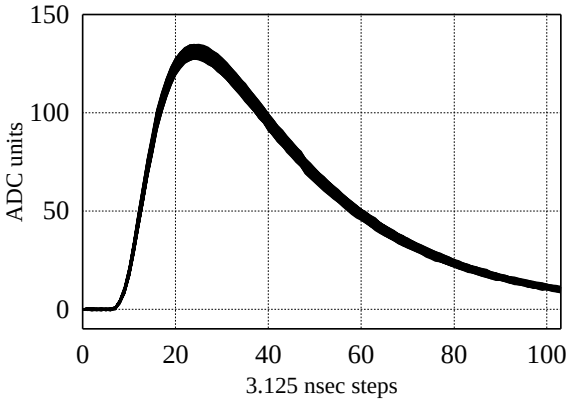

Figure 6. APV25s1 amplifier peak mode pulse shape for all 128 channels, measured using the internal calibration feature

Figure 6 shows the pulse shape in peak mode for all 128 channels superimposed, measured using the internal calibration circuitry. Good uniformity indicates that both channel gain and calibration signal matching are good. This is an improvement on the first version of the chip where a better layout of the calibration circuitry along the input edge of the chip has been implemented.

C. Noise

The first version of the chip showed noise dependence on channel number with channels at the bottom edge (low number channels) exhibiting higher noise. Figure 7 shows the noise dependence on input capacitance for the APV25s1 in peak and deconvolution modes for three channels, one close to the middle, the other two close to the top and bottom edges. The measured noise is consistent with that achieved for the previous chip version, and no significant difference between channels is observed. The noise target performance for silicon microstrips in CMS is 2000 electrons and from figure 8 we can see that this can be achieved (assuming amplifier noise alone) for detectors with capacitance up to 25 pF.

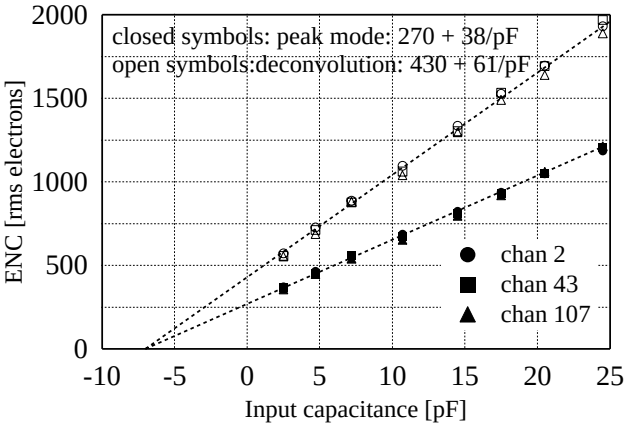

Figure 7. APV25s1 noise dependence on input capacitance

D. Pipeline tests

The APV25 pipeline is realised using gate capacitance of NMOS transistors biased in strong inversion. Uniformity of pipeline cell capacitance is necessary to avoid variations in channel pedestals depending on pipeline location which lead to additional noise sources. Figure 8 shows the pedestal dependence of a single channel on pipeline location. Taking the rms pedestal value, converting the result to an equivalent noise charge, and histogramming the results for all channels results in the picture shown in figure 9. It is clear that the pipeline pedestal contribution to the noise is negligible in both modes of chip operation.

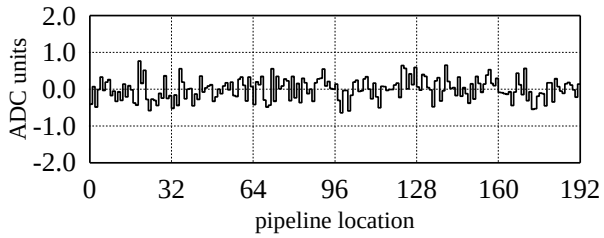

Figure 8. APV25s1 pipeline pedestals for a typical channel

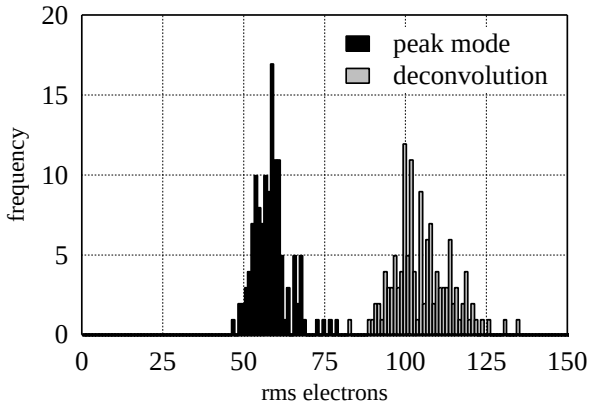

Figure 9. rms pipeline pedestals for all 128 channels

Another way of evaluating pipeline cell capacitance uniformity is to measure the gain dependence on pipeline location. This can be achieved by storing and retrieving a signal to and from every pipeline location. Figure 10 shows a histogram of the gain for all 192 pipeline cells for one channel. The width of the distribution is small indicating close matching of capacitance between cells.

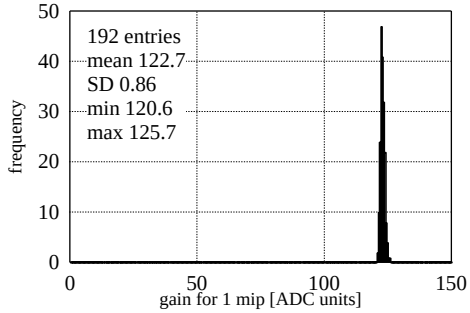

Figure 10. Pipeline gain uniformity

IV. RADIATION TESTS

The APV25 has been designed using the techniques investigated by the RD49 collaboration [3] to ensure radiation tolerance. The first version of the chip, and associated test structures have been irradiated with X-rays, ^{60}Co γ-rays, electrons and neutrons [6] to levels well in excess of those to be experienced in CMS, without suffering significant degradation of performance. In addition, chips have been exposed to a heavy ion beam, primarily to investigate SEU effects [7], but where no permanent damage due to gate breakdown effects has been observed. Due to lack of time only one chip from the APV25s1 run has so far been irradiated, but results from this chip are consistent with those from the previous run.

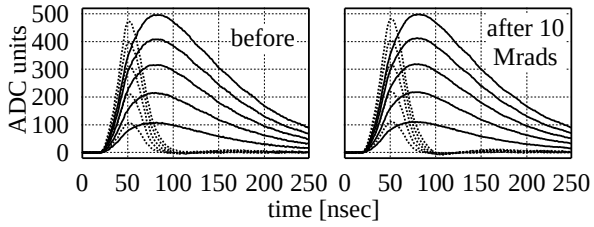

Figure 11. APV25s1 pulse shapes before and after irradiation

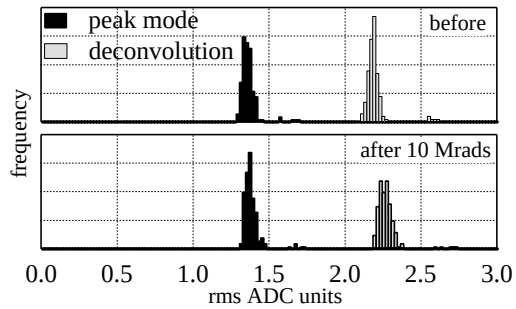

Figure 12. APV25s1 noise before and after irradiation

The APV25s1 chip was irradiated in 1 step to 10 Mrads with 50 kV X-rays (spectral peak at 10 keV) at a dose rate of 0.6 Mrads/hour. Figure 11 shows the pulse shapes recorded before and after irradiation. Minor tuning of bias parameters is required to maintain the post-irradiation pulse shape identical to the pre-irradiation shape. Figure 12 shows histograms of the noise for all 128 channels, in peak and deconvolution modes, before and after irradiation, where no significant noise degradation is apparent. The small group of channels for each distribution that sit at higher noise values are those which have been bonded out onto the test board and which therefore see a higher capacitance.

V. APV25s0 PROBE TESTING

The CMS tracker detector module production procedure requires the mounting of known good die on readout hybrids, to avoid a significant amount of hybrid re-work. It is therefore desirable to perform as exhaustive a test as possible on chips prior to mounting, which can be done using a probe card before the chips are cut from the wafer. Test set-ups and protocols, previously developed for earlier versions of the APV [8], have been adapted for use with the APV25.

Four wafers were available from the APV25s0 multi-chip production run, from which 501 chips were used for the probe test study. These chips had already been cut from the wafers, so manual alignment to each chip was required. An APV25s0 chip under test can be seen in figure 13, and a brief summary of the test protocol will now be given.

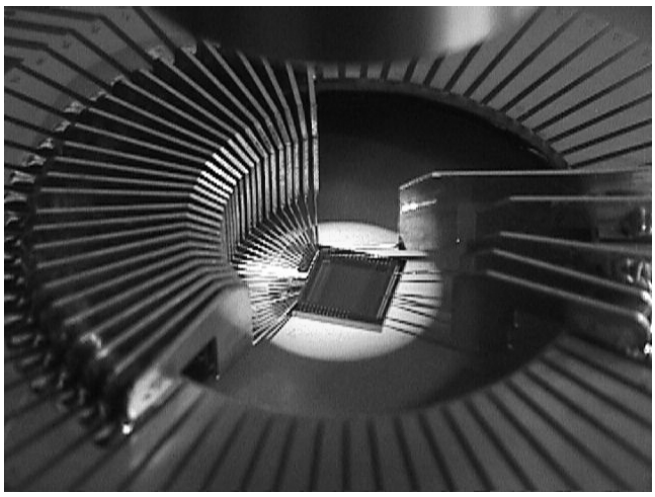

Figure 13. APV25s0 chip under probe test

A. Digital functionality tests

During the test the chip is operated at the 40 MHz LHC clock speed. The digital functionality tests include:

1) Read/write operations to all internal addresses (bias and operational mode registers) looking for stuck bits.

2) Verification that the chip will respond to all possible chip addresses (up to 31 chips can share the same I2C slow control bus with individual addresses determined by bonding)

3) Checking for the expected digital header and verifying no error bit is set after 1000 pseudo random triggers.

Any digital error found during the above tests results in the chip being recorded as a failure and 33 of the 501 chips tested were failed in this category.

B. Power supply currents

The power supply currents were measured after programming default values to the bias registers. Figure 14 shows two plots, one a histogram of the currents in both rails and the other a scatter plot of the current in the VSS rail against that in the VDD rail. The rectangular box in the second plot indicates where pass/fail thresholds were set for this test. Only 6 chips were failed solely on the power supply currents being out of range, but it is clear from figure 14 that the pass/fail thresholds can be made more stringent without significant impact on the overall yield.

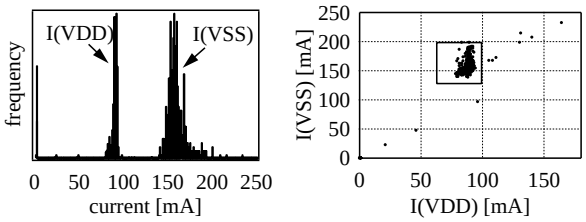

Figure 14. VDD and VSS currents for all probed APV25s0 chips

C. Pipeline tests

The integrity of the pipeline is evaluated by acquiring the pedestal values for all 192 cells for all 128 channels. The symptom of a faulty cell is a pedestal value which is stuck at an abnormally high or low value. This is easily observed and a chip fails this test if only one cell is found faulty. A total of 12 chips were failed in this category.

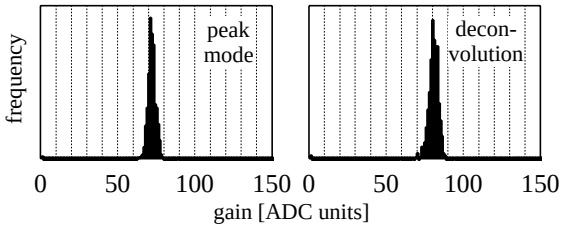

Figure 15.Gain histograms for good probed APV25s0 chips

D. Channel pedestals and calibration

The analogue baseline is adjusted to a nominal value and the pedestals for each channel are acquired and compared with the nominal value. A chip with an abnormally high or low value is failed. The analogue pulse shapes for all channels are acquired using the internal calibration facility. Chips with channels exhibiting low gain are failed. These tests are performed in both peak and deconvolution modes. A total of 26 chips were failed due to bad channel pedestals or gains. Figure 15 shows histograms of the average gain, in peak and deconvolution, for all the chips which passed all tests. The histograms indicate good gain matching between chips from all 4 wafers, although it should be noted that these wafers all came from the same run and that run to run differences are likely.

The overall results of the APV25s0 probe testing are summarised in table 1. A total of 419 out of 501 chips passed all tests, giving a yield for this run of 84%, with no significant differences between wafers

Table 1. APV25s0 probe test results summary (numbers in brackets indicate no. of chips in that category which showed cutting damage)

TEST DESCRIPTION	# of fails
digital functionality	33 (1)
power supply current out of range	6
pipeline defects (>0 bad cells)	12
channel defects (pedestals or pulse ht.)	26 (5)
physically damaged during probing	2
rejected due to visible cutting damage	3
TOTAL NO OF FAILURES	82

.

VI. CONCLUSIONS

The APV25s1 0.25µm CMOS readout chip for the CMS microstrip tracker has so far shown excellent performance on the test bench, and detector modules built using the previous version of the chip have demonstrated performance consistent with laboratory measurements. Further testing is envisaged as well as detector module construction and evaluation.

Probe testing of a substantial number of chips from the first APV25 run has demonstrated a yield of 84%.

VII. ACKNOWLEDGEMENTS

We would like to acknowledge technical support at Imperial College, particularly Sarah Greenwood and Maria Khaleeq. We would like to thank the UK Particle Physics and Astronomy Research Council for supporting this work.

VIII. REFERENCES

[1]The APV6 readout chip for CMS microstrip detectors, M.Raymond et al, Proceedings of 3rd workshop on electronics for LHC experiments, CERN/LHCC/97-60,158-162

[2]Characterisation of the APVD readout circuit for DC coupled silicon detectors, U.Goerlach et al, these proceedings

[3]Deep submicron technologies for HEP, A.Marchioro, Proceedings of 4th workshop on electronics for LHC experiments, CERN/LHCC/98-36,40-46

[4]APV25s1 user manual, http://www.te.rl.ac.uk/med/

[5]The APV25 deep submicron readout chip for CMS detectors, L.Jones et al, Proceedings of 5th workshop on electronics forLHC experiments,CERN/LHCC/99-09,162-166

[6]Total dose irradiation of a 0.25µm process, E.Noah et al, these proceedings

[7]Single event upset studies on the APV25 readout chip, J.Fulcher et al, these proceedings

[8]Wafer testing of APV chips for the CMS tracker, J.Fulcher et al, Proceedings of 4th workshop on electronics for LHC experiments, CERN/LHCC/98-36,196-200