Progress in Development of the Readout Chip for the ATLAS Semiconductor Tracker.

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Abstract

The development of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS Semiconductor Tracker has entered a pre-production prototyping phase. Following evaluation of the ABCD2T prototype chip, necessary correction in the design have been implemented and the ABCD3T version has been manufactured in the DMILL process. Design issues addressed in the ABCD3T chip and performance of this pre-production prototype are discussed.

I. INTRODUCTION

The ABCD design is one of the two options of the binary readout architecture which have been developed for the ATLAS SCT [1-3]. Recently, based on the performance of the ABCD2T prototype, this option has been chosen as a baseline. The ABCD chip developed and manufactured in the DMILL process comprises in a single chip all blocks of the binary readout architecture; the front-end circuit, discriminator, binary pipeline, derandomizing buffer, data compression logic, and the readout control logic, as required for the ATLAS SCT.

For the binary architecture one of the most critical issues is the uniformity of parameters of the front-end circuit and matching of the discriminator threshold. A major improvement of the ABCD2T performance has been achieved by implementation of individual threshold correction in every channel using a 4-bit digital-to-analogue converter (TrimDAC) per channel.

The ABCD2T version has met all basic requirements of the ATLAS SCT, however, detailed evaluation of the ABCD2T chips, including extensive radiation testing, pointed to some possible improvements. These improvements, which concern mainly improvement of the radiation resistance and reduction of the design sensitivity to variation of the process parameters, have been implemented in the ABCD3T version. The later aspect is important for large volume production as it may impact the production yield.

An overview of the ABCD architecture and of the performance of the ABCD2T prototype can be found in earlier publications [1,4]. In this paper we focus mainly on the specific issues which have been addressed in the ABCD3T design.

In the front-end circuit of the ABCD2T we have identified two points which compromised slightly performance of that prototype, namely: (i) the internal calibration circuitry showed non-linearity for low input charges, (ii) TrimDACs response curves appeared to be non-linear and exhibited large spread from channel-to-channel. The non-linearity of the calibration circuitry, although not critical, makes the calibration procedure more complicated than necessary. The source of the non-linearity has been identified as parasitic charge injection from CMOS switches employed in the calibration circuit.

A non-linear response of the TrimDAC is not a serious problem as the trimming procedure is based on measurement of the TrimDAC characteristics and using these results in a look-up table. A consequence of the non-linearity is a slightly worst matching of the threshold compared to what one can expect assuming perfectly linear response curves of this circuit. More important, however, is that TrimDACs in some channels become so non-linear that those channels fall outside the trimming range. Since for good chips we require all the channels to be within the specification that effect, if not corrected, would impact significantly the yield in the production. The source of the problem has been identified in the design and an easy correction has been found.

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II. FRONT-END PERFORMANCE

Basic performance of the front-end circuit in the ABCD design, in particular the noise, has been discussed in previous papers. In this paper we focus on the two issues, which have been improved in the ABCD3T design compared to the ABCD2T, i.e. linearity of the calibration circuit and TrimDAC characteristics.

A. Internal calibration circuit

Internal calibration circuit is foreseen to be used at various steps of chip testing and module testing as well as for threshold calibration in the experiment. A first purpose of this circuit is providing testability of the chip. It allows to take measurements of analogue parameters; gain, noise, offset, time walk and TrimDAC characteristics for every channel during of wafer screening without supplying a precise analogue signal to the chips. All these measurements are then repeated for complete modules equipped with 12 ABCD chips each.

For the binary architecture as implemented in the ABCD design the linearity of the front-end circuit is not a critical issue. However, a good absolute precision is required for setting the working threshold in the discriminators which impact the efficiency and noise occupancy. The threshold setting will be based on calibration using internal calibration circuit and so the precision of this circuit around the nominal threshold setting, i.e. 1 fC, is a key issue. As mentioned before the calibration circuit in the ABCD2T design exhibited non-linear behaviour for low input charges which has been identified as parasitic charge injection in the chopper circuit.

The response curves for 128 channels in one chip measured using internal calibration circuit are shown in Fig.1. The measurements were taken starting with an input charge of 0.5 fC of the input charge. The points at 0 fC obtained from the noise occupancy scan are included in the plot. The response curves are satisfactorily linear within a range between 0.5 fC and 4 fC which allows to use simple linear fits when performing calibration of the threshold in the range around 1 fC.

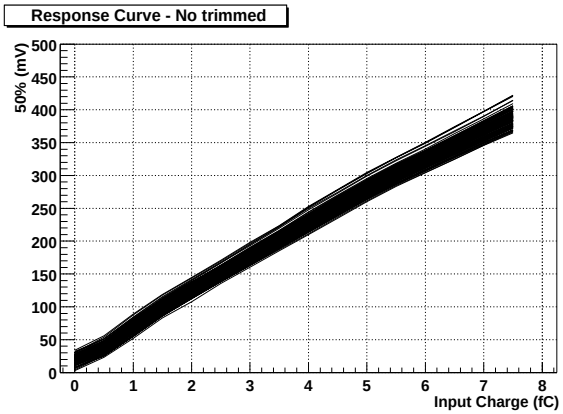

Figure 1: Response curves for 128 channels in one ABCD3T chip before threshold correction.

B. TrimDAC

The TrimDAC circuit as implemented in the ABCD2T chip has been proved to be an efficient solution to correct the threshold spread. The functionality of this circuit has been demonstrated [1], however, its performance could still be improved. First, the characteristics of the TrimDACs exhibited large non-linearity. The source of the non-linearity has been identified and a simple correction, without changing the concept of the circuit, has been implemented in the ABCD3T design. Second, radiation tests showed that the spread of the discriminator offset increased significantly after irradiation and exceeded the range of the TrimDACs. In order to not compromise the precision of threshold correction for non-irradiated chips and to guarantee that for fully irradiated chips all the channels can be corrected, a set of ranges has been implemented in the ABCD3T design.

Fig. 2 shows the characteristics of the TrimDACs for 128 channels in one ABCD3T chip for the minimum range set. One can see that the characteristics are satisfactorily linear given the 4-bit resolution of the TrimDAC. The minimum range of the TrimDAC is sufficient to cover the discriminator offset spread. Fig. 3. shows the characteristics of the TrimDAC in a single channel for 4 different range sets.

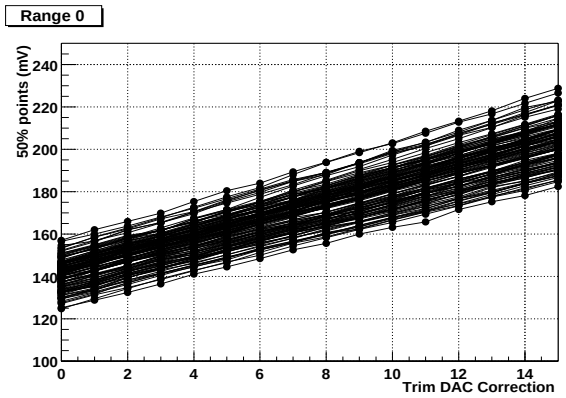

Figure 2: Typical characteristics of the TrimDACs for 128 channels in the ABCD3T chip

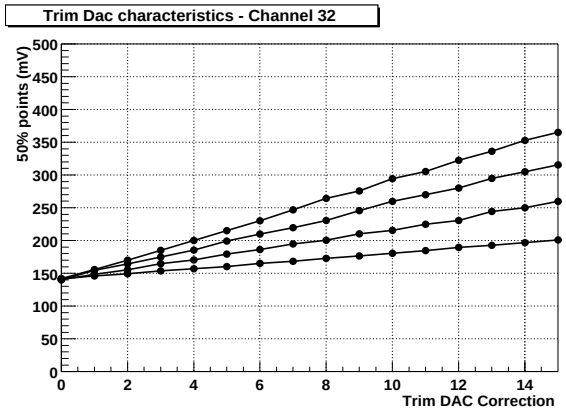

Figure 3: Characteristics of the TrimDAC in a single channel for four different range sets.

In order to confirm the functionality and performance of the TrimDACs we performed the trimming procedure as it is foreseen in the experiment. The distribution of the threshold in 128 channels in one chip for 1 fC input charge is shown in Fig. 4. The rms value is 7.4 mV. The same distribution after threshold correction is shown in Fig. 5. The spread has been reduced now down to 1.5 mV rms which is the value one can expect given the TrimDAC step of 4 mV. The spread of the threshold is equivalent to ENC of 180 e^- rms, which is completely negligible compared to the typical noise of 1400 e^- rms for a module with long silicon strips, as foreseen for the ATLAS SCT.

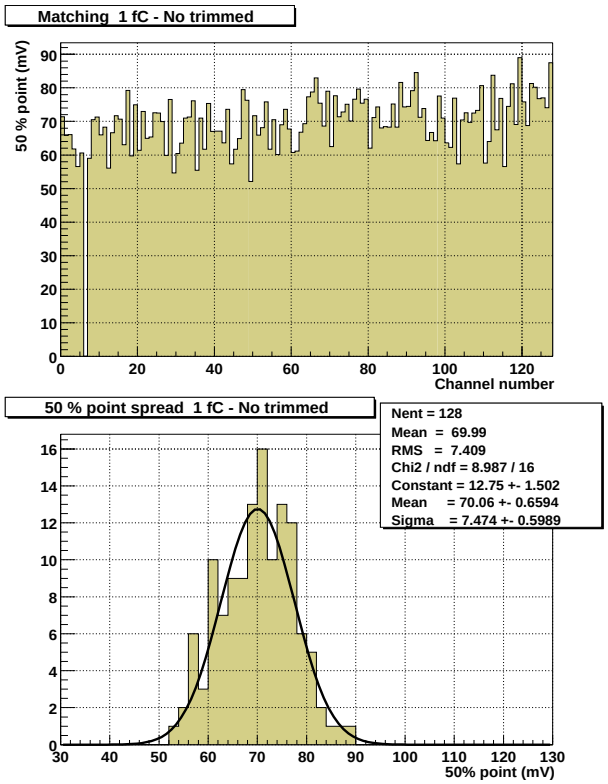

Figure 4: Distribution of threshold for 128 channels in one ABCD3T chip before threshold correction.

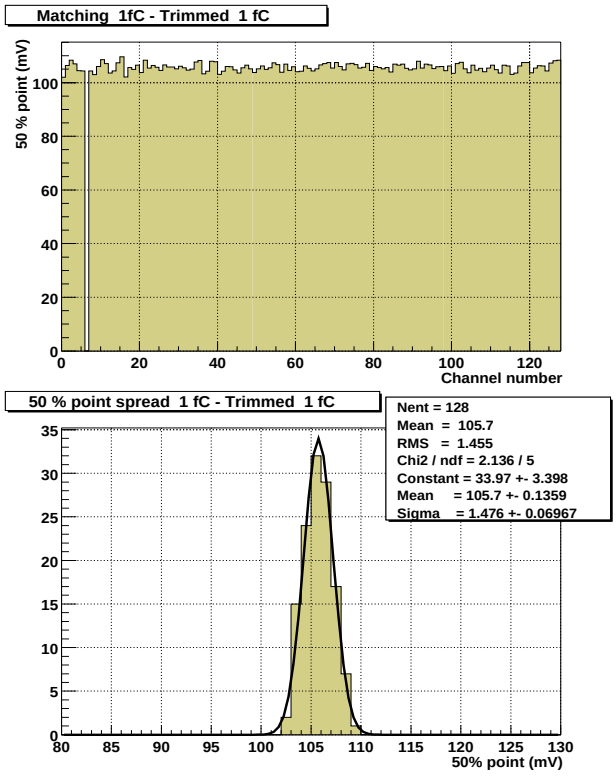

Figure 5: Distribution of threshold for 128 channels in one ABCD3T chip after threshold correction.

III. RADIATION EFFECTS

The radiation effects in the DMILL technology and in the ABCD design have been discussed in the previous paper [4]. The DMILL technology is qualified as a radiation resistant one, however, the radiation levels expected for the SCT detector in the ATLAS experiments exceed the upper limits of those specified for the DMILL process, i.e. 10 Mrad of the ionising dose and 1×10^{14} n/cm^2 1 MeV eq. neutron fluence. In addition, if one takes into account very advanced requirements regarding the noise, speed and power consumption of the ABCD chip, it becomes obvious that radiation effects in the basic devices, although limited, can not be ignored.

A. Total dose effects

The radiation hardness of the ABCD design has been evaluated in numerous tests in various radiation environments. The performance of the front-end circuit is affected by the major radiation effect in bipolar transistors, i.e. degradation of the current gain factor β. As a results the parallel noise in the front-end increases. This effect has been taken into account from the beginning of the ABCD project.

Fig. 6a. shows evolution of the parallel noise vs. particle fluence during irradiation of a hybrid with 6 ABCD3T chips in 24 GeV proton beam. Each curve represents the average for 128 channels in one chip. The results of neutron irradiation performed in a reactor are shown in Fig. 6b. In both cases we observe an increase of the parallel noise which is due to the increase of the shot noise of the base current when the input stage is operated with a constant collector current. As discussed in previous paper [1], the increase of the parallel noise has a small effect on the total noise when the chips are connected to long strips and the noise is dominated by the series noise.

Another effect, which was not expected from the beginning but has been observed systematically in all radiation tests, is an increase of the offset spread in the discriminator. The source of this effect has been identified as worsening of resistor matching. The evolution of the offset spread vs. proton fluence (a), and neutron fluence (b), for 6 irradiated ABCD3T chips is shown in Fig. 7. The offset spread increases by a factor 3-4 after proton irradiation and by a factor about 2 after neutron irradiation. The same effect was observed before for the ABCD2T chips.

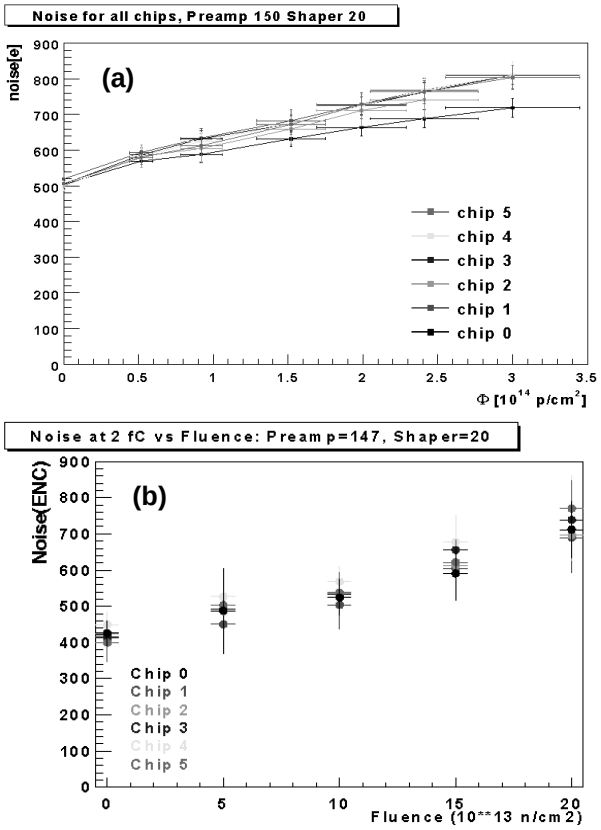

Figure 6: Increase of the parallel noise vs. particle fluence: (a) protons, (b) neutrons.

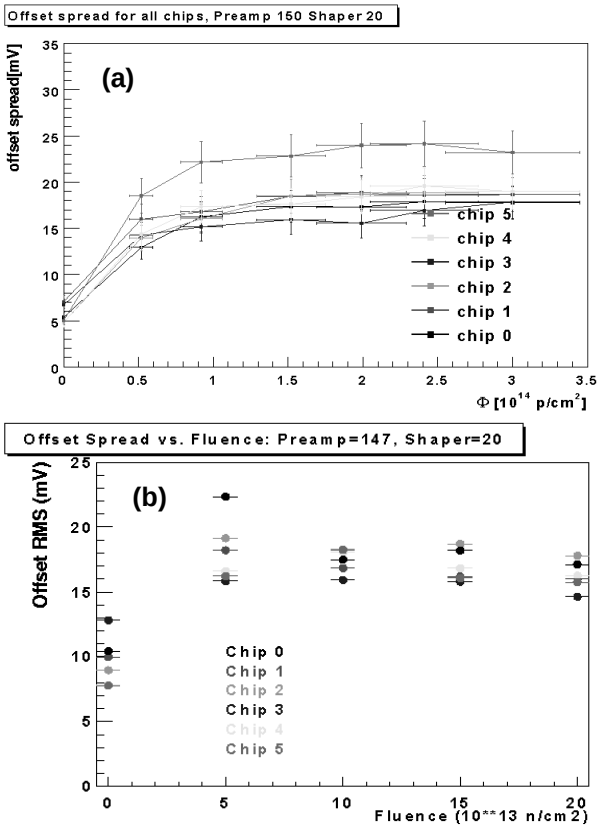

Figure 7: Increase of the discriminator offset spread vs. particle fluence: (a) protons, (b) neutrons.

A major total dose effect expected in the digital part of the ABCD design is slowing down. The post-radiation drifts of the parameters of MOS devices as well as the variation of the process parameters have been anticipated and a sufficient speed margin has been foreseen in the design. Typical degradation of the maximum clock frequency vs. total ionising dose for ABCD3T chip is shown in Fig. 8. Since the test was done with a high dose rate the standard high temperature annealing was performed in order to simulate irradiation with a low dose rate. After full dose of 10 Mrad the maximum clock frequency is 52 MHz at nominal supply voltage of 4 V, compared to the required 40 MHz. Compared to the ABCD2T design the speed margin has been improved by about 10 MHz by tuning the timing in various blocks of the circuit.

In the ABCD2T chips excessive leakage current was observed after irradiation. The source of the leakage has been traced down to a particular latch structure which was used in various block of the chip. The design has been corrected in the ABCD3T version. The evolution of the digital supply current after irradiation up to the nominal dose of 10 Mrad and annealing is shown in Fig. 9. A rapid increase of the supply current is observed immediately after irradiation with high dose rate. The excessive current anneals then very quickly down to the ultimate level, which is even below the initial value.

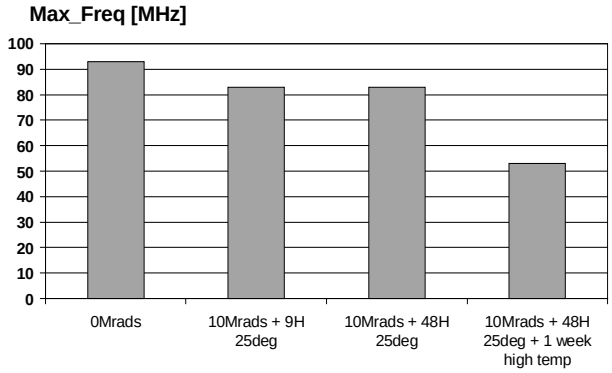

Figure 8: Evolution of the maximum cock frequency after irradiation and annealing.

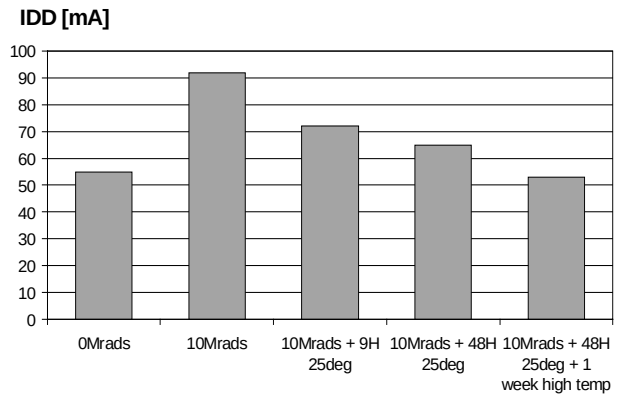

Figure 9: Evolution of the digital current supply after irradiation and annealing.

B. *Single event effects*

Since the ABCD chips will be exposed in the experiment mainly to high energy charged particles and neutrons single event effects (SEE) are equally important as the total dose effects. Given the architecture of the ABCD chip there are two major types of digital blocks which may be affected by SEE, namely the pipeline and the static registers which contain information about chip configuration and settings of operating points. Any bit flip in the pipeline causes a single data error and thus to be compared with the noise rate expected from the front-end circuit. Such errors will not require any intervention. The errors in static registers may lead to changes of static biases in the front-end, setting of the threshold or changes of operation mode. In order to recover from such errors it will be needed to reload the chip configuration.

The sensitivity of the ABCD chip to the SEE has been tested in 24 GeV proton beam and in 200 MeV pion beam. The results from both tests are fully consistent as one can expect assuming that for the DMILL process the energy transfer threshold for SEE is well below 200 MeV. An example of data is shown in Fig. 10. The plot shows the number of SEE counted in the pipeline of one chip while the beam was scanned across the hybrid with 6 ABCD2T chips. The upper plot shows the SEE counts performed within the beam spills and the lower plot shows the SEE counts outside the beam spills.

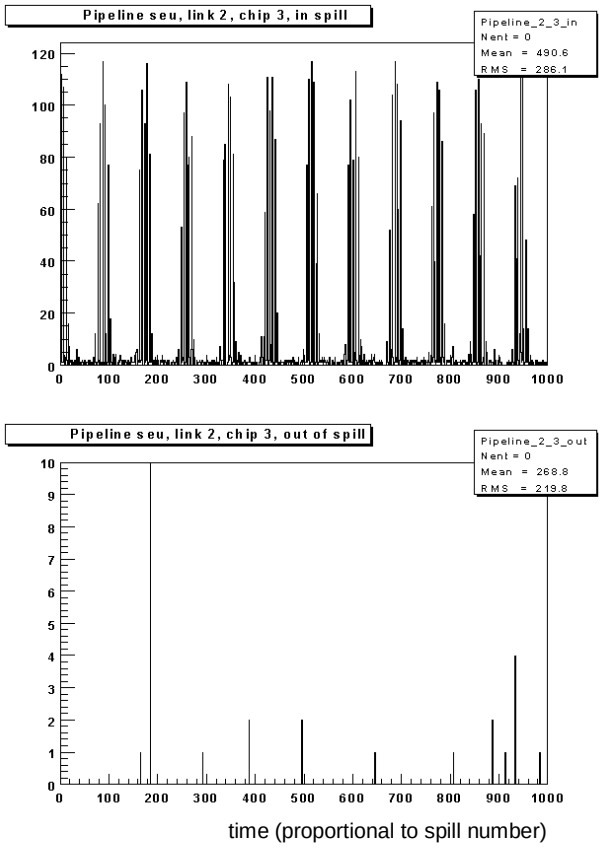

Figure 10: Measurement of SEE in the pipeline during irradiation proton beam.

From such measurements we have estimated the cross sections for two types of memory cells used in the ABCD design. For the pipeline in which dynamic memory cells are used the SEE rate has been measured as 5×10^{-7}/bit/s. For the static registers the SEE rate has been estimated as 1×10^{-7}/bit/s. None of these numbers seems to create a problem for operation of the SCT in the particle fluxes as presently estimated.

IV. SUMMARY

The ABCD3T chip is the final version of the binary readout for the ATLAS Semiconductor Tracker. It incorporates fixes of minor imperfections identified in the previous prototypes. The ABCD2T and ABCD3T chips have been used extensively for building complete SCT modules used then in the beam tests and the multi-module system test. About 100 ABCD2T and ABCD3T chips have been irradiated in various tests up to the total doses as expected in the ATLAS SCT. All these tests showed consistent results. An efficient wafer screening system has been developed and used for testing wafers from prototype batches.

V. REFERENCES

1. W. Dabrowski et al., Design and Performance of the ABCD Chip for the Binary Readout of Silicon Strip Detectors in the ATLAS Semiconductor Tracker. Proc. of the IEEE Nucl. Science Symposium, Seattle, IEEE Trans. on Nucl. Sci., in print.
2. T. Dubbs et al., The Development of the CAFE-P/CAFE-M Bipolar Chips for the Atlas Semiconductor Tracker. Proc. of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA September 20-24, 1999, CERN/LHCC/99-03, 29 Oct 1999, p. 123.
3. D. Campbell et al., The Development of the Rad-Hard CMOS Chip for the Binary Readout of the ATLAS Semiconductor Tracker. Proc. of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA September 20-24, 1999, CERN/LHCC/99-03, 29 Oct 1999, p. 152.
4. W. Dabrowski et al. Radiation Hardness of the ABCD Chip for the Binary Readout of Silicon Strip Detectors in the ATAS Semiconductor Tracker. Proc. of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA September 20-24, 1999, CERN/LHCC/99-03, 29 Oct 1999, p. 113.