The ALICE Silicon Pixel Detector Readout System

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Abstract

The ALICE SILICON PIXEL DETECTOR (SPD) [1] is located within the Inner Tracking System (ITS) and is the detector with the highest active channel density and closest to the point of interaction.

Approximately 10 million active electronic channels, contained in a volume of approximately 3 litres, have to be read out and controlled.

Such a high density in an inaccessible position has imposed a high degree of multiplexing to reduce the amount of cabling to a minimum.

This paper will describe the proposed architecture of the readout and control paths.

I. INTRODUCTION

The basic building block of the ALICE SPD is the *half stave* consisting of two *ladders* of Pixel detector matrix flip-chips each bonded to five front end readout chips (*Pixel Chips*).

Two *half staves* are aligned in the beam direction, glued and wire bonded onto two buses to form a 33 cm long *stave*. Pilot chips are located at the extremities of this *stave* to perform the readout and control functions and transmit the digital data to a remote *Router* which will assemble the data for transmission to the DAQ.

Six *staves*, two from the inner layer and four from the outer, are mounted on a carbon fibre support and cooling sector. Ten such *sectors* are then mounted together around the beam pipe to close the full barrel. In total there will be 60 *staves*, 240 *ladders*, 1200 *Pixel Chips*, 9.83 * 10^6 cells or active channels of read out.

Each front end readout chip contains a mixture of analogue and digital circuitry for the readout of 8192 detector cells. These cells are arranged in a matrix of 256 rows by 32 columns. Each cell comprises of a preamplifier, shaper, discriminator, 2 trigger latency delay units, a four event de-randomising buffer and an output shift register.

Acquisition and readout are independent activities which are performed in parallel. Both are controlled by the *Pilot chip*. The front end chips run as slave devices. The *Pilot chip*, on receipt of a Level 1 (L1) trigger signal will cause the detector hit pattern to be stored in the first free location of the de-randomising buffer of the front end chip. The Level 2 decision will determine whether the front end chip is read out or not. A Level 2 Yes (L2Y) will cause each *Pilot Chip* to initiate a read out cycle, sequentially addressing each of its own ten front end chips. The data from the addressed de-randomising buffer are shifted out of the front end chip into the Pilot chip and serialised for transmission over an optical fibre link to the *Router module* which will be located outside of the ALICE detector. A Level 2 No (L2N) will cause the data from the de-randomising buffer to be ignored. In each case the de-randomising buffer location is freed for future use.

Trigger	Type	Latency	Rate(Pb-Pb)
Level 1	L1	5.5μs	1100Hz
Level 2	L2Y	100μs	40 – 800Hz
	L2N	<100μs	
The average occupancy is expected to be 1-2%.			

Table 1 shows the expected Trigger Latency and Rates

Each *Router* will receive the Pixel data from six optical fibre links. The input stage of a *Router* will perform, on the fly, zero suppression of the redundant data before formatting for insertion into the DAQ via the ALICE Digital Data Link (DDL) [2, 3]. The controls for the pilot chips and front end chips will be issued by the *Router* on reception of the trigger system decisions. The *Router* also monitors the readout chip de-randomising buffer usage and issues the appropriate busy to the DAQ control. Additional memory is contained to provide multi-event buffering. An additional data path has been supplied to enable spying on the event data.

The control, parameter loading and testing of the front end chip is realised by JTAG. A JTAG controller is incorporated in the Router module.

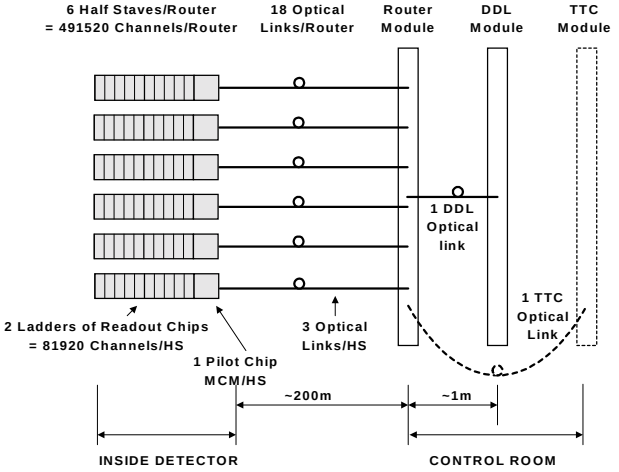

Figure 1 shows the degree of multiplexing achieved per Digital Data Link.

II. The Pixel Readout Chip

A. Readout

The acquisition part of the *Pixel Chip* may be regarded as a matrix of 32 columns by 256 rows of Pixel Cells. These Cells are connected as 32 parallel shift registers of 256 bits each and are read out sequentially at a frequency of 10MHz. Each Pixel Cell includes a four event de-randomising buffer connected as a FIFO. The control of the readout of the acquisition is performed via dedicated signal lines.

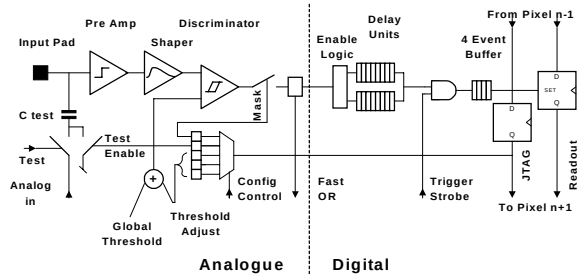

Figure 2 shows the Block Diagram of a Pixel Cell.

B. Parameter and Configuration Registers

The Parameter loading and Configuration of the *Pixel Chip* are performed via JTAG [4] which can operate at a frequency of 5MHz.

Most of the Parameter registers are contained within the periphery of the device and consist of 8 bit digital to analogue converters to provide a global threshold voltage, voltage and current references for the front ends and current starved logic. There are two other registers, one to control the strobe delay time the other to switch on the front end leakage current compensation and control the delay of the strobe inside the device. There are five bits of individual Pixel Configuration, three for the threshold fine control and two bits for *Test Enable* and *Pixel Mask*. These five bits are contained within the Pixel Cell and are individually loaded from a single bit of a column shift register chain. These JTAG column shift register chains are internally organised as 32 data registers of 256 bits, one for each column, each bit being loaded into the location selected by the values in the *enable* data register. The values previously loaded into these registers may be read back by means of the JTAG capture-dr function.

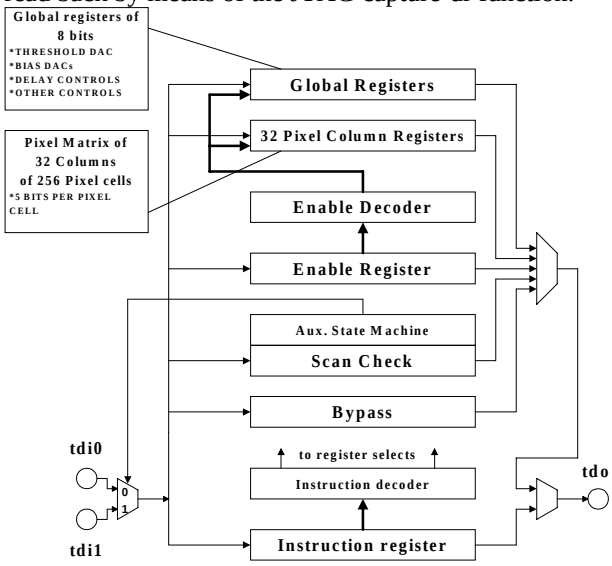

Figure 3 shows the architecture of the Pixel Chip JTAG circuitry.

As a means of security to allow some redundancy in the JTAG chain a second tdi has been implemented on each *Pixel Chip* to allow bypassing a device which has been detected as having a faulty JTAG chain. See Figure 4. The selection of which tdi to use is made by a Scan Check circuit. An auxiliary state machine is triggered each time the JTAG TAP Controller state machine enters the Test-Logic-Reset state. An infra structure type of test is executed when the capture-value of the preceding *Pixel Chip* instruction register is compared to an expected value. Should, for example, an error caused by *Pixel Chip* n be detected by *Pixel Chip* n+1, *Pixel Chip* n+1 will select the JTAG input tdi1 as its input for JTAG data, bypassing *Pixel Chip* n. *Pixel Chips* with errors may be detected by reading the state of the Scan Check registers. This scheme will allow the reconfiguration of the JTAG chain to compensate for faulty non-consecutive *Pixel Chips*

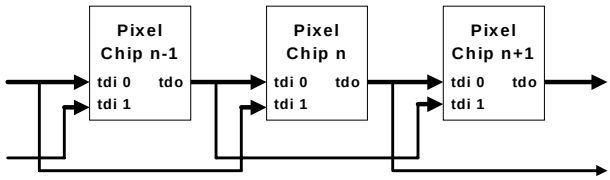

Figure 4 shows the tdi/tdo Interconnections between the *Pixel Chips.*

III. MOUNTING THE PIXEL READOUT CHIPS

The two *ladders* of *Pixel Chips* (2*5 *Pixel Chips*) are glued and wire bonded onto a Low Mass Kapton/Aluminium data bus to form the *Half Stave*. The bus is made up of six layers, three signal and three power and ground, and has a total thickness of 200µm. One edge of this bus is in the form of a staircase to allow bonding to the various layers, see Figure 5. Signal Integrity Simulations have shown that by employing output stages with controlled rise and fall times the cross talk between bus lines would be acceptable.

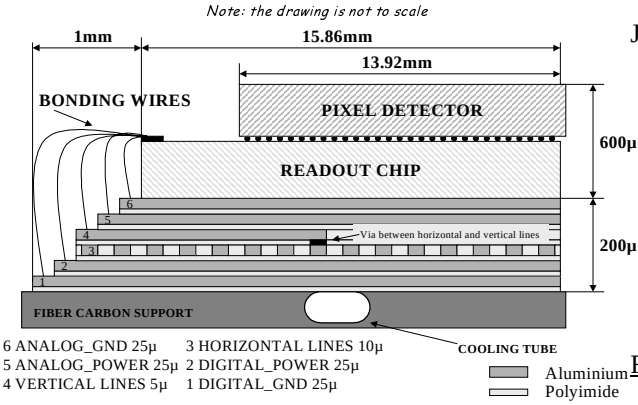

Figure 5 shows a cross section of the Data Bus assembly.

At the extremity of the *half stave* there is a *Pilot Chip Multi Chip Module* which controls the readout of the *Pixel Chip* and performs the necessary logic and interfacing to the optical links which carry the data to the outside of the detector and receive the trigger control signals and JTAG control signals.

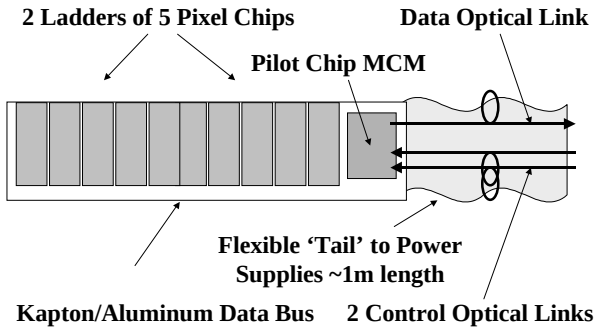

Figure 6 shows the assembly of the various components onto a *half stave*.

IV. THE PILOT CHIP MULTI CHIP MODULE

The *Pilot Chip Multi Chip Module* (PCMCM) [5] is mounted at the extremity of the data bus and serves as the interface between the *Pixel Chips* on one side and the *Pixel Router* located in the control room on the other side.

The PCMCM includes:

- GTL/CMOS adapters to interface the *Pixel Chip*s to the internal logic of the MCM,
- the Pilot state machine which controls the readout of the *Pixel Chip*s ,
- G Link interface and serializer for the optical link [6],
- Laser receiver and transmitter diodes.

Three optical links connect the PCMCM to the *Pixel Router* which is situated in the control room. Two are lower speed links and are used to supply the control and trigger information and the third, a faster link, is used to carry the Pixel readout data back to the *Pixel Router*.

Control data consists of either trigger information or JTAG parameter information.

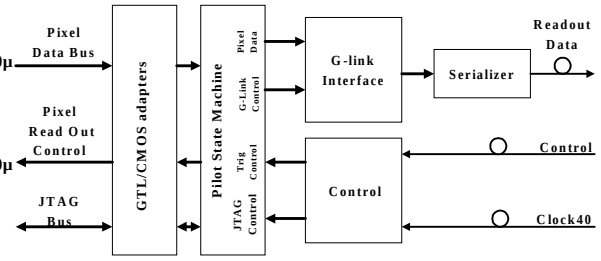

Figure 7 shows an overview of the *Pixel Pilot MCM*.

On receipt of a Level 1 trigger from the *Pixel Router module* the *Pixel Readout Control state machine* will strobe the *Pixel Chips* causing the hit patterns to be stored into the next vacant position of the multi-event buffer. On receipt of a L2Y trigger the *Pixel Chip Readout Control state machine* will perform a sequential readout of the pending event data in the multi-event buffer. The 10 *Pixel Chips* of each *half stave* are read out at a frequency of 10MHz in 256µS. Should a L2N or data reject be received the address pointers of the multi-event buffers are incremented to discard the pending event data. A busy logic has been implemented inside the *Pilot Chip Readout Control state machine* to prevent data corruption.

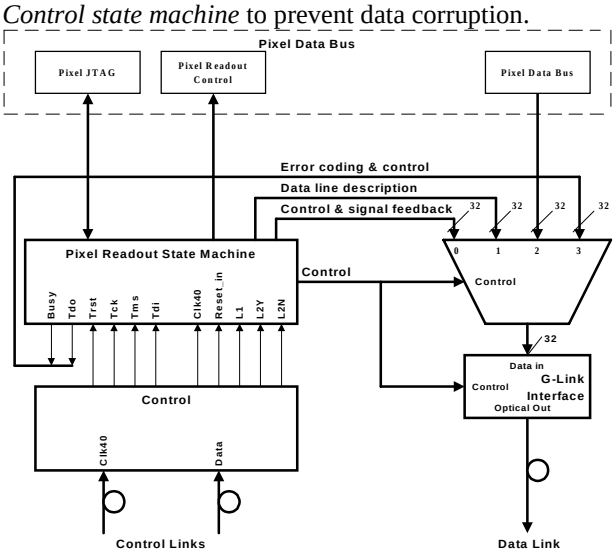

Figure 8 shows a functional block diagram of the Pilot Chip MCM

The readout data optical link has a bandwidth of 1.28 Gb/s. The data input is sourced from four 32 bit registers which are multiplexed into four time slots at a frequency of 40MHz which will allow four words to be transmitted within the 10MHz clock period of the *Pixel Chip*. As a consequence one out of the four time slots will be used to transmit the 32 bit Pixel Data line and the other three time slots can be used to transmit control data and error coding, especially when the system is being commissioned.

V. The Router Module

The *Router* module is a 9U VME module and provides the interface between the on detector electronics and the DAQ.

A. Router Architecture

Each *Router module* will have six channels in order to connect all the links required for the operation of one half of a *sector*, ie all the optical links from one side of the *sector.*

Each channel will have three optical fibre links, one to receive data being returned from the Pixel Detector and *Pilot Chip MCM* and a pair for the transmission of trigger control signals and JTAG parameter and configuration data to the *Pilot Chip MCM*.

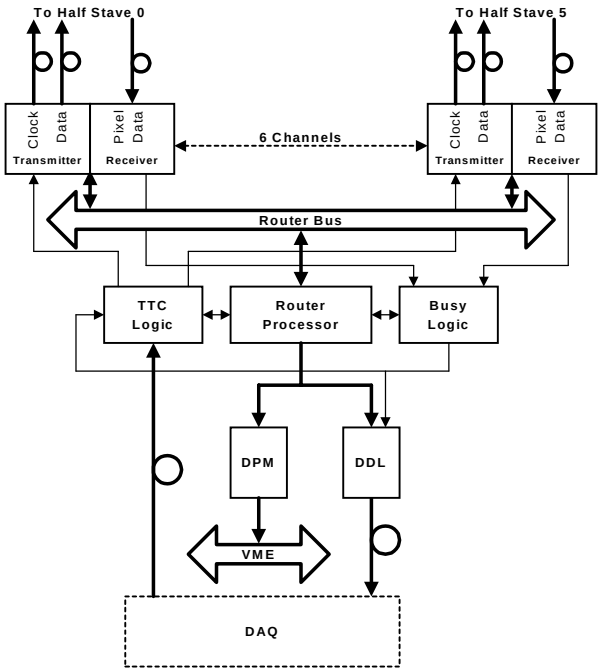

Figure 9 shows the Block Diagram of the Router Module.

The main data flow will be that which arrives from the Pixel detector for reformatting by the Router processor. Other debugging information is made available during the other transmission time slots. The output of the processor will be coupled to the DDL as well as a dual port memory which may retain a copy of the data transmitted to the DDL which will be accessible via the VME port of the Router to allow online monitoring of the experimental data.

B. Functioning

On receipt of triggers from the Timing, Trigger and Control System [7] (TTC) the *Router* will issue commands to the *Pilot Chip* to either save the data in a free buffer location, readout the next stored event data from the multi-event buffer or to reject the stored data awaiting readout. The *Router* monitors the multi-event buffer busy signal generated by the *Pilot Chip Readout State Machine* so that should all the locations be occupied a busy will be issued to the trigger system for further processing. The *Router* also maintains an image of this busy within its own logic to overcome cabling delay problems.

All manipulations on the Pixel data will be performed by this module to ensure that the amount of vulnerable electronics placed in the harsh environment of the detector is kept to a minimum. Provision will be made to ensure that the programme which will be executed may be modified easily.

C. Pixel Data Link Receiver

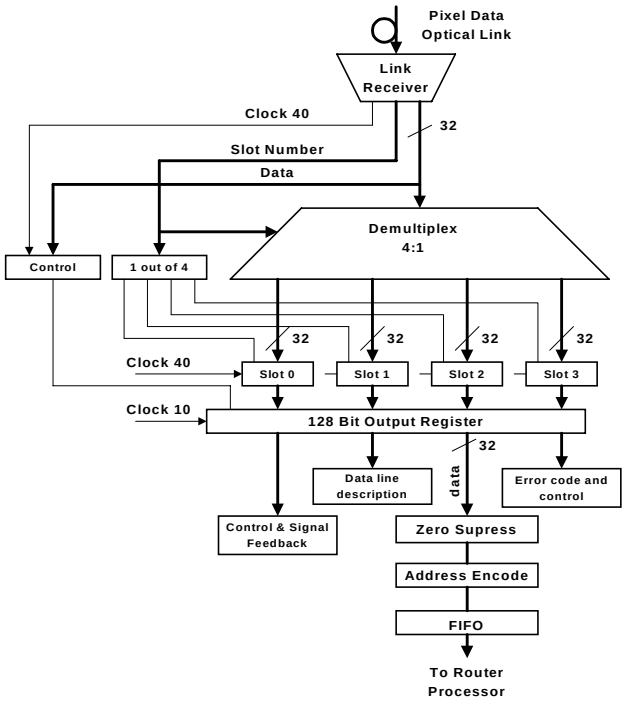

Figure 10 shows the Pixel Router receiver block diagram.

The serial data received from the *Pilot Chip MCM* will be de-serialized by G-Link receiver into the four time slots and reformatted as a 128 bit data word synchronised to the 10 MHz readout clock. Having this large data word will assist with the installation and verification of the integrity of the communications. The data received will be an image of the data read out of the *Pixel Chip*. After Zero Suppression of the redundant data it is stored in a FIFO for subsequent hit encoding. Reformatting of this

data will be performed by the Router processor to make each event uniquely identifiable when inserted into the data stream.

D. Control Transmitter section

The trigger control signals received from the Trigger Timing and Control (TTC) or JTAG control and configuration data would be categorised into commands then serialised for transmission at 40MHz to the *Pilot Chip MCM*. As example, commands could be: L1 Trigger, L2Y, L2N, JTAG information is following, etc.. Such a system would allow commands to be transmitted every 100ns and JTAG data may be transmitted at an effective clock frequency of 5 MHz.

E. *Router Functioning*

The data, after Zero Suppression and address encoding, is stored in FIFOs that are large enough to contain two typical events. The Router Processor will sequentially read one event from each of the channels and perform the data formatting and data tagging as required for the DAQ. These data are then passed to the DAQ via the DDL. A dual ported memory has been included so that a copy of the data written to the DAQ may also be accessed from the VME port of the Router module.

F. Router Data Output Channel

A Digital Data Link Source Interface Unit (DDL-SIU) will be implemented inside the *Pixel Router* to establish the connection to the DDL.

VI. ALICE DIGITAL DATA LINK

The ALICE DDL has been selected as the medium for transferring the experimental data to the DAQ. This ALICE standard link provides a generic connection that will always be compatible independently of the state of the art of the actual technology of the DAQ.

VII. STATUS OF THE PROJECT

The *Pixel Readout Chip* is currently being manufactured. A test system has been developed to evaluate the performance and characterise the device under laboratory, radiation and test beam conditions. A prototype model of the data bus is also under construction. In all of the tests that have taken place so far the *Pilot Chip MCM* has been emulated with success by a custom design VME module. The *Pilot Chip MCM* itself is progressing through the design and simulation stage and a submission for manufacturing a prototype device is expected to take place at the beginning of next year. The final design of the *Router Module* is still under discussion and a prototype should ready during the next year.

VIII. CONCLUSIONS

To build such a detector is a challenge. Two problems that immediately spring to mind are those of radiation and of confinement.

The level of radiation is not as severe as in some other experiments but never the less it can not be ignored. This problem has been overcome by the use of deep submicron CMOS technology and gate all around transistors [8] for the manufacturing of the components that are mounted within the detector.

The problem of confinement is still a problem today. To fit so many active electronic channels into such a volume still poses problems. The interconnection technologies which are being used are in their infancy and what needs to be achieved is at the limit of what can be done today. Two examples of where there are difficulties are the Bump Bonding of the Pixel Detector to the Readout Chip where there are 8192 bumps on a matrix of 50μm by 425μm. The carrier bus is the other one. It consists of a multi-layer structure of very fine pitch data lines and long and thin power planes passing high currents and requiring low voltage drops.

IX. REFERENCES

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