Readout of the CMS Pixel Detector.

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Abstract

The design of the readout of the CMS pixel detector is presented. The basic detector layout is shown together with the data rates expected at full LHC luminosity. The pixel readout chip is described and the scheme for the transfer of the trigger confirmed data is outlined. The integration of the pixel readout system into the CMS DAQ system is shown.

I. Detector Layout

The task of the CMS pixel detector is to provide high resolution 3D space points required for the track pattern recognition and for b-tagging.

Two barrel layers of the pixel detector will be located at mean radii 4.3 cm and 7.2 cm with a third layer at 11.0 cm added later. The pixel barrel will be 53 cm long and will be supplemented by two end disks on each side (see Figure 1). In order to achieve the optimal vertex position resolution in both the (rΦ) and the z co-ordinates a design with a square pixel shape 150×150 μm^2 was adopted.

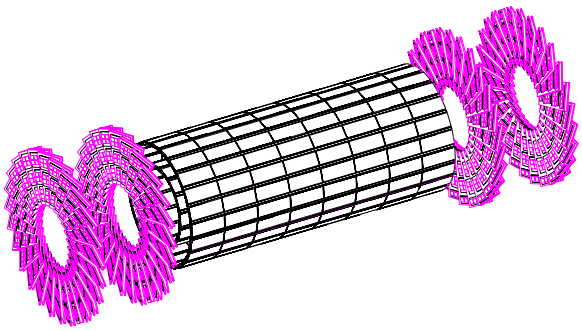

Figure 1: Perspective view of the CMS pixel system.

To enhance the spatial resolution by analogue signal interpolation the effect of charge sharing induced by the large Lorentz drift in the 4 T magnetic field is used. Hence the detectors are deliberately not tilted in the barrel layers but are tilted in the end disks resulting in a turbine like geometry. The use of signal interpolation means that full analogue information has to be transferred from each hit pixel.

The whole pixel system consists of about 1500 detector modules arranged into half-ladders of 4 identical modules each in the barrel and blades with 7 different modules each in the disks.

To read out the detector about 16000 readout chips are bump-bonded to the detector modules. The total number of readout channels (pixels) is about 45*10^6. More detailed discussion of the detector layout and geometry can be found in Ref. [1].

A picture of the CMS barrel pixel module is shown in Figure 2. A 65.9 mm long, 17.45 mm wide and 250 μm thick Si sensor has 16 readout chips (ROCs) bump-bonded to it. Each ROC reads 53 (rows) * 52 (columns) pixels and includes a column periphery and an interface area.

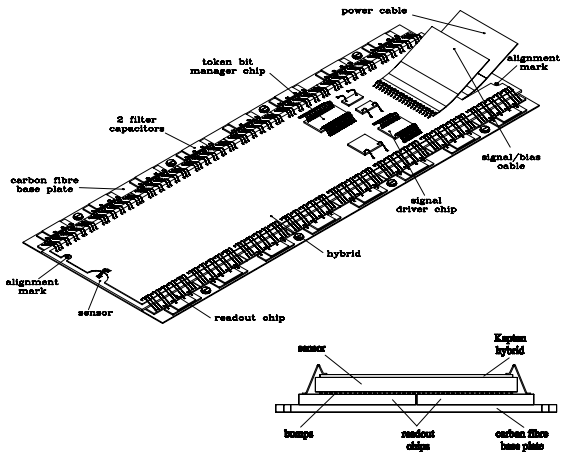

Figure 2: View of a barrel module. In the insert the vertical scale is raised by a factor of 5.

The ROCs are glued to a 270 um thick Si base plate which can be attached to the cooling frame. A 50 μm Kapton hybrid is glued on the top of the sensor. The readout chips are wire bonded to the hybrid circuit. On the hybrid, clock and control signals arriving via a copper-on-Kapton cable are distributed to the readout chips, involving the Token-bit manager chip (TBM), and the hit signals from triggered events are sent by a driver chip through the same Kapton cable to the barrel periphery mounted at the ends of the barrel. Power is brought from the barrel periphery to the hybrid via aluminium wires.

The Kapton cable is glued and wire bonded to the hybrid. The bump-bonding procedure using Indium has been developed at PSI. The end-cap detector modules are somewhat different. Due to the blade design the sensor area varies in size from 2 ROCs to 10 ROCs.

II. Detector Readout

A. Data rates

At full LHC luminosity about 1000 tracks cross the pixel barrel layers every 25 ns. Out of these less than 50 tracks are interesting from the physics point of view (p_T > 1 GeV). The rest have either low momenta or belong to pile-up events.

For the barrel layer at 7 cm about 3300 pixels are hit every 25 ns. On the average 15 pixels are hit in one barrel module which translates into an occupancy of 3.3 * 10^{-4} or a single pixel counting rate of 10 kHz. Since the readout is double-column oriented it is of interest to note that a double-column is hit at a 0.6 MHz rate (occupancy of 1.5%) and on the average a hit column will register 2 hit pixels.

The overall number of hit pixels per event is 1.3 * 10^4, which, assuming 3 Bytes of information per pixel, translates into a data volume of about 40 kBytes/event. At the nominal 100 kHz trigger rate this results in a 4 GBytes/s data flow.

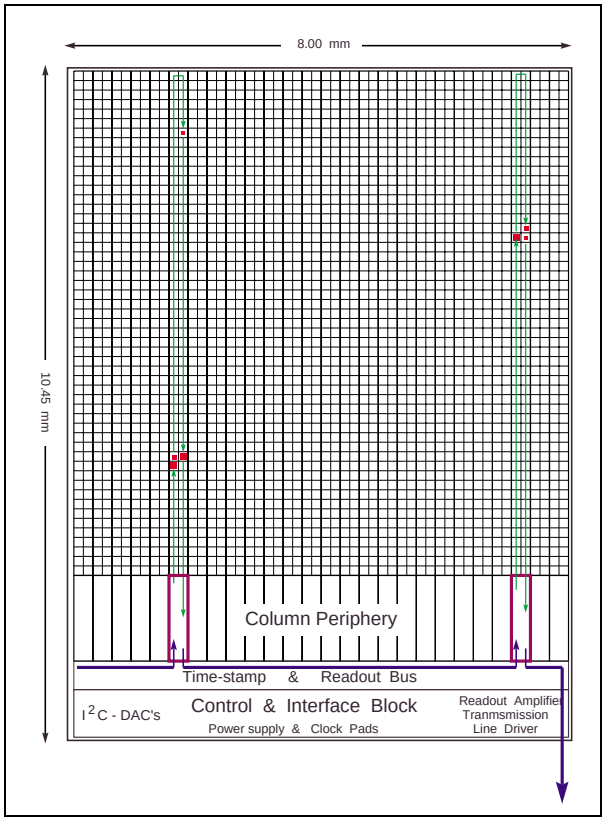

Figure 3: Conceptual layout of the pixel readout chip.

B. Readout Scheme

Readout chips are organised in double-columns. Each double-column consists of a group of 106 pixels and a periphery circuit. Figure 3 shows the overall layout of the readout chip, while Figure 4 presents the column periphery circuit in more detail.

Each pixel cell consists of analogue and digital parts. The analogue part has an amplifier, shaper and a comparator. The thresholds of the comparator are individual programmed for each pixel using a 3-bit DAC. Only signals that are above the threshold are allowed to trigger the digital part of the circuit.

Pixel cells within one double column are connected to its periphery with a set of local bus lines, one of them being the Column-OR which combines all pixel cells in a double column into a global OR. Hit pixels use this Column-OR to notify the periphery about a new event. The data are then read out in two stages.

The first stage, called the column drain cycle, takes place within each double-column and runs at 40 MHz. The time information is stored (within 25 ns) in the time-stamp buffer and the address and the analogue signal of each hit pixel is transferred as fast as possible to the column data buffer located in the column periphery. For the average of 2 pixels hit per double column, about 6 clock cycles (at 40 MHz) are required to complete the readout.

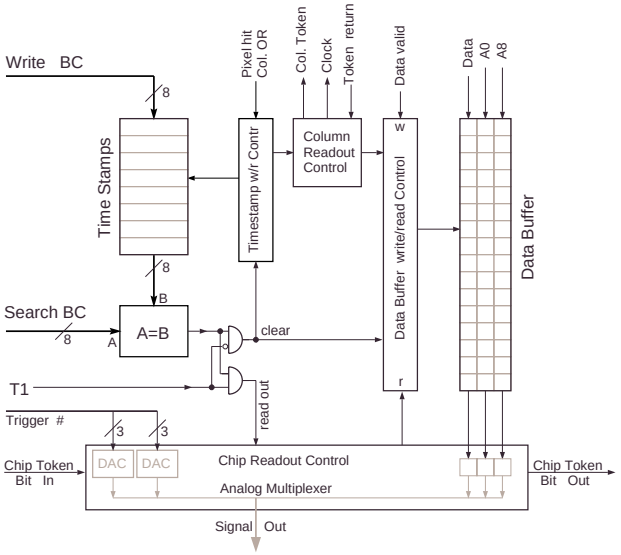

Figure 4: Schematics of the column periphery mechanism with multiple time-stamp and data buffer management.

This data has to be stored for 3.2 μs while waiting for the 1st level trigger (1LT) decision. For every clock the bunch crossing counter (BC in Figure 4) stored in the time stamp buffer is compared with the search counter (Search BC). If both agree the time stamp is considered for trigger confirmation (T1 signal in Figure 4).

The data confirmed by the 1LT are saved for the second stage of the readout while the unconfirmed data are erased. The 1LT rate is about 30 kHz, which results in a data reduction factor of 1000.

In the second readout stage the triggered data are transmitted to the CMS data acquisition. The data confirmed by the 1LT are flushed from each double-column and are sent on optical links to the readout electronics (Front End Driver modules - FEDs) 100 m away from the detector. A schematic view of the token bit readout mechanism is shown in Figure 5 while Figure 6 shows the overall integration of the pixel readout in the CMS DAQ system.

Groups of 8 or 16 ROCs are connected to one readout link. In order to synchronise the data transmission a token-bit manager chip (TBM) is used (see Figure 5). This chip, through a token mechanism, controls the access of each column to the readout link. It also formats data packets and signals errors. The preliminary design of the TBM chip (made by the CMS group from Rutgers University) will be ready at the end of 2000 and will initially be implemented in a programmable gate array.

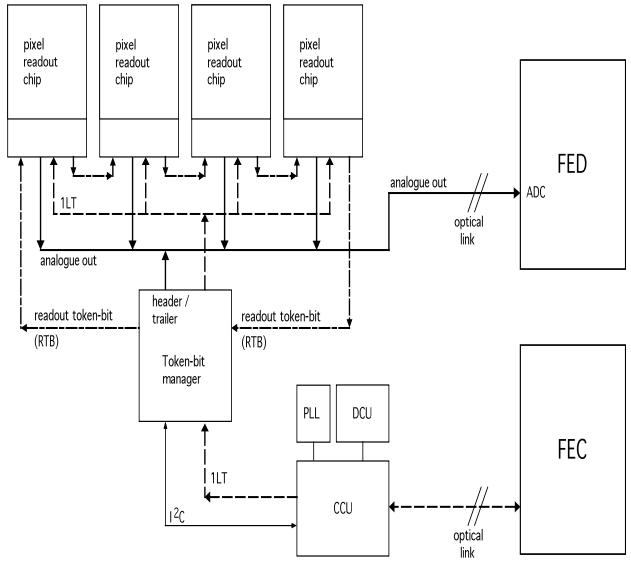

Figure 5: A schematic diagram of the pixel readout system. The FED and FEC modules are located in the counting room. The Token-bit manger chip is placed on the module's hybrid for the barrel and on the port cards for the end disks.

A data packet is sent through each link for every triggered event, even if no pixels were hit. A packet includes a header and trailer provided by the TBM chip. In addition to the analogue pixel-charge amplitude several digital signals have to be transmitted as well e.g. pixel addresses, column addresses, ROC's IDs and trigger numbers. In order to save bandwidth digital signals are compressed using a 5-6 level analogue coding. The exact number of the coding levels will be determined later when the noise and stability of the optical links are known.

Both chips, the ROC and the TBM will include I2C interfaces in order to be able to program various internal registers like e.g. pixel thresholds, DAC values or the trigger latency. The I2C protocol will also be used to read back status information from the front-end system.

C. Integration with the CMS Data Acquisition

The FED modules, located in the counting room, receive data packets, perform digitisation, format events and send them to the CMS DAQ (indicated by the Readout Unit - RU in Figure 6).

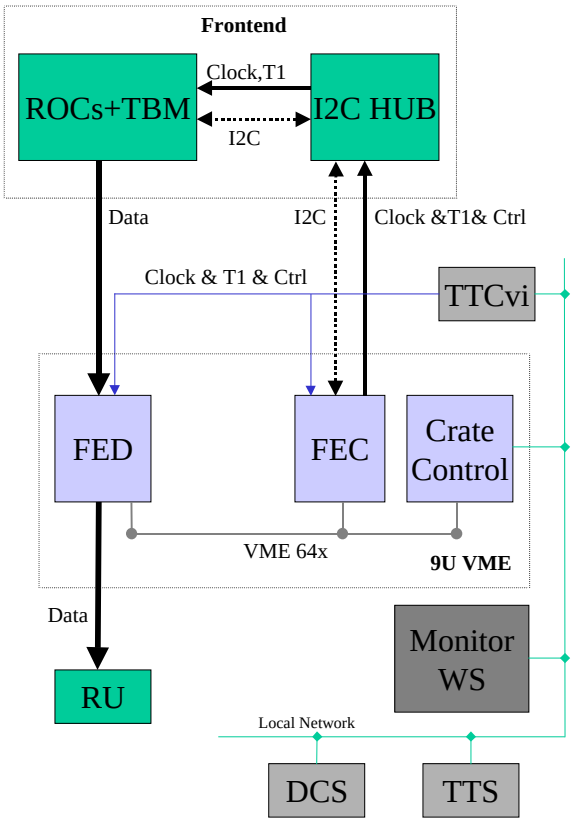

Figure 6: The integration of the pixel readout in the CMS data acquisition system.

Each FED has 48 input optical links. The circuit in each input includes an amplifier and an ADC. A lookup table is also needed to decode the packed digital signals. After the signal processing events are assembled by combining pixel information from all 48 inputs. By mixing in one FED links from different pixel layers, we can achieve the 2 kByte average event fragment size per FED, required by the CMS DAQ. The FED can buffer up to 100 events. The prototype

pixel FED is being designed by the CMS group from Vienna and will be available in late 2000.

The control modules (FECs), also located in the counting room, send the clock, trigger and all other control and reset signals down to the detector. The ROC chip programming (e.g. setting of the pixel thresholds) is also done by the FECs. FECs communicate with the front end using the I2C protocol. A faster version of the protocol is developed in order to be able to download the pixel thresholds within a reasonable time. In order to limit the number of optical links a I2C-Hub chip is being designed. This chip, placed at the detector, will be used to distribute the incoming stream from one control link to a number of detector modules. The I2C-Hub will be a standalone chip or could be included in the TBM chip. Note that the generic label "CCU" used in Figure 5 has been replaced in Figure 6 by a more appropriate "I2C HUB" label.

The FED and FEC modules which service the same segment of the detector will be located in the same VME crate. This way both can communicate with the same crate controller CPU allowing for efficient system monitoring and fast resets in case of error conditions. Each crate controller communicates with a monitoring workstation where more global data diagnostics will be done. Also shown in Figure 6 are the standard components of the CMS DAQ system : TTC used to distribute the fast signals, DCS detector control system and TTS the trigger throttle control.

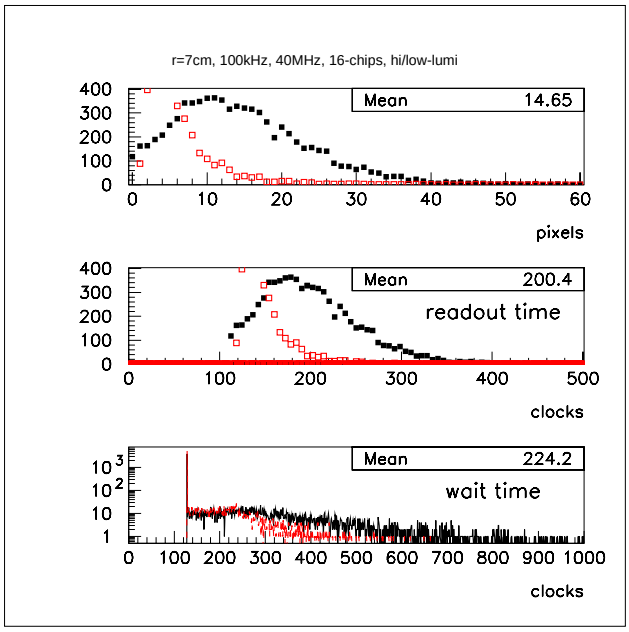

Figure 7: ***Upper figure***: The number of hit pixels per data packet for the pixel layer at 7~cm, the full dots are for the high luminosity and the open dots are for the low luminosity. ***Middle figure:*** The packet readout time shown in units of LHC clocks. ***Lower figure:*** The packet wait time, the peak at 128 clocks corresponds to data packets being transmitted immediately after the arrival of the trigger.

Together about 1500 optical links are needed to readout and control the pixel detector.

D. Readout Time

The number of readout optical links has to be optimised. On one hand this number has to be kept as small as possible in order to minimise the cost and the material budget. On the other hand the bandwidth has to be sufficient to avoid large data losses. With the assumption of maximum 100 kHz trigger rate and a 40 MHz analogue link we arrive at the segmentation presented in Table 1 for the barrel pixels.

Table 1: Readout related parameters at high luminosity for a 100 kHz L1 trigger rate.

Radius [cm]	4	7	11
ROCs/link	8	16	16
Pixels/link	16±11	15±9	8±6
Read. Time [μs]	4	5	4
Max. time [μs]	14	13	10
Wait time [μs]	1.4	2.4	1.1

For example at 7 cm 16 ROCs are connected to a single optical fibre, resulting in an average of 15 pixel hits transmitted per event. The average readout time is then 5 μs. Due to statistical fluctuations in the number of hit pixels (σ=9 at 7 cm), for some events the link will have to readout much more data, which might take up to 13 μs.

The distribution of the readout time lengths, together with the histogram of the number of pixels per link, are shown in Figure 7. While the average number of pixels per link is 15 the tail of the distribution extends up to 50 pixels, resulting in very long data packets. The readout system should be able to deal with such cases and not time-out too early.

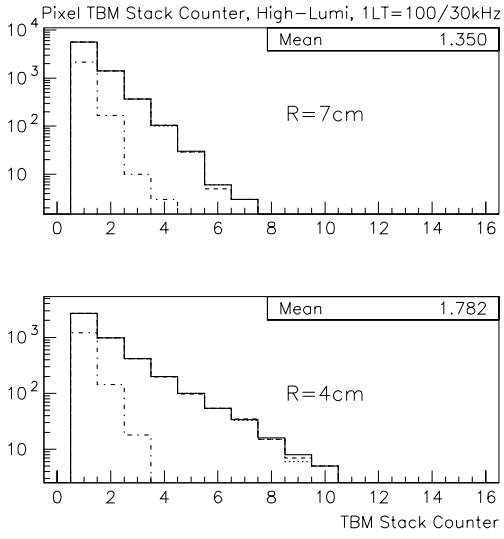

Figure 8: The TBM stack counter occupancy. The solid line is for a 100 kHz 1LT rate and the dashed line is for 30 kHz. The upper figure is for the pixel layer at 7 cm and the lower one is for 4 cm.

Sometimes the readout will still be busy with the previous event and triggers will have to be queued in the TBM chip. The average waiting time after the arrival of the trigger is also shown in Figure 7. Most of the time the data packet is sent immediately after the arrival of the trigger (note the sharp peak at 128 clocks in the lower part of Figure 7), for some events however the waiting time can be as long as 1000 clocks (25 μs).

To queue triggers the TBM chip requires a buffer of a sufficient size. Figure 8 shows the average occupancy of these buffers for pixel layers at 4 and 7 cm at high and low luminosities and for typical trigger rates. From these plots one can conclude that a size between 8-16 is sufficient. The TBM chip is designed to react when the number of queued triggers is above a certain programmable value. It then blocks triggers from reaching the ROCs and sends empty data packets to the FED with an error code asking for a rest.

III. Readout Chip Development

A simplified 22*30 readout chip has been designed and produced in 1998 both in the DMILL (DM_PSI30) and Honeywell RICMIS IV (HW_AC30) technologies. In those chips the time-stamping mechanism was present but the zero-suppression within a double column and the data buffers were not implemented

Since then all required functional components have been designed and tested on independent test structures. In July 2000 a fully featured chip has been submitted to DMILL (DM_PSI41). It is a 36*40 pixel array and includes all blocks needed for the LHC operation at full luminosity :

1. A fully functional pixel cell (with 127 transistors/cell).
2. A fast (1.8 GHz) empty pixel skipping mechanism.
3. A 9 * 8 bit time stamp buffer in each double column.
4. A 24*4 analogue data buffer in each double column.
5. 2 * 8 bit clock counters and 2 * 4 bit trigger counters.
6. A pixel programming mechanism, which includes a 3 bit threshold and a 1 bit disable switch.
7. A safety mechanism to bypass defective pixel cells and defective columns.

The chip is expected to arrive for testing in January 2001. The final readout chip is planned to be submitted in spring 2001.

In our, column drain architecture design, the hit pixels are continuously readout by the fast scan mechanism running at 1.8 GHz. One of the main concerns has been a possible cross talk between the digital search signals and the analogue circuit in a pixel unit cell. In a recent measurement [2] this contribution has been determined to be less than 500 electrons, which is small comparing to the planned threshold of 2500 electrons.

IV. References

[1] CMS The Tracker Project Technical Design Report, CERN/LHCC 98-6, 15 April 1998.

[2] Roger Schnyder, Diplomarbeit Fachhochschule Zuerich, September 2000.