Packaging of silicon particle detectors.

How to adapt microelectronic processes to large dies

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Abstract

In the area of packaging of microelectronic IC, a lot of results exist to reduce the size and increase the speed of the package. This work is the consequence of the progress made in the wafer processing industry and aims at solving on a system level the new requirements of the applications. The same trend can be seen in particle detectors packaging; though the amount of work in this area is much more limited. With the advent of large-scale silicon based detectors, the need for a reliable and efficient packaging of large area chips emerged. The same trend was seen years ago for sensors and actuators that, after years of design effort, felt the need for efficient packaging. By selecting, and if needed slightly modifying, current technologies, companies were able to bring a whole range of products to the markets. CSEM was one of the companies that participated to this effort and invested in an assembly facility dedicated to Microsystems.
In this paper, we will review the major processes, from probing to final packing, used in packaging of sensors and study their specificity compared to conventional ICs. We will then present the available technologies and competencies at CSEM, especially a high precision placement robot able to do 3-D assembly, together with dicing, double side probing, reliable bonding of large number of bonds on small pitch or consideration for shipment and storage. Finally, the potential of new technologies to the particle detectors activity will be evaluated.

I. NEED FOR PACKAGING

The purpose of the package is to link the die (active or passive function) to its outside world. It facilitates its handling and connection. At least three main levels of packaging are identified [1]:

First level packaging, which directly links the chips (usually made of silicon) to its housing (like DIL or metal can packages).

Second level packaging relates the packaged chip together, like various SMD packages on a PCB.

Finally, third level packaging is that of the various cards together like boards in a test rack or inside a computer frame.

Recent technology developments (e.g. Chip On Board) tend to suppress these distinctions and unify all levels into one like in MCM (Multi Chip Modules) [2].

Independently of which level, one can divide the functions of packaging into three main categories:

Mechanical function: in a first approach it is that of the protection for the fragile chip against the outside world, but also the ability to manipulate or handle it efficiently. Some extra functions include also that of heat removal since it is mainly an issue of material selection and mechanical path for heat exchange.

Electrical function: it is in most cases the most important since signals need to be brought in and out of the chips as fast as possible and with the lowest distortion. It usually competes with the mechanical function, since issues are opposite (small leads give better signal, but are more difficult to realise and do not dissipate much heat).

Chemical function: it is known that silicon dies can be damaged by corrosion, usually enhanced by heat, mechanical stress, voltage or combination of any of them. This is why the package has also a chemical function, to prevent such corrosion or at least slow down reactions.

Depending on the design, these functions can be applied to any level of packaging as indicated above.

Regarding silicon based large area particle detectors, most issues are linked to the first level packaging. Electrical issues are present at all levels due to the complexity of the signal measured.

II. PACKAGING PROCESS FLOW

Packaging usually starts at the wafer level and finishes with a fully packaged die that can be handled in most environments. The various steps to reach this goal are summarised in fig.1.

Wafer Testing:

The first step is that of electrical testing. Chips are made through a succession of modification made by masking technique. Any defect occurring during any of these operations (amounting in hundreds) can lead to a non-functioning device. Since most defects are local, each die needs to be tested (as much as possible) before any assembly work starts. This is done on the wafer itself

using scanning contact needles and very fast signal generators. Bad dies are inked to be rejected, and results usually stored for tracking or binning purpose. It should be noted that most chips can not be fully tested (question of time, cost, heat, signal speed…) what leads to reject of packaged dies at the final test or later. Semiconductor industry market offers plenty of automatic test systems allowing a fully automatic cassette-to-cassette test, usually supported by custom software for on-site data analysis and bad chip inking.

With the advent of MCM technology, a large effort (labelled as Known Good Die) was made to guaranty the properties of the chip before assembling it to the other ones.

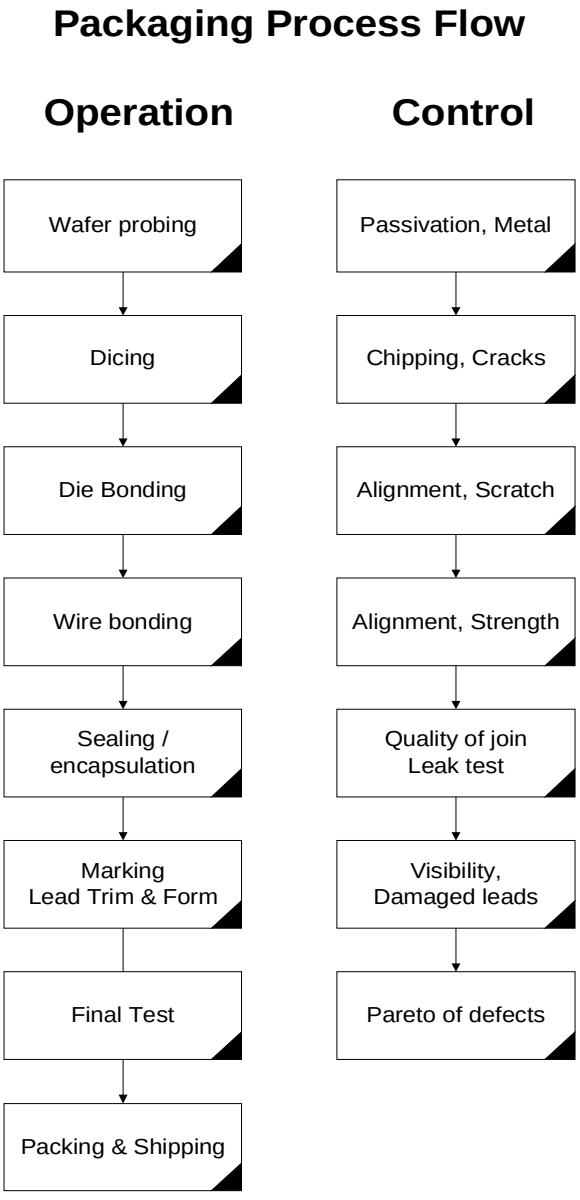

Figure 1: Packaging process flow

Dicing:

Once good dies are identified, they need to be separated from bad ones. This is usually done using wafer saws especially designed for silicon. A thin blade (20 to 150 microns in width, made of hard material like diamond powder) cuts through the silicon or another material (GaAs, $LiNb_3$, Glass...). In order to keep the pieces together, the wafer is glued before dicing on a special tape or maintained by ice. For complex shapes, laser or water stream techniques can be used.

Die placement / bonding:

This is usually one of the most critical steps. More and more precision is asked for this step. The precision can be needed for the final application, but also to guaranty automatic assembly, done with powerful Pattern Recognition Systems. The die is usually held with special tools (vacuum tips or custom tweezers) and positioned on its housing or substrate. Joining is done using glues, brazing or soldering, or using the mechanical pressure of the package. This operation is very depending on the design phase since proper match of the joined materials properties is required to prevent destruction of the fragile die during processing (usually due to thermal mismatch during curing operations).

Electrical interconnect:

Several techniques exist for this process [3]. The most used one is that of wire bonding, using combination of heat, ultrasonic energy and pressure to join aluminium or gold wire (12 to 500 microns for power) to the metalisation of the chip. Several variations have been developed around this basic technique like TAB where all connections of the chip are made to a leadframe through small gold bumps that have been deposited during wafer processing. A further development is that of Flip Chip, where no leadframe exists between the chip and the substrate. The chip is joined directly with its active area on the substrate with small gold or SnPb balls that act as mechanical and electrical joint between chip and substrate. This technique allows for precise placement of the chip and faster interconnects [4]. It also gives a more efficient use of silicon area since the whole surface can be used for connection and not only periphery, like for wire bonding.

Sealing or capping:

This operation protects the chip from outside aggressions. It can be made by gluing, welding or soldering a cap on the housing, giving usually hermetic packages. Plastic encapsulation or potting provides cheap solution for mass-market products. For new technologies, where the chip is directly bonded to a multichip substrate (PCB or ceramic hybrid), a simple coating of polymer is usually applied (called glob top). This operation has a great influence on the cost of the package and its resistance to aggression. It should be evaluated during the design of the whole system.

Identification, leads and trim.

During this set of operations, all steps that are needed to do further processing of the package are done. It includes separating the package from the leadframe for injection, bending / cutting of leads and identification.

Final Test:

Packaged device testing is the very final probing step in which the device is tested for its functionality using on-purpose test boards (most of times designed for an on-site signal treatment) and again automatic test systems.

This operation, similar to the first one, makes sure that no damages were induced during the various steps and for some products allows for a more complete testing since devices are now properly connected (high speed test, temperature test…).

Packing and shipping:

In this step care is laid on guarantying that components will not be affected by these operations. Influence of humidity, shocks and vibration are considered and minimised when possible.

Quality control:

For all the above operations quality checks, either statistical or 100%, are performed. A large part is optical control, where defects (scratches, passivation defects, and badly positioned wires) are looked after using microscopes. They are used to guaranty that the pieces are not damaged and can go further in the flow. Other quality test verify the good flow of the process, their results can be used for Statistical Process Control. Leak test for the sealing operation, pull or shear test for die / wire bonding, are some examples of these quality checks during operations.

III. ADAPTATION TO DETECTORS

The typical process flow described above is adapted to mass market products. For large dies as the ones used for particle detection, some differences apply which will be described in detail according to the process flow. From the special application of these particle detectors, major design differences exist which will not be detailed here but listed for better comprehension.

Design considerations [5], [6]:

The three above-mentioned functions have a slightly different meaning when applied to silicon detectors:

- Mechanical function: rather than protecting the chip, its function is that of adding some stiffness to the overall structure and connecting the components which constitute a readout module. In fact usually no boxes or closed containers are used, but just support frames and boards, whose main requirements are rigidity and stiffness as well as lightness and good thermal properties. Of course, also mechanical protection is a kind of issue, especially because assembled modules have non ordinary sizes (from 20 to 70 cm and more), which calls for safe and easy handling. The considerations that usually drive the choice of materials and packaging techniques are:

1. Radiation hardness and minimal amount of material , minimising the interference with particle detection;
2. Thermal conductance and dilatation coefficient, in order to optimise cooling (usually done by cooling pipes) and reduce mechanical stress at interfaces;
3. Stiffness and low weight to improve mechanical properties keeping a very low total mass, critical in last generation's Silicon Vertex Trackers (SVT).

- Electrical function: signal propagation from detector to detector is not such a critical issue and standard daisy chaining of readout strips by micro bonding assures optimal connection. Nevertheless, recently for some special applications, new techniques, like bump bonding and rigid head-to-head connection, are being analysed. Electrically connecting the detectors to readout electronics is a much harder task, whose main challenges are:

  - Pitch adaptation: from the very high number of readout channels coming from the detectors to the lower number of readout chip channels. This is usually done with an on-purpose designed High-Density Interconnect (HDI) ceramic hybrid, optimised for grounding scheme and signal propagation.
  - Heat dissipation and chip cooling: due to the extremely high number of channels, even a very small power consumption per channel will result in a considerable amount of heat to be removed. Though all components must be designed in order to assure quick and efficient dissipation as well as good performances and stability with temperature;
  - High readout speed and low distortion: in high radiation environments, where a very high rate of events exists, signals must be read out and treated without excessive delays and loss of information, so every electrical connection must account for these issues.

- Chemical function: silicon detector's working environment is a very special one, perhaps more protected for what concerns usual contamination or corrosion phenomena, but very aggressive and damaging because of high radiation. Moreover, maintenance periods of an SVT are very limited in number and time and this calls for good resistance against any type of chemical degradation of materials. This type of considerations also drives choice of materials and components.

All these issues influence greatly the design, what governs later assembly of detectors. The various adaptations of the process steps will now be described.

Wafer test:

Besides their large sizes, detectors differ by two main characteristics:

- They can be double side processed
- High voltage test is required.

The second issue is quite simple to fit with current technologies. It mainly requires some modification of hardware and safety procedure to prevent accident. It is also used in the power electronic industry.

The double side issue is more delicate, since most machines are designed for single side processed wafers. Special care has to be taken to handling of wafer as well as methods for backside polarisation.

The large size of the wafer has one more consequence for testing. Since contact are distributed along the side of the detector and most detectors are 10 or 100 time bigger than a standard chip, all contacts can not be tested at the same time. Instead, at each step of the prober, usually designed to move to next chip, a subset of the strips is tested and the whole detector is scanned this way. Extra care has to be taken during this operation since the machine may not have, in the considered viewing area, any reliable alignment marks what leads to damage to the pads. This explains why optical control is of prime importance for detectors.

Dicing:

For this operation's adaptation to detector work, several considerations exist:

Since most devices are not passivated, an adapted cleaning treatment needs to be done right after dicing.

The dicing process itself has to be well adapted and controlled. Unlike conventional ICs, detectors use the whole thickness of the wafer. It is then important to guaranty a high quality of the diced area. Any chipping or cracks in this area, which can not be seen from the top surface, will induce electrical defects.

Finally since assembly usually requires very tight tolerances. Mechanical dimensions need to be well-controlled on large areas, what makes it more difficult.

It is also important to mention the special care needed to dice thin wafer or double side detectors.

Die placement /bonding:

For this operation, the large size of the die is one of the major concerns. Manual assembly is done using special gears. Dies are aligned to a precision of about 10 microns and held together during polymerisation of glue. The long stacks are then glued on special carriers made of carbon fibre-reinforced composite carriers.

In order to do such assembly on automatic machines, the following requirements are needed:

- Precise alignment capability
- Large field of view for the PRS system
- Large working area since dies are around 3.5"
- Capability to polymerise glue in situ

Wire Bonding:

For wire bonding, the speciality of these assembly is the large number of bonds as well as the difficulty to do re-bond, due to the fine pitch of the devices.

For such a large number of bonds (typically 1000 bonds), reliability better that 99.9% is required. This is beyond most equipment in production lines. To be able to bond these dies, several adjunctions are made to the machine. Most recent machines detect when the bond process did not go well and stop; this allows for manual bonding to occur. In some cases, an extra camera can be added to detect the absence of wire before the bond is made.

Sealing or capping:

No such operations are performed since the devices are encapsulated in the final assembly housing.

Identification:

It can be a critical issue, since no space is available on the devices and tracking is of prime importance. Several scribing trials are under way.

IV. CSEM OFFER FOR ASSEMBLY

For years, CSEM has been active in the field of Microsystems fabrication. This includes design, fabrication of wafers, test and assembly. This experiences spans from accelerometers, where assembly stress and precision are of prime importance, DOE where each system is composed of one wafer and MOEMS where assembly precision is the selecting criterion. Current work for detector includes wafer test and dicing, and analysis is made for detector assembly.

Wafer probing:
Testing of silicon detectors is done at CSEM at wafer level (undiced) and special procedures as well as customised systems have been developed.
In fact, detector probing differs from standard IC testing for several aspects, mains of those being:

1. absolutely non-standard device geometry, asking for complex test patterns;
2. non-repetitive contact pad patterns (e.g.: wedge detectors), needing accurate site-by-site prober positioning;
3. high number of contact pads that calls for finding a compromise between using the largest number of

probe pins (in order to minimise prober movements) and reducing parasitic effects between tips;
4. need for a backside contact, which is even more stringent for double sided (DS) devices; in this case not only a simple contact is required, but in a very small and precise zone of the backside;
5. wafer handling that becomes quite critical especially for DS detectors;
6. high voltage testing, fairly common in power device testing but quite unusual for standard ICs.

CSEM faced all these aspects using both technical general knowledge and specific experience acquired in several years of manufacturing of silicon detectors. Every aspect has been analysed and solved with a close collaboration between back end and design group in order to make sure that every incoming project had testability insured. Specifically:

a) for the above listed item 1, a set of design and layout rules has been implemented, accounting not only for technological issues, but as well for testability; an automatic design rule check (DRC) is then run on every new design in order to check its compliance with those rules;
b) for item 2, particularly for wedge detectors, probe patterns are extracted directly from mask design and layout extremely high accuracy is this way transferred to probing, accounting for any positioning offset introduced by the test system;
c) for item 3, designing and choosing a probe card is done keeping under control both sides of the problem;
d) item 4 has been solved by modifying a standard test system in order to allow backside contact in a selected zone and developing a special technique that now allows CSEM to perform a full automatic DS test;
e) of course item 4 and 5 are strictly related, and modifying the test system included taking care of wafer handling, so no damage is induced on the backside while testing the front;
f) finally, high voltage instruments and connection matrixes have been inserted in our test system in order to allow a complete and safe high voltage testing.

Moreover, as sometimes detector testing is not just an on-off step, in which only two categories exist, good or bad chips, dedicated software programs have been written in order to perform an offline data analysis and critical parameters monitoring.
In fact, for silicon detectors data analysis goes a little beyond what is merely good/bad chip selection, and grading is often related not only to compliance/non-compliance with chosen specifications, but also to some second order parameters that affect the overall quality.
Most of the times this requires a deeper analysis of electrical results, and this way CSEM assures full quality control of the production and a quick feedback to the wafer fab.
Last but not least, sample testing of diced devices, even if done only manually, adds more control on chip quality and helps monitor dicing process reliability, not to affect device electrical features after cutting.
This is done at CSEM using a manual probe station, equipped with proper instruments and specials chucks for single and double side detector holding.
This system is also useful for failure analysis and aimed measurements when further investigations are needed to solve a specific problem.
Covering all aspects of electrical test and quality check is though crucial for any IC as well for silicon detectors, whose special requirements call for a continuous upgrading and adapting of standard and customised test systems.

Dicing:

At CSEM, mechanical and electrical considerations are always present during dicing of detectors. Precision dicing on double side wafer is offered with a precision better than 15 microns, which, for large wafer implies good control of machine, blade and dicing foil. For this type of product, dicing has been adapted in order to minimise rejects:

a) an appropriate structure of the dicing channel at a technological level, as well as an accurate choice of dicing alignment marks, allow to reach the required geometrical dimension accuracy; blade thickness and dicing parameters are also tuned to achieve an optimal precision ant to minimise edge chipping;
b) the above-mentioned precautions are also strictly related to damage reduction, whose control is the main purpose of dicing procedure tuning;
c) surface contamination is eliminated by performing a combination of cleanings and thermal treatments after cutting; based on our experience of these devices as indicated in Fig.2 and 3, showing the I-V measurements (guard ring and bias line currents) on one sample that showed a low voltage sharp breakdown after cutting.

The improvement is easy to notice: both currents decreased after the treatment, and for the guard ring breakdown occurs at a much higher voltage (740 rather than 200 V).

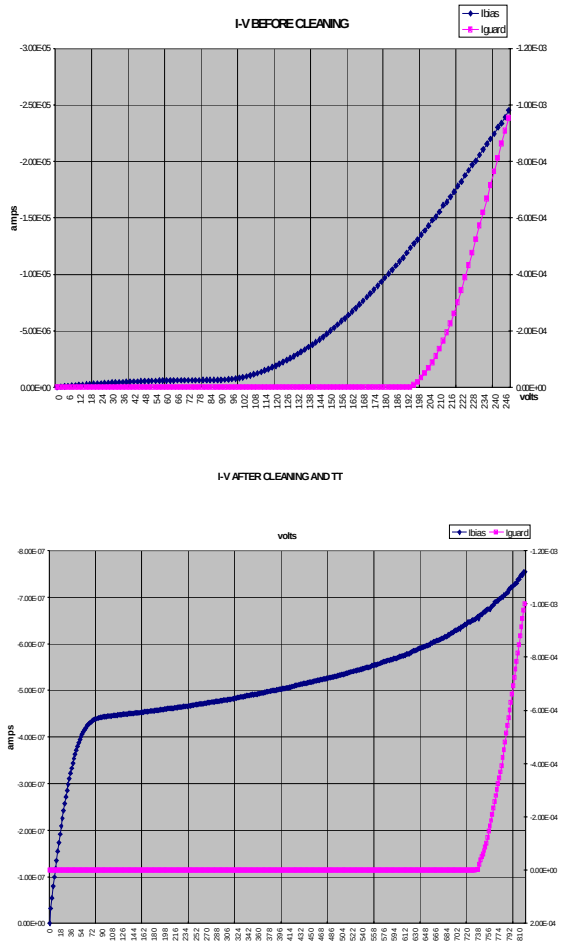

Fig.2 and 3: results of treatment after dicing

This technique, joined with the long experience of our technicians, allows the cutting even of very complex detector shapes, like the one depicted in the next picture.

Fig.4: Example of special shape

Die Bonding:

Large investments were made for a flexible assembly line able to work on small and medium quantities of various products with an emphasis on precision. This led to the joined development of a precision assembly robot in 98, which now is used for most assemblies. It has a precision of the order a few microns and a working area of 4 x 6". Some of the special features of the machine include:

- State of the art pattern recognition system, able to adapt to varying contrasts (useful for sensors made in small quantities)
- Innovative vision, with the camera axis fully perpendicular to the assembly plane. This feature, combined with dedicated vacuum holding tips, allows for final correction to reach micron precision
- Very precise axes with 0.5 micron resolution
- Height measurement laser system
- Force sensor for touch down detection with threshold
- Possibility to view the piece being assembled from top and bottom.

Pieces are held on a carrier that is compatible with other assembly equipment like for wire bonding.

Wire bonding

Wire bonding is fully automatic on equipment with PRS recognition. In order to accommodate various type of housing, substrate and dies, bond quality is monitored on line. For each bond, the deformation of the wire can be recorded as a function of time. The curve is viewed and any deviation from set limit leads to a process interruption.

Fig 5: Automatic wire bonding equipment

Other processes include low-pressure neutral gas sealing and conventional glob top facility.

V. CONTROL AND EXISTING STANDARDS

As indicated in Fig. 1, several controls are made along the flow of operations. They are designed to eliminate pieces with defects that can not be repaired and correct the process in case it drifts away from ideal setting.

Lots of standards exist that are related to a particular market (Medical, Military [7], Automotive). When choice is offered, people select the one best adapted to their needs [8]. We will review some of the controls usually made and link it to some popular standards.

Wafer Optical Control:

This test is made before or after testing depending on the level required. It looks for defects from the wafer processing or the test/ dicing operation. Die are looked using 10-50 magnification under microscope and defect families are looked after like:

Defect in passivation or metalisation (absence, crack, and marks of test needles)

Aspect of chip edges (broken corners, chipping, cracks, wrong dicing). Some standards (MIL STD 883E, Method 2010.10) give conditions for side inspection of chips.

Die Bonding:

The control is done optically and mechanically. With optical methods, the quality of the alignment of the die regarding its substrate is controlled. Excess of glue contaminating the top surface or the bonding pads is also looked after. The control also checks for any damages induced by the operation (e.g. scratches due to picking tool).

Using calibrated equipment, shear test can be performed. The force needed to remove the die from its substrate is measured on several samples, together with the type of failure (in chip, in adhesive…). This destructive test helps find defects like contaminated surfaces, cracks in adhesive / solder layer, wrong wetting / wrong polymerised glues.

Wire Bonding:

Performed controls during this operation are similar to those for die bonding.

Optical controls verify presence of all bonds, position on the bonding pads of the chip and substrate (centring, tail over the circuit) as well as position of the wire to each other (no touching, crossing….).

Mechanical tests can also be performed, the force to shear or pull break a bond is measured and type of failure (at foot of bond, in wire, delamination, chip metalisation failure) analysed. For some products where all bonds need to be checked, a non-destructive test is performed where the bond is pulled until a threshold value, well under known failure values. It is intended to isolate weak bonds. This parameter is well adapted to Process Control, using SPC graph.

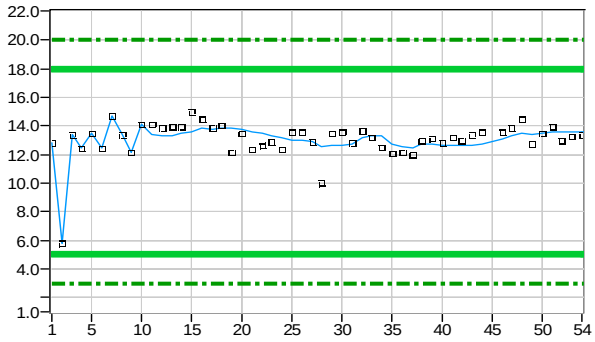

Fig 6: SPC Graph of bond wire pull strength with control limits.

Sealing or capping:

Control for these operations depends greatly on the technology used. Optical control is always a big part of it. Integrity and appearance of solder joint or welded surface is checked for material missing, excessive corrosion, porosity, and mechanical damage.

For plastic encapsulation, bubbles, cracks, bad adhesion to substrate and other symptoms of creapage path for water are looked after.

A common test used for hermetic is that of leak testing. So called gross leaks are tested by pushing an organic solvent inside the cavity using high pressure. After this so-called bombing treatment, the pieces are immersed in a bath held at a temperature higher than the boiling point of the solvent. If a leak is present, solvent infiltrates inside the package and will escape when led to boiling, showing small streams of bubbles in the bath. This very simple technique helps evaluate the gravity of the leak and its location. So called fine leaks are tested using similar techniques with smaller atoms. The test medium is Helium, forced inside the cavity using pressure and detected with a mass spectrometer. Leak rate range detected with this method is between 10^{-7} to 10^{-9}cm^3/sec. The threshold can be set at any requested value. This test has to be used with care regarding porous materials since helium adsorbed on surface can induce an apparent leak that does not exist. This especially applies to plastic materials.

Identification, leads and trim

The purpose of these controls is to make sure that the component will keep its tracability and can be further processed.

It has two areas of investigations:

- detect small defects that can hinder further assembly: bad quality identification, bent leads, absence of metalisation. This is done by optical control.
- make sure ageing will not affect these properties.

The resistance of the identification to solvents is checked if needed, as well as resistance to wetting of surfaces for component which needs soldering steps.

Reliability:

it is difficult to decide if these steps should be in the description of operations or that of standards. Depending on several factors like security, size of market, cost of repair, a more or less extensive reliability study is necessary to identify failure modes and propose solutions to fix them. In some cases a burn-in cycle, which activates such defects, can be proposed to remove parts with premature failure.

Extensive tests exist for reliability check. They can be divided in several categories:

Electrical: they are made of large number of powering or signal sequences.

Mechanical: their goal is to create a mechanical failure in the system, using mechanical (shock, bending, vibration, pressure) and or thermal stimuli (sudden or slow temperature change as well as storage temperature) [9].

Chemical: the resistance and influence of chemical species (humidity, solvents, salt, acid…) are analysed during these tests.

Radiation: Similar to chemical test, influence of radiation (light, UV, other radiation) is investigated during these experiments.

In most cases, a combination of tests of different categories is used. Thermal cycling with powered devices is common, vibration during thermal cycling is of lesser usage.

VI. CONCLUSIONS

A wide knowledge exists for packaging of electronic dies. It mainly comes from the microelectronic industry. For special applications like sensors or power electronics, industries tend to derive and adapt processes and standards to their needs.

For years CSEM has been active in adapting processes to handling and assembling of fragile dies. This led to an assembly facility with automatic equipment dedicated to packaging of sensors.

This experience of production, with strong support from design, can easily be adapted to large area particle detectors. It will mean the continuity for a company already active in the fabrication of particle detector wafers.

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