PERFORMANCE AND IRRADIATION TESTS OF THE 0.3 μm CMOS TDC FOR THE ATLAS MDT

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Abstract

ATLAS Muon TDC test-element group chip (AMT-TEG) was developed and tested to confirm the performance of critical circuits of the TDC and measure radiation tolerance of the process. The chip was fabricated in a 0.3 μm CMOS Gate-Array technology.

Measurements of critical elements of the chip such as the PLL, and data buffering circuits demonstrated adequate performance.

The effect of gamma-ray irradiation, using a Co^{60} source, and neutron irradiation, using PROSPERO reactor in France, were also examined. The test results revealed radiation tolerance adequate for the operation of the circuits in the environment of the ATLAS MDT.

1. INTRODUCTION

High-resolution, low-power and low-cost VLSI TDC's are required in the ATLAS precision muon tracker (MDT: Monitored Drift Tubes). The MDT requires about 370 k channels of sub-nano second TDC to realize the high resolution of the MDT.

Although we have developed several TDCs which fulfil some of the basic requirements, the ATLAS MDT TDC has more demanding requirements especially in data handling. Thus we have began a project to develop a new TDC chip called the AMT (ATLAS Muon TDC) [1] in collaboration with the CERN microelectronics group. To study the chip architecture, intensive Verilog simulations were done [2]. In addition, a quick test chip was developed in a 0.7 μm CMOS process [3] for a medium scale test (10 k channels) of muon front-end electronics.

Since the mass production of the chip is scheduled for year 2001, we have selected a relatively advanced process, 0.3 um CMOS Gate-Array technology (Toshiba TC220G), for the final TDC chip. This new process provides a lower per channel cost and higher performance. In addition, we can expect a longer lifetime for the process, and, in turn, easier maintenance.

To measure the basic performance of the design and confirm the radiation tolerance of the process, we have developed a test element group chip (AMT-TEG) using the 0.3 μm process.

The chip contains bare NMOS and PMOS transistors, a ring oscillator for radiation tests. Gamma-ray irradiation was performed with a Co^{60} source at Tokyo Metropolitan University. Neutron irradiation was performed at the PROSPERO reactor in France.

Photograph of the chip is shown in Fig. 1, and a block diagram of the AMT-TEG chip is shown in Fig. 2. There are 24 input channels in the chip. These inputs are connected to three 8 ch ASD chips [4] in the MDT design. To reduce number of input pins, only 16 hit input pins are implemented and selectively connected to internal circuitry in this AMT-TEG chip.

The AMT-TEG chip contains most of circuits used in the final AMT chip. Only the trigger interface and trigger matching circuit are excluded. In addition some circuits were simplified and error checking was minimized.

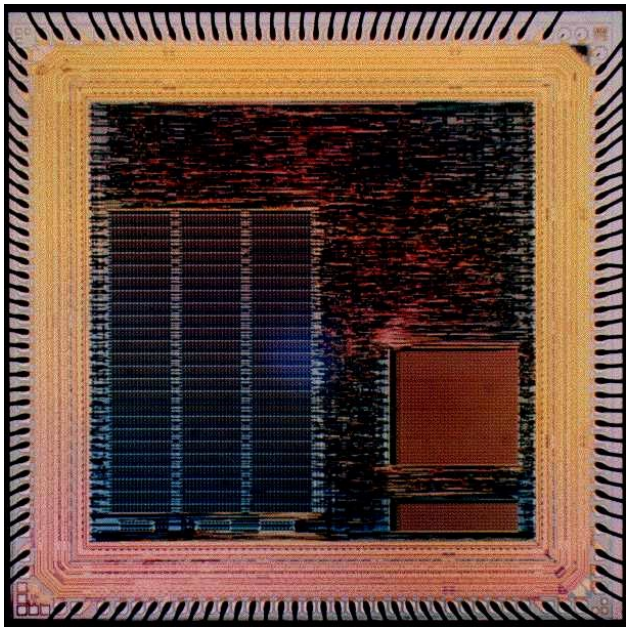

Fig. 1. Photograph of the AMT-TEG chip. The size of the chip is 5.2 mm by 5.2 mm. Total number of gates used is about 70 k gates. The large block in the left side is the 24-ch channel buffer.

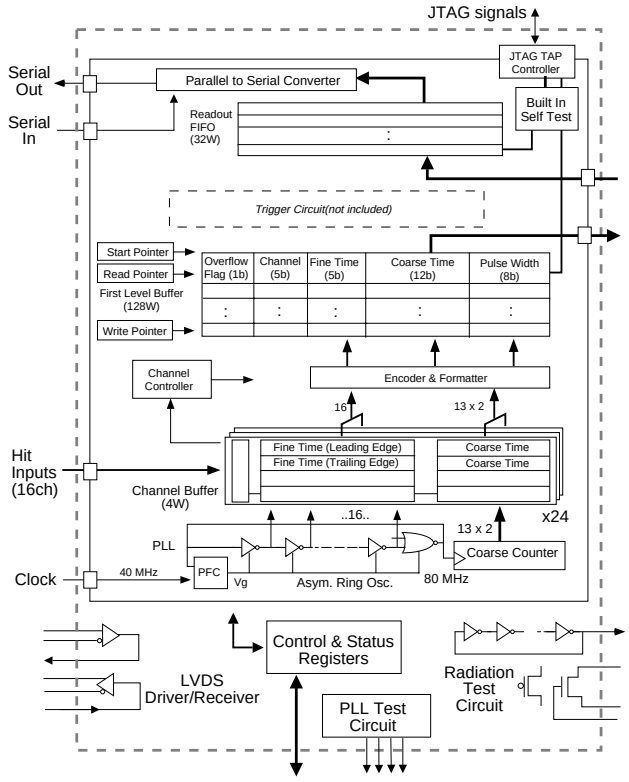

Fig. 2. Block diagram of the AMT-TEG chip.

Since the detailed operation of the chip is described in other documents [1, 2], only brief explanation is presented here.

The hit signal is used to store the fine time and coarse time measurement in individual channel buffers. The fine time measurement is obtained from taps along an asymmetric ring oscillator. The time of both leading and trailing edge of the hit signal can be stored.

Each channel has a 4 word buffer where measurements are stored until they can be written into the common first level buffer.

To achieve a high-resolution time measurement with sufficient stability, Phase Locked Loop (PLL) is used. The PLL circuit produces a double frequency clock of 80 MHz from the LHC clock (40MHz). By dividing the 12.5 ns clock period into 16 intervals a time bin size of 0.78 ns is obtained.

2. PERFORMANCE TEST

2.1 PLL and Ring Oscillator

Although the chip is designed in a gate-array technology, layout of the time critical parts such as PLL and the asymmetric ring oscillator were designed manually to achieve high resolution.

We determined the jitter of the PLL circuit by measuring the oscillation period of each cycle. RMS values of the measurements versus frequency and power supply voltage are plotted in Fig. 3 (a) and (b) respectively. The jitter of the PLL is small (< 140 ps) and stable for the 40-120 MHz frequency range and for supply voltages between 2.8 - 3.8 V (normal operating condition is 80 MHz and 3.3V respectively).

The jitter shows a small structure around 90 MHz and the value is a little worse than that of the previous chip [5] which was fabricated in a 0.5 µm process. However the jitter is still small enough for the MDT detector which requires 500 ps resolution. Additional attention will be directed to the layout around the PLL in next chip to achieve better stability.

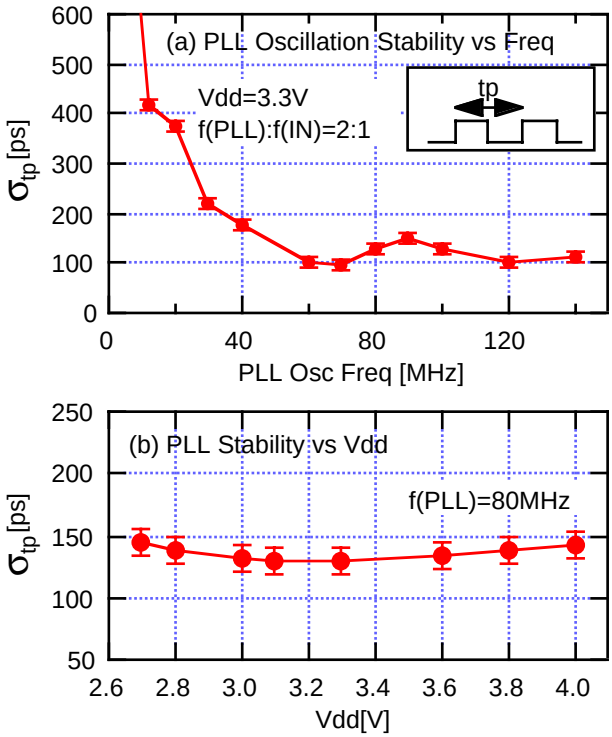

Fig. 3. (a) Stability of the PLL vs. oscillation frequency. (b) Stability of the PLL vs. supply voltage.

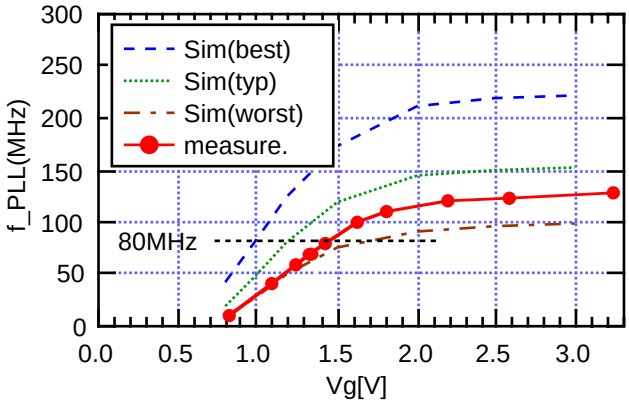

Fig. 4. Simulation and measurement results for the oscillation frequency of the asymmetric ring oscillator versus control voltage Vg.

Fig. 4 shows the control voltage (Vg) dependence of the asymmetric ring oscillator. Results from simulations for worst, typical and best conditions are also indicated. In the present chip, maximum frequency of the oscillator is 130 MHz, and well beyond that required for the 80 MHz operation.

2.2 Two Edge Separation

Recording speed of the channel buffer is important to have a good double pulse resolution or edge separation.

Minimum edge separation was determined by reducing pulse width and pulse separation until the hit information is lost.

Fig. 5 shows an example of minimum pulses. Two leading and two trailing edge timing are successfully recorded in the 4 word channel buffer. Since the test instruments can not generate pulses shorter than 5 ns, actual performance of the chip may be better than 5 ns, which is already far better than the MDT requirement.

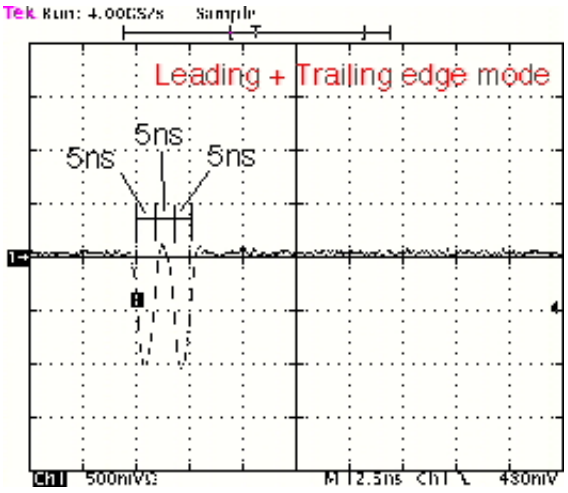

Fig. 5. Minimum pulses successfully recorded in the AMT-TEG chip.

2.3 Data Buffering Speed

The data transfer speed from the channel buffer to the first level buffer is an essential part of this TDC architecture. If the channel buffer become full, further hit information will be lost. In a Verilog simulation, the probability of hit loss is very low ($< 10^{-6}$) for 300 kHz input rate in all channels.

The transfer speed is measured by changing the number of simultaneous hit channels and determining the minimum hit interval where all hits are accepted.

In Fig. 6 we plot minimum hit interval for N channel simultaneous inputs. Above the data point all hit information is recorded, but if the hit interval is reduced less than the data point, a part of the hit information become lost due to the lack of the transfer capability. The line in the figure shows expected speed from the circuit. We see the overhead for arbitration is only 2 cycle and successive data transfer occurs at each cycle.

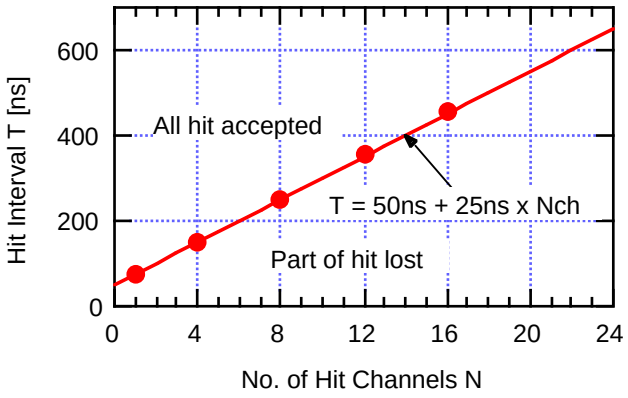

Fig. 6. Minimum hit interval for simultaneous hit inputs. System clock cycle is 25 ns. The data points show minimum hit intervals and the straight line indicates the expected performance from the 2 cycles plus N cycles required by the design.

2.4 Time Resolution

Time resolution was measured by supplying a clock synchronous hit signal to the input and varying the delay time of the signal. The result is shown in Fig. 7. The RMS value of 305 ps is obtained. This value is worse than that of previous TDC chip [5] which achieved 250 ps resolution, but still has adequate resolution for our purpose.

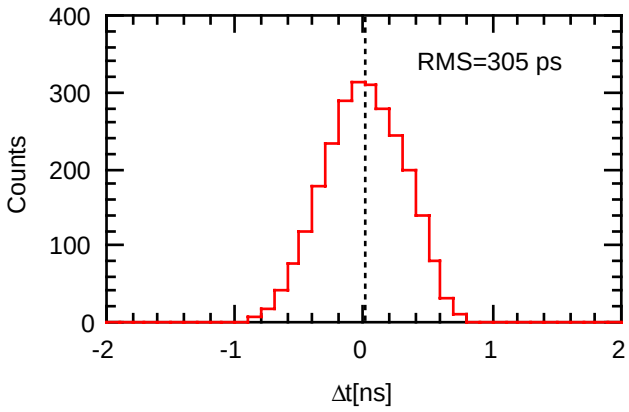

Fig. 7. Time resolution measurement. Input clock frequency is 40 MHz and time bin is 781.25 ps/bit. The data contains digitization error of 225 ps.

2.5 Non-Linearity

Non-linearity of the time measurement was measured by applying a hit signal for which the delay time is uniformly distributed, and counting the number of hits recorded in each bin. The Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are shown in Fig. 8 (a) and (b) respectively. Both are small enough (RMS < 70 ps) for our purpose.

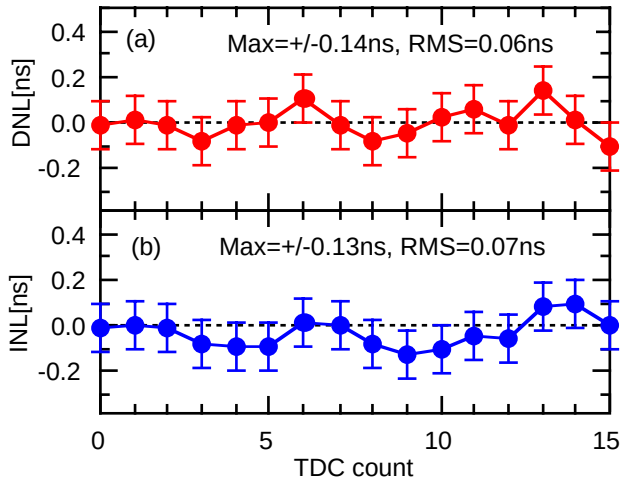

Fig. 8. (a) Differential non-linearity, and (b) Integral non-linearity measurement.

3. IRRADIATION TEST

3.1 Gamma-ray Irradiation

Gamma-ray irradiation test was done at Tokyo Metropolitan University with a Co^{60} source. The irradiation rate was about 90 rad(Si)/sec, and total dose irradiated was 100 krad(Si). During the irradiation so called worst bias conditions for MOS transistors (3.3 V is applied to NMOS gate, and no voltage is applied to PMOS gate), were used. To study post-radiation effects, parametric measurements were also done after annealing (1 week at 100 degree C) following the MIL-STD-883 method [6].

Total dose expected for worst location of the MDT electronics is 11 krad(Si) for 10 years LHC operation (including a factor 4 safety factor) [7].

In a sub-micron process, most severe damage from the ionization process is an increase of leakage current. Fig. 9 shows drain leak current for NMOS and PMOS transistors. An increase of NMOS drain leak current above 25 krad(Si) was seen while no increase is seen in PMOS. Recovery of the pre-radiation condition is seen after the annealing in NMOS.

Threshold voltage shifts of transistors are shown in Fig. 10. There is no shift seen in PMOS transistors and a NMOS transistor while small shifts (~100 mV) are seen in two NMOS transistors. Since these transistors do not have any protection circuit, the transistors are susceptible to damage. More samples are needed to confirm whether the shift is due to the irradiation or not.

Fig. 11 shows variation of oscillating frequency of a ring oscillator and supply current. The ring oscillator is composed of 33 NAND gates. The oscillating frequency becomes lower above 50 krad(Si). The total chip current was also increased above 50 krad(Si).

Considering low dose rate in the LHC environment, we think the chip can be used safely up to 50 krad(Si), thus the chip has enough margin to be used in the MDT environment.

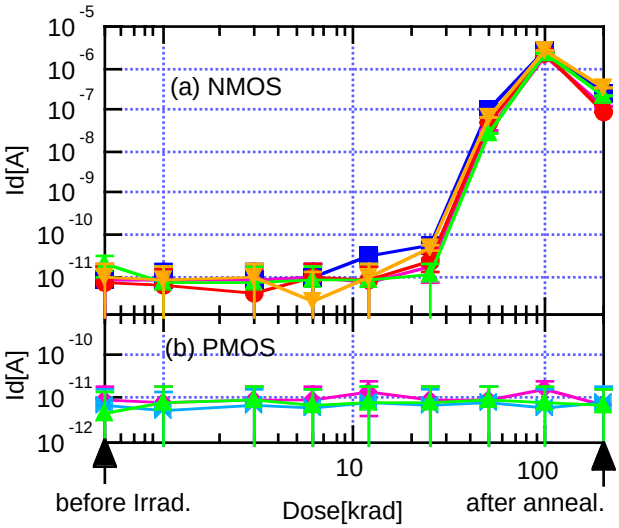

Fig. 9. Drain leakage current of (a)NMOS and (b)PMOS transistors. Left-most and right-most points show the value before irradiation and after 1 week at 100°C annealing respectively.

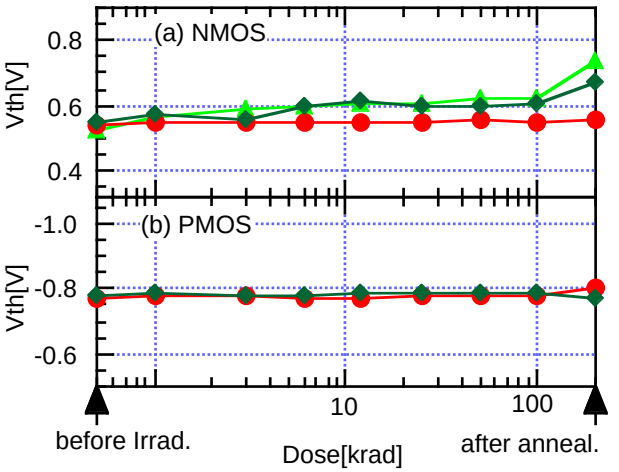

Fig. 10. Threshold voltage shifts of (a)NMOS and (b)PMOS transistors.

Table 1. Summary of the measurements and the requirements.

	Measurements	Requirements
PLL frequency	40 - 120 MHz	80 MHz
PLL operating voltage	2.8 - 3.8 V	3.3 V
Coarse time counter speed	120 MHz	> 80 MHz
LVDS interface	> 100 MHz	> 40MHz
Multiple edge resolution	< 5 ns	< 30 ns
L1B transfer speed	(2+N) cycle	(4+N) cycle
Time resolution	305 ps RMS	< 500 ps RMS
Diff./Int. Non-Linearity	< 70 ps	< 300 ps

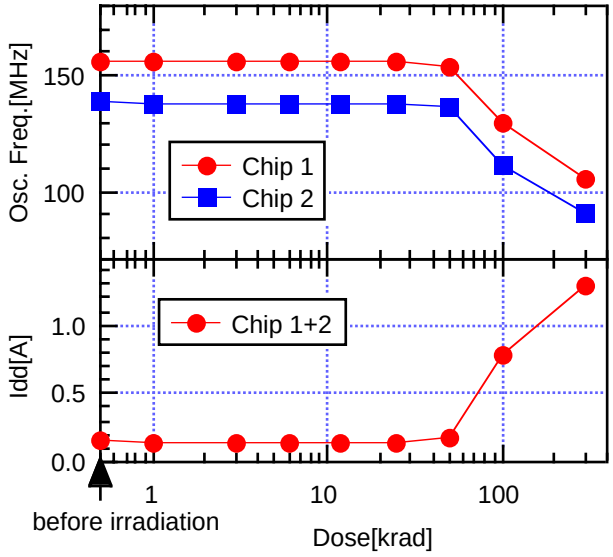

Fig. 11. (a) Oscillation frequency of a ring oscillator, (b) Total current of two chips. Left-most points show the value before irradiation.

3.2 Neutron Irradiation

Neutron irradiation was done at the PROSPERO reactor facility in France. Eight chips were exposed to neutron flux of 1.0 x 10^{13} and 4 chips were exposed to 1.6 x 10^{13} n/cm^2 (1 MeV neutron equivalent). During the neutron exposure, chips are placed in a conductive plastic case. The expected neutron flux at MDT front-end electronics for 10 years of LHC operation is less than 1.2 x 10^{13} n/cm^2 (including safety factor 4) [7].

After cooling of the radioactivity (~ 2 months), we measured transistor parameters and ring oscillator frequency. We have not observed any apparent change in all sample chips.

4. SUMMARY

A test-element group chip (AMT-TEG) for the ATLAS Muon TDC was developed for circuit performance test. Radiation tolerance was also measured for gamma-ray irradiation and neutron exposure.

Table 1 summarize the results of the present measurements and requirements of the TDC. The AMT-TEG chip demonstrated adequate circuit performance for the MDT TDC. In addition, the 0.3 µm process showed adequate radiation tolerance for both gamma ray and neutrons at the radiation level of MDT front-end electronics.

Acknowledgements

We are grateful to J. Christiansen and CERN microelectronics group for their help on the chip architecture study. Authors would also like to thank, R. Richter for help on the neutron exposure, and R. Hamatsu for help on the gamma-ray irradiation.

5. REFERENCES

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