DILOGIC-2 a Sparse Data Scan Readout Processor

For the HMPID Detector of ALICE

H. Witters, IMEC vzw , 3001 Leuven, Belgium (witters@imec.be)
J.C. Santiard , CERN 1211 Geneva 23, Switzerland (jean-claude.santiard@cern.ch)
Paolo Martinengo, CERN 1211 Geneva 23, Switzerland (paolo.martinengo@cern.ch)

Abstract

Processing of analog information is always spoiled by additional DC level and noise given by the sensors or their additional readout electronic. The Dilogic-2 circuit has been developed to process the data given by an Analog to Digital Converter in order to eliminate the empty channels, to subtract the base line (pedestal) and store locally the true digitised information. The analog information will be sent to the ADC by a set of three 16-channel front-end analog processors, the Gassiplex07-3 [1], multiplexed on the same analog line.

I. Introduction

The Dilogic-2 can handle up to 64 channels by group of 16, 32, 48 or 64 channels. The processing has to be done in two steps, firstly pedestals and noise of each channels have to be measured and stored on the chip, then the normal operation can start, zeros will be eliminated and the on-chip memories will be loaded with true value information. The sparse data scan section is made of a digital comparator and a subtractor; the pedestal field has been limited to 8-bits while the data have 12-bits range. These two elements are fed on one side by the digitised information and on the other side by the contents of two separate memories filled respectively for each channel by the chosen level of comparison (threshold) and the pedestal value. Calling PED(i) and SIG(i) the average and r.m.s. values of a pedestal distribution, the operating threshold of the channel (i) is defined as: TH(i) = PED(i) + N*SIG(i), where N is a selectable constant, usually ≥3.
Thresholds and pedestals are first measured and stored in a memory, for every channel; the channel address allows finding the right values of each channel during the processing. A BIT-MAP memory (64w x 16-bits) is filled with "1" for channels above threshold or "0" for channels below the threshold. An analog data FIFO memory (512w x 18-bits) is loaded with the digitised amplitude information (12-bits) and the address of the selected channels (6-bits). An End-Event word turns off the event readout sequence; it contains the number of good channels (7-bits) and the corresponding event number (11-bits). A presettable almost-full flag indicates over-writing the FIFO and an internal 4-bit controller allows to choose the different front-end and back-end operations, particularly one, which is used to test the functionality of the chip.

Finally, the Dilogic-2 can be daisy-chained to allow the readout of several hundreds of channels on the same bi-directional data bus at a maximum speed of 20MHz with a power consumption of 60mW.
The Dilogic2 is divided into three main parts: the front-end that concerns the writing part of the circuit, the back-end with the memories and the different flags and finally the controller. Fig. 1 shows the layout and Fig. 11 describes the block diagram of the Dilogic2.

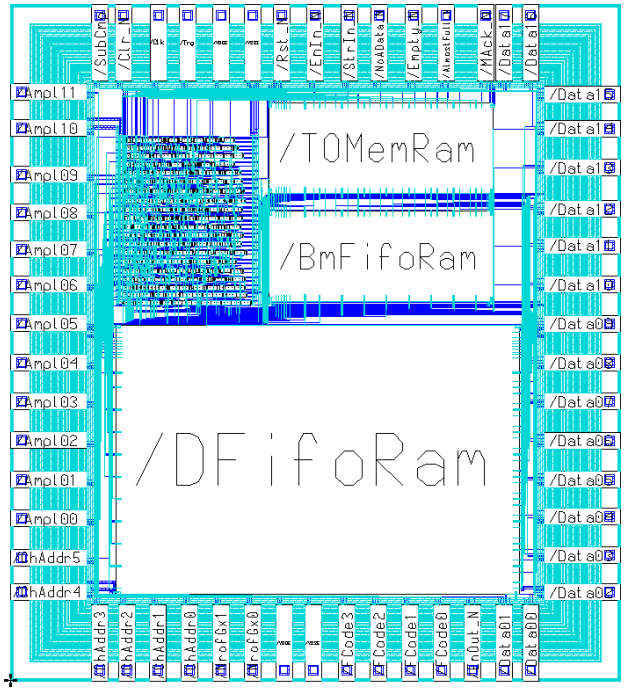

Fig. 1: Dilogic2 layout

II. Controller

There are two main operations that can be performed simultaneously if necessary: the front-end operation and the back-end operation.
The front-end operation reads digital information, in our case from an ADC, makes the necessary calculations and stores the data into the memories.
The back-end operation is connected to an external processor through an 18-bits bi-directional bus.

The controller can instruct the Dilogic2 to perform several operations under the control of the external processor. Table 1 shows the functions that have been implemented and can be activated with a 4-bit code.

Table 1: 4-bit Function code

Function code	Description
0000	Front-end test mode
0001	Load “almost full” preset
0010…0111	No operation
1000	Pattern readout
1001	Pattern delete
1010	Analog readout
1011	Analog delete
1100	Reset fifo pointers
1101	Reset daisy chain
1110	Configuration write
1111	Configuration read

III. FRONT-END OPERATION

A. *Data Acquisition*

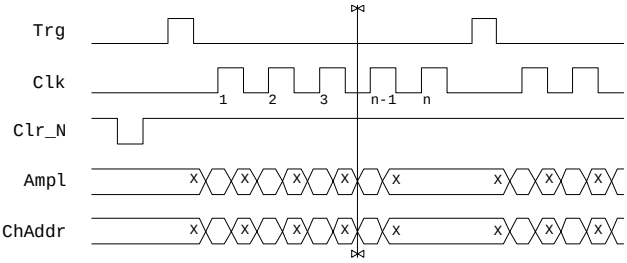

Fig. 2: Data acquisition timing diagram

Fig. 2 shows that, before starting the first acquisition of data the front-end has to be cleared with Clr_N and the back-end with Rst_N. Then the subtraction memory and the threshold memory have to be filled respectively with the pedestal value and the operating threshold of each channel, namely PED(I) and TH(I) = PED(I) + N*SIG(I). The SubCmp pin allows disabling the subtractor and the comparator during the pedestals and the noise measurements.
Every event starts with a pulse on Trg and a number of clocks on Clk that will depend on the number of channels to be processed by group of sixteen. It is defined by a 2-bit code shown in Table 2.

Table 2: Write clocks Vs number of channels

NrofGx	Nb. of input data	Nb. of clocks
00	16	17
01	32	33
10	48	49
11	64	65

When the SubCmp is in the low state (disable), the amplitude Ampl and channel address ChAddr are put in the data fifo memory without subtraction of the offset. When the SubCmp pin is high (enable) the data are only stored if the amplitude is bigger than the threshold. The data stored in the DfifoRam is the amplitude minus the offset and the corresponding channel address.
The pattern word, in every event, can be 1, 2, 3 or 4 groups of 16 bits depending on the number of channels. They are stored in the BIT-MAP memory. Every bit of the pattern word indicates whether or not (1 or 0) a hit has occured on that channel.
An extra clock cycle is necessary to store the end-event word and turn off the readout of an event. The 18-bits of the end-event word are the contents of 2 counters: 7-bits from D00 to D06 give the number of channels above the threshold and 11-bits (D07-D17) give the events numbering. The end-event word is signalled in time by the Mack-N output.

B. *Test mode*

Fig. 3 shows the test mode operation, which is similar to the data acquisition sequence, but instead of asserting the amplitude and channel address on the input pins, they should be filled through the I/O bus, respectively with ChAddr (5:0) on D17-D12 and Ampl (11:0) on D11-D00.

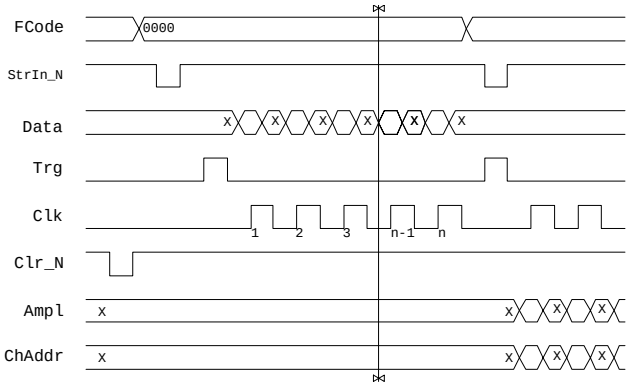

Fig. 3: Test mode timing diagram

IV. BACK-END OPERATION

Most of the operations defined by the function code (Table1) are made in the Back-End mode. We will describe the main functions.

A. *Almost-Full pre-set load*

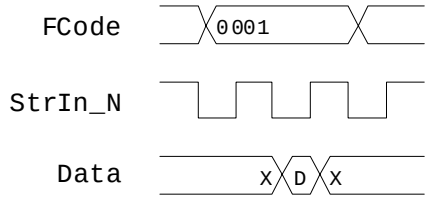

Fig. 4: Almost-full pre-set timing diagram

The load pre-set operation (Fig. 4) loads a register in the data fifo controller with a 9 bit value, D08-D00.
This number is used to compare the read and write address counters. The pin AlmostFull_N goes low when the write counter value reaches the read counter value minus the loaded pre-set. This flag indicates that the data fifo is almost full, and should be used to stop the trigger flow in order to prevent overwriting. If the pre-set is not loaded, the pre-set register defaults to 67 after reset of the Dilogic2 chip.

B. *Analog readout*

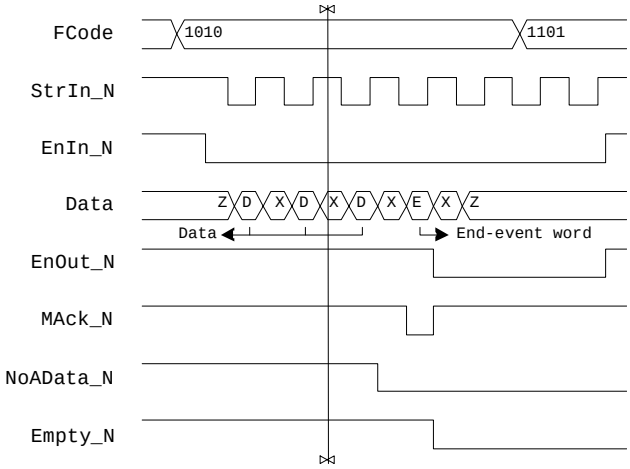

Fig. 5: Analog readout timing diagram

The Dilogic2 chip is put in analog readout mode (Fig. 5) when the function code is set to"1010" and EnIn_N is low.
Successive StrIn_N cycles will cause all modules in the chain to place their digitised data on the data bus one at a time, starting with the first module in the chain. An enable signal is passed from the EnOut_N pin to the EnIn_N pin of the next chip when the module has finished putting its analog data of one event on the data bus.
The Mack_N pin indicates the occurrence of the end-event on the data bus and marks the end of the analog readout on that Dilogic2. At that moment the EnOut_N pin is pulled low to start the readout of the next chip, and Mack_N goes high again.
The analog readout operation is finished when the EnOut_N of the last chip goes low.
All the Dilogic2 have to be reset by applying the reset daisy chain code "1101" and an extra Strin_N strobe. This will reset the EnOut_N pins of all chips in the chain, otherwise they will stay in analog readout mode.
The analog data fifo has 2 flags: the Empty_N flag indicates that the fifo is completely empty and the NoAData_N indicates that there is no analog information in the fifo, but only end-event words. This status occurs when the Dilogic2 has received triggers with empty events. The function code allows deleting the events in the fifo, starting with the first event to be read.

C. *Pattern readout*

The Bit-Map memory stores the profile of an event by writing "1" or "0" if the amplitude on the channels have been bigger or not than the threshold.
Channels status is stored with words of 16 bits, thus one word per 16 channels from D00 to D16.

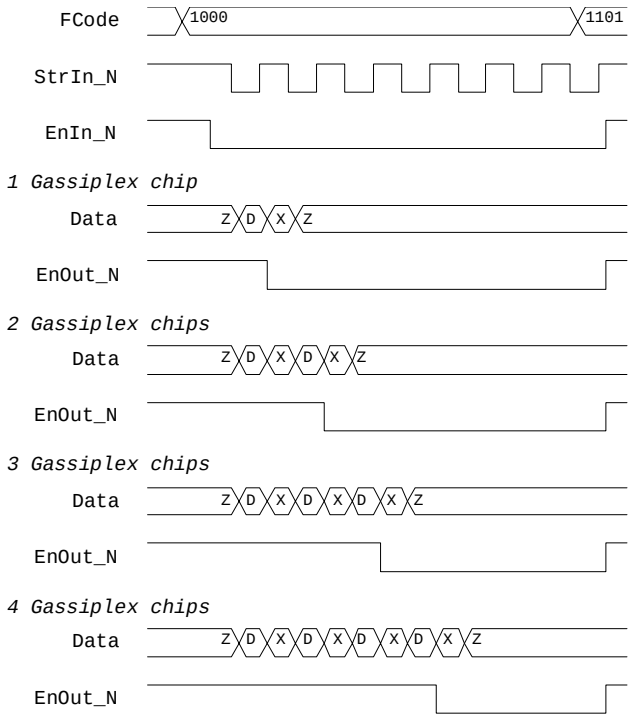

Fig. 6: Pattern readout timing diagram

To perform the pattern readout (Fig. 6), the function code must be set to "1000" and EnIn_N must be low. The patterns will appear on the data bus as long as StrIn_N remains low.
The readout sequence will be the same as the analog readout, it will be finished when the last module drives its EnOut_N pin low. A reset daisy chain has to be applied to turn off the EnOut_N pins.
As in the analog readout mode a pattern delete can be performed.

D. *Configuration write*

The threshold and offset memory can be loaded (Fig. 7) using the function code "1110", EnIn_N set to low and StrIn_N cycles. The data should be stable on the data bus at the rising edge of StrIn_N.
The first 64 cycles of StrIn_N are used to write the first Dilogic, after which it asserts its EnOut_N low and enable the next chip which will take the next 64 cycles to load its data.
A reset daisy chain has to be applied at the end of the operation.

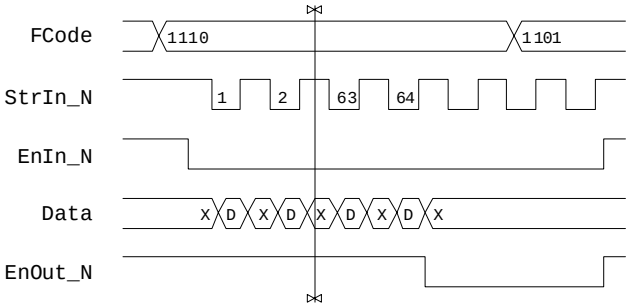

Fig. 7: Config. write timing diagram

E. Configuration read

The threshold and offset memory can be read back (Fig. 8) using the function code "1111", EnIn_N set to low and StrIn_N cycles. The data will appear on the data bus after the falling edge of StrIn_N and will stay stable until the rising edge of StrIn_N. 64 StrIn_N cycles have to be applied to read each Dilogic and the reset of daisy chain has to be applied to end the operation.

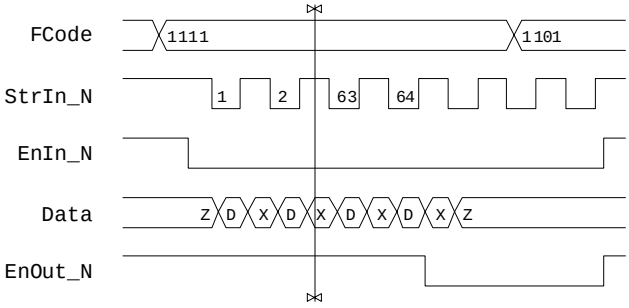

Fig. 8: Config. Read timing diagram

F. Reset fifo pointer

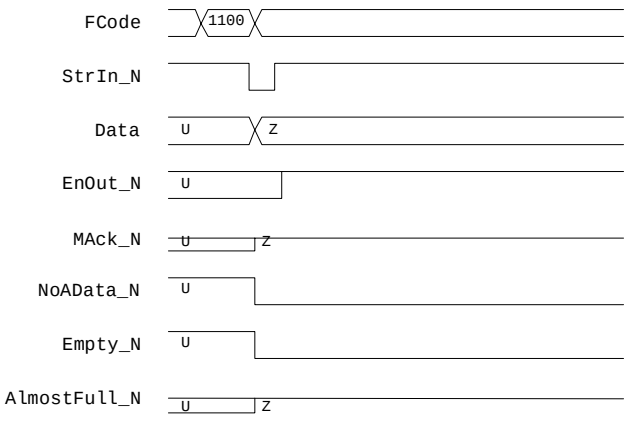

Fig. 9: Reset fifo pointer timing diagram

When function code "1100" is applied (Fig. 9), the address counters in the data fifo and bitmap fifo memories are reset after a StrIn_N cycle is given. The result is a memory clear.

G. Reset daisy chain

By applying "1101" or "0xxx" to Fcode and a StrIn_N cycle, the Dilogic2 will set the state machine that controls the back-end, in the start state (Fig. 10).
It has to be used at the end of the following modes: pattern readout, analog readout, configuration write, configuration read.
The state of the following pins will change: EnOut_N will be set high while Mack_N and the data bus will be put in tri-state.

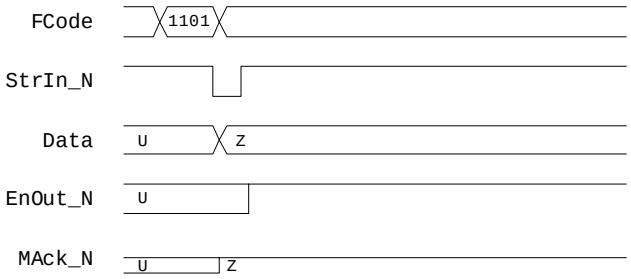

Fig. 10: Reset daisy chain timing diagram

V. CONCLUSIONS

The Dilogic2 has been tested successfully by loading random data on the front-end at a rate of 10MHz. No errors have been detected after performing the sparse data scan operation and readout of the analog memory and the bit-map memory at the same clock cycle.
To simplify the analog front-end electronics by removing the Digital to Amplitude Converters that were supposed to adjust the offset between the Gassiplex, we have been asked to increase the subtraction and threshold field to 9 bits instead of the present 8 bits. The new version will be available in the beginning of 2001.
The Dilogic2 is an upgrade of the Dilogic1 that had been designed to be used with an 8-bits 4 ranges ADC. This first chip had been the implementation in a full ASIC of the sparse data scan part of a CAMAC module, the DRAMS [2].

VI. REFERENCES

[1] J.C. Santiard, K. Marent, The Gassiplex07-2 Integrated front-end analog processor for the HMPID and the Dimuon spectrometer of Alice.
[2] E.Chesi et al., Nucl. Instrum. Methods A283 (1989) 602

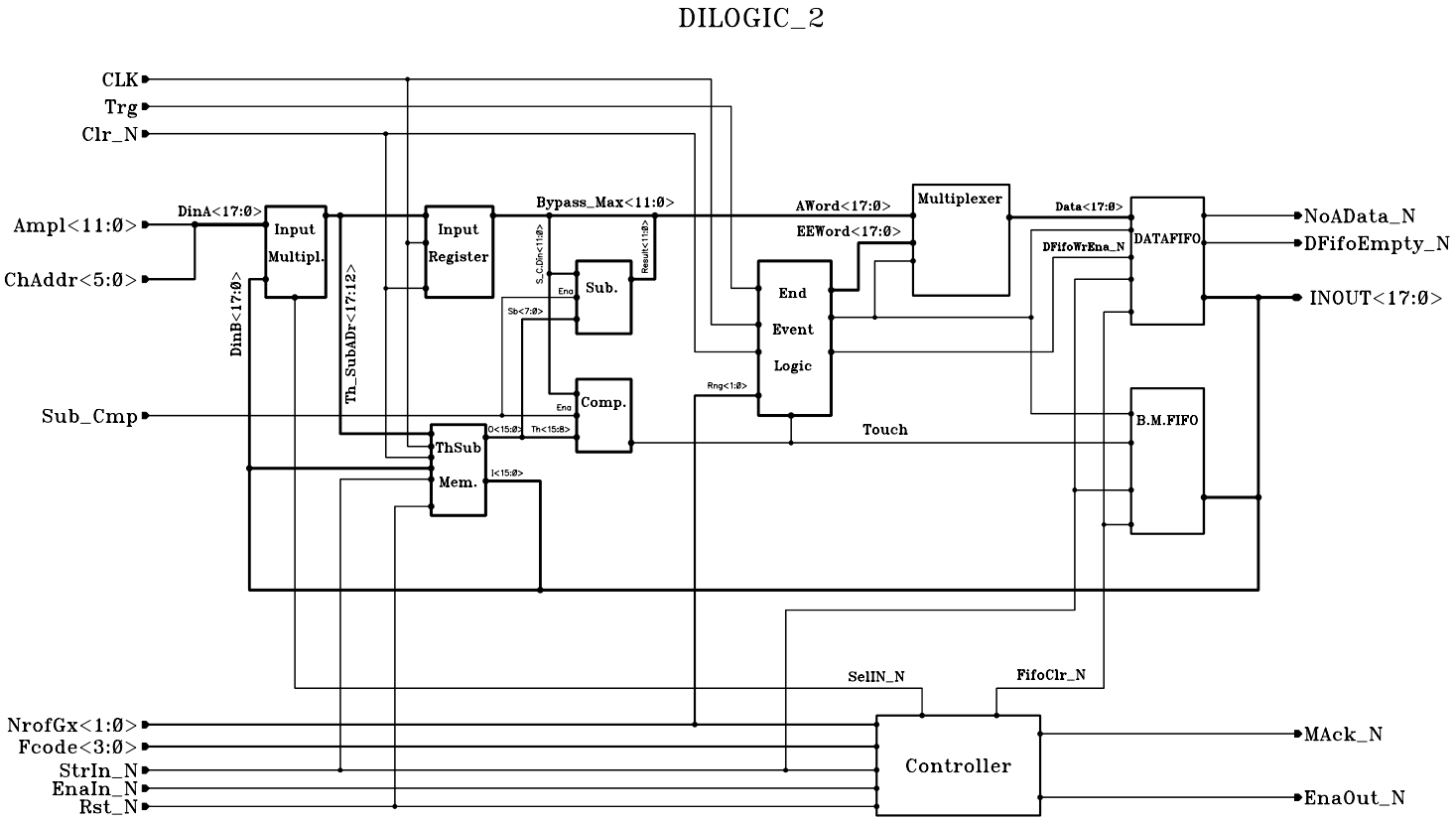

Fig.11:Dilogic2 block diagram