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The ALICE Silicon Pixel Detector (SPD)

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The ALICE silicon pixel detector (SPD) consists of two layers in the barrel region at small radius (4cm and 7cm, respectively). The main requirements are summarised. The design considerations and development status are reviewed.

1. Introduction

ALICE (A Large Ion Collider Experiment) is an experiment optimized for the study of nucleus-nucleus collisions at a centre-of-mass energy of ~ 5.5 TeV per nucleon at the LHC (Large Hadron Collider) [1].
The central part of the experiment, in a 0.2T solenoidal field, consists of the Inner Tracking System (ITS), Time Projection Chamber (TPC) and Transition Radiation Detector (TRD) for electron identification, covering the pseudorapidity interval $-0.9 < \eta < 0.9$. The ITS consists of six layers of silicon detectors. From inside outwards: two layers of Silicon Pixel Detectors (SPD), two layers of Silicon Drift Detectors (SDD) and two layers of Silicon microStrip Detectors (SSD), all in a barrel geometry. A muon spectrometer at forward rapidities will be used to measure muons for the study of quarkonia.
A comprehensive description of the SPD can be found in the ITS technical design report (TDR) [2]. In this paper, we outline the main requirements, some design considerations, and the current status of the SPD project.

2. Main Requirements

The two SPD layers are fundamental in determining the quality of the vertexing capability of ALICE (determination of the position of the primary vertex, measurement of the impact parameter of secondary tracks from the weak decays of strange, charm and beauty particles).

In order to identify tracks from the decay of charm and beauty hadrons, an impact parameter resolution of the order of 50 μm is required. A major technical challenge is presented by the large number of particles created in nucleus-nucleus collisions: up to 8000 charged particles per unit of rapidity around mid-rapidity are expected for the most central Pb-Pb collisions. These constraints determine the requirements on the radial position and on the granularity of the pixel layers [3].

The two SPD layers are located at r = 4 cm and r = 7 cm respectively. Each pixel cell measures 50 μm (rϕ) x 425 μm (z). Such a granularity allows to manage the expected track densities of ~ 90 cm^{-2} for the very central Pb-Pb collisions in the case of the inner SPD layer. From simulation, we obtain a pixel precision in the tracking of 12 μm along the rϕ-axis and 100 μm along the z-axis. The impact parameter resolution is better than 50 μm along the rϕ for pt > 1.3 GeV/c [1,2].

The primary vertex coordinates in the transverse plane (x and y) with respect to the beam axis (z) are determined by the size of the bunches which defines the interaction region with a r.m.s. $\sigma_x = \sigma_y = 15$ μm. Longitudinally, the spread of the interaction region is $\sigma_z = 5.3$ cm. Correlating the hits in the two SPD layers, the location of the primary vertex can be determined with an error $\sigma_z = 15$ μm in the case of Ca-Ca interactions and even better in the case of higher multiplicity Pb-Pb interactions, without

using information from the other central detectors [1].

The ALICE SPD system will be used in different readout configurations, operating simultaneously with four different trigger conditions: minimum bias, central events, central events with dielectron trigger and central events with dimuon trigger. For the latter class of events, the SPD will be the only barrel detector to be read out. In this case, the determination of the primary vertex position, crucial in order to improve the precision on the effective mass of the dimuon topologies reconstructed in the muon arm, will depend solely on the standalone capabilities of the SPD system discussed above.

In the SPD cell, the signal has to be delayed for up to 5.5 μs after the crossing of the particles in order to wait for the arrival of the level 1 strobe. For Pb-Pb collisions at a luminosity of 10^{27} cm^{-2} s^{-1}, the expected rate of the minimum bias interactions is 8kHz. The cumulative rate of the different types of triggers will be of the order of 1 kHz. For Ca-Ca collisions at higher luminosity (10^{29} cm^{-2} s^{-1}) the rate of 300 kHz gives the most stringent requirement on the integration time: the strobe width will have to be limited to a couple of hundreds of ns in order to maintain the event pile-up rate to an acceptable value.

The material budget must be kept very low, since multiple scattering affects the momentum and impact parameter resolution especially with small transverse momentum particles. In case the material is kept within ~1% X_0 for each layer of the SPD, the expected momentum resolution should be better than ~3% for pions with momenta greater than 100 MeV/c and the impact parameter resolution should correspond to the values quoted above [1]. This places challenging constraints on the thickness of the hybrid pixel detector and the amount of additional material in the active volume (electronics, cabling, support structure and cooling).

The radiation levels, integrated over the nominal 10 years running scenario, have been calculated taking into account the anticipated sharing of operation with proton, light (Ca) and heavy (Pb) ion beams, see ref. [2]. According to this scenario, the inner SPD layer will be exposed in ten years to a total dose of ~ 200 krad and to a neutron fluence of approximately $3x10^{11}$ cm^{-2} We estimate that ~60% of the dose level will be absorbed during high luminosity Ca-Ca running. [1,2,5]. These radiation levels require the use of radiation-hardened processes for the front-end electronics. They have little impact on the detectors, which are made of high resistivity silicon. We believe that with such levels of radiation the bulk material should not reach the dangerous inversion point.

3. Design considerations

The SPD consists of two barrels, each subdivided in ten sectors [3] in the rϕ-plane.

Each sector consists of two staves (inner layer) and four staves (outer layer), with a turbine blade-like layout. A 200 μm thick carbon fibre structure holds the staves, the busses, the cooling system and the services. Mechanical prototypes of sectors are shown in Fig.1.

A half-stave (see Fig.2) is made up of two in-line detector ladders. Each ladder is 12.80 mm wide and 70.72 mm long, and is bump bonded to five read-out chips. A chip contains 8192 pixels with a cell size of 50μm (rϕ) x 425μm (z) [6]. The total number of pixel in the SPD is ~ 10^7.

The readout chip is an ASIC in 0.25μm CMOS6 technology on 8" wafers. Bump-bonding these chips with the detector ladders is a challenging task because of the 50 μm size and other issues. The industry standard minimum size for flip-chip technology is currently around 200μm for volume production. Some experience has been gained in the HEP community in bump bonding with the sizes we require, mainly in the construction of the pixel telescope of experiment WA97/NA57 [7], but in our case additional complexity derives from the use of large size 8" wafers. We are working with a few vendors to optimize the technique by trial runs using first low-cost dummy wafers with special test patterns that allow a direct evaluation of the quality of bump bonding.

The 0.25μm CMOS6 process used for the front-end ASIC is a standard one commercially available; good radiation hardness is achieved by design using enclosed transistor layout techniques [8]. The design has been submitted to the foundry and delivery is expected in August 2000. The chip dimensions are 13.60 mm x 15.95mm.

The data flow in each half-stave is supervised by a control chip mounted at the edge of the half-stave (see Fig.3). The chip (designated as Pilot) handles the multiplexing of output data from the readout chips and the downloading of parameters into those chips. The Pilot is designed using the same layout techniques, and in the same CMOS6

process as the readout chip. The design will be submitted to the foundry in January 2001.

The readout and control chips are wire-bonded to a multilayer carrier bus for data, controls and power distribution. The bus for each half-stave (see Fig.4) has six aluminium layers on polyamide support [9]. The outer dimensions of the carrier bus are 16.86 mm x 193 mm x 0.2 mm.

Electrical power is supplied to the front-end electronics using a copper multilayer flex.

The development of the carrier bus and of the power/signal interconnection is a challenging task since the space available is extremely small and the choice of materials is severely restricted by material budget considerations. Design options have been modelled and a prototype is being produced. In Fig.5 a first prototype of the carrier bus is shown.

The readout chip control and parameter downloading is done using the JTAG protocol. Copper cables and optical fibres are both being considered for the clock and control data transmission. The fibre-optic solution has the advantage of a considerable reduction in cable bulk and power dissipation. A decision will be taken after functional tests in the first half of 2001.

The nominal frequency of the readout clock is 10MHz and the SPD is read in 256μs. Signal integrity on the bus is obtained by limiting the rise/fall transitions to not less than ~ 10 ns.

The output data from the Pilot (see Fig.3) enter a serialiser followed by a laser driver, both implemented in the same CMOS6 process as the other ASICs, and are transmitted on optical fibres at 1.2Gb/s speed to the Router module at the back-end.

Each router unit (see Fig.6) receives data from six half-staves. The zero-suppression and hit encoding on the data are done in twenty router VME boards based on programmable devices to guarantee the flexibility. Data transfer is initiated by a positive 2-nd level trigger decision, 100 μs after the event takes place. The introduction in each pixel cell of a front-end buffer of four events [2] allows to use more efficiently the bandwidth and the number of channels of the transmission on optical fibre to the DAQ.

4. Cooling and Material Budget

The study of the cooling system done both by simulations and by prototyping gives as favoured inert coolant the fluorocarbon (C6F14) with pressure >1 bar [10]. This coolant should be able to manage ~ 30-40 W per stave. Less than 5 degree of temperature differences in the coolant circuit are measured on a prototype across a stave (see Fig.7).

A straight track perpendicular to the beam line crossing both pixel layers sees on average 1,7% X_0. This figure takes into account support, cooling, read-out chip, detector and bus. An external mechanical/thermal shield towards the silicon drift detector layer contributes an additional 0.25% X_0.

A major concern is the cabling between the half-staves and the patch-panels on the endcaps at a distance of ~ 1 m. An installation jig is being studied to relieve the possible strain induced on the detector structure by cabling and fluid pipes particularly during the installation phase. The mass of harness attached to each half-stave unit is estimated at 110-140 g. A total mass of 7-8 kg for the services on each side is expected (see Fig.8).

5. Conclusion

The ALICE SPD consists of two layers of silicon pixel detector located at r = 4 cm and at r = 7 cm respectively. The pixel cell size is 50 μm x 425 μm. The SPD is designed to achieve primary and secondary vertex detection even in presence of the high track densities expected.

The front-end electronics consists of several ASICs developed in a commercial 0.25μm CMOS6 process, and radiation hardness is obtained by design using edgeless transistor layout.

The total material budget is calculated to be less than ~ 2% X_0.

Fibreoptic techniques are used for data transmission to reduce the cable bulk on the front ends.

A readout system has been developed and tested with chip emulators.

Further investigations are needed on the bump bonding yield.

References

[1] ALICE Technical Proposal, CERN/LHCC 95-71, LHCC/P3.

[2] ALICE-T.D.R., “Inner Tracking System”, CERN/LHCC 99-12, ALICE TDR 4.

[3] F. Antinori, Nucl. Instr. and Meth. In Phys. Res. A 395 (1997) 404-409.

[4] J. Hubbell et al., ALICE/ITS/INT-2000-10/February 20, 2000.

[5] F. Meddi and M. Morando, Nucl. Instr. and Meth. In Phys. Res. A 395 (1997) 416.

A.Badala’ et al., ALICE/ITS/INT-1999-01/January 9,1999.

[6] W. Snoeys et al., “Pixel readout electronics development for ALICE PIXEL VERTEX and LHCb RICH”, these proceedings (PIXEL 2000, Genova, Italy, June 5th-8th, 2000).

[7] F.Antinori et al., Nucl. Phys. A590 (1995) 139c

V.Manzari et al., J. Phys. G25 (1999) 473

[8] W. Snoeys et al., Proceedings of the Fourth Workshop on Electronics for LHC Experiments (pp.114-118) Rome, September 21-25, 1998

F. Faccio et al., Proceedings of the Fourth Workshop on Electronics for LHC Experiments (pp.105-113) Rome, September 21-25, 1998

[9] M. Morel, CERN-EP/ED, URL http://morel.home.cern.ch/morel/alice.htm

[10] F. Scarlassara et al., ALICE/ITS/INT–2000-18/July 11,2000.

Figure captions

Fig.1 Prototypes of sectors are shown. The cooling fluid distributor for each end-sector and a sector with heating resistors, cooling pipes, thermal and pressure sensors for the cooling efficiency study are shown.

Fig.2 A half-stave unit is sketched. The aluminium multilayer bus will accommodate two pixel ladders, a control chip and link drivers. For the external connection optical fibre and copper flex multilayer bus are envisaged.

Fig.3 Architecture of the pixel system based on read-out chips, pilot chip, optical link and router unit is shown. The trigger signals handshake (L1, L2Y, L2N, and Busy) is also shown.

Fig.4 Vertical sections for two possible pixel bus solutions are shown. One optimises the cooling efficiency (shown on the right part), the other (shown on the left part) optimises the space available for the lines along the bus.

Fig.5 A photo of the first pixel bus prototype is shown. The geometrical details of this prototype are illustrated on the drawing on the side.

Fig.6 The router unit architecture is shown.

Fig.7 The measurements of the temperature increase across the stave in function of the power to be dissipate from each stave, is shown. In the test performed different pipe diameter were used (D). The pipe was flattened to cool more efficiently the stave. The coolant fluid used is fluorocarbon.

Fig.8 The mass breakdown of the cabling for each half-stave is shown.