ASD for the Thin Gap Chambers in the LHC Atlas Experiment

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Abstract

An amplifier-shaper-discriminator (ASD) IC and 16-ch ASD board were designed and built for Thin Gap Chambers in the forward muon trigger system of the LHC Atlas experiment. The ASD IC uses SONY Analog Master Slice bipolar technology. The IC contains 4 channels in a QFP48 package. The gain of its first stage (preamplifier) is approximately 0.8V/pC and the output from the preamplifier is received by a shaper (main-amplifier) with a gain of 7. The baseline restoration circuit is incorporated in the main-amplifier. The threshold voltage for discriminator section is common to the 4 channels and their digital output level is LVDS-compatible. The IC also has an analog output of the preamplifier. The equivalent noise charge at input capacitance of 150 pF is around 7500 electrons. The power dissipation with LDVS outputs (100 Ω load) is 59 mW/ch. Beam tests of the ASD boards were made and showed good performance. The results of the irradiation tests by gamma ray and neutrons proved that the circuits retains the properties required for the TGC readout after 10 years of LHC running.

I. Introduction

The Atlas experiment in the LHC uses Thin Gap Chambers (TGC) [1,2] as its forward muon trigger detectors [3,4]. The total number of TGCs are 3600 and we will be dealing with TGC signals from their anodes (several wires are ganged together) and strips, totaling nearly 330k channels. The capacitance of the TGC as a signal source is a few hundred pF, which comes from the thin gap structure of the chamber and is rather large capacitance when compared with that of an ordinary chamber. The requirement of fast signal processing and the characteristic of large detector capacitance contradict each other when we design a low-noise preamplifier. Much attention was paid to the process choice and circuit design for the TGC application. The ASD as TGC front-end electronics must have a good time resolution for bunch-crossing identification and a high rate capability to cope with high background rate (100 kHz /channel) and must be robust for the longtime operation without maintenance.

II. Circuit Design

Because the signal source has relatively large capacitance and because fast signal shaping as well as low noise are the requirements on the amplifiers, transistors with large g_m are preferred. Hence we chose to base the amplifiers on bipolar transistors [5,6]. The chip has been developed in collaboration with SONY Corporation, using their bipolar 'Analog Master Slice Process'. This semi-custom process provides prefabricated NPN and PNP transistors, resistors and capacitors, so that a designer has to design using these elements that are predetermined beforehand for the silicon wafer. The base-structure we used contains 850 NPN transistors, 3834 PNP transistors, 1738 resistors and 42 capacitors, totaling approximately 1000 usable elements. There are five kinds of NPN transistors on the chip including low noise transistors and power transistors. The standard transistor has f_T = 3.2 GHz. The low noise transistor has f_T = 950 MHz and base-spread resistance $r_{bb'}$ = 17.5 Ω. Availability of the low-noise transistors with very low $r_{bb'}$ was one of the motivation to use the process. There also are two kinds of PNP transistors of which the standard one has f_T = 300 MHz. Capacitors are of 2 pF and 20 pF value totaling 408 pF (Metal Insulator Semiconductor, MIS capacitor) in total. resistors are of either 8 kΩ or 2.5 kΩ (poly-silicon), 297 Ω (diffused) and 129 Ω (diffused).

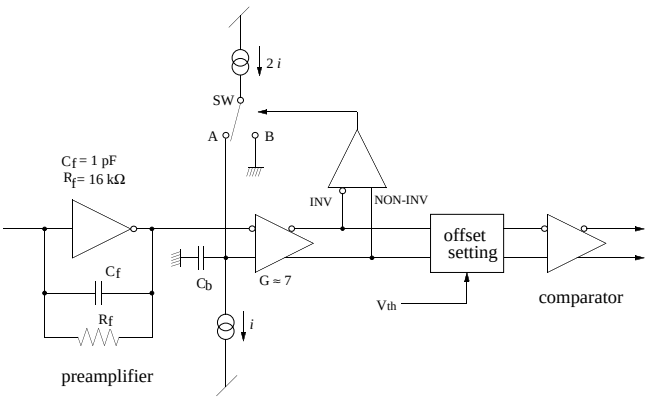

Figure 1 : Block diagram of the ASD chip.

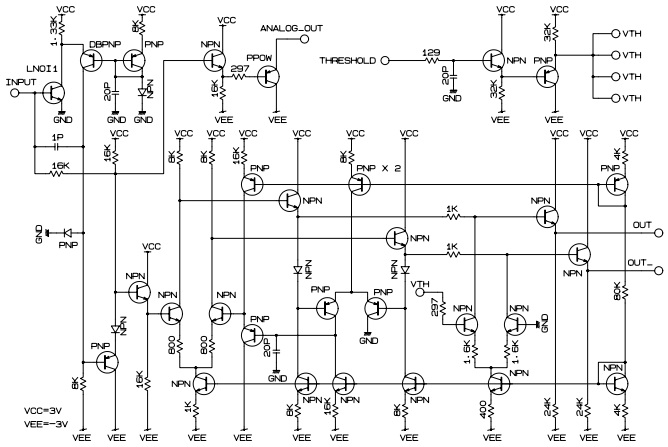

Figure 2 : Preamplifier, baseline restorer and main-amplifier schematics.

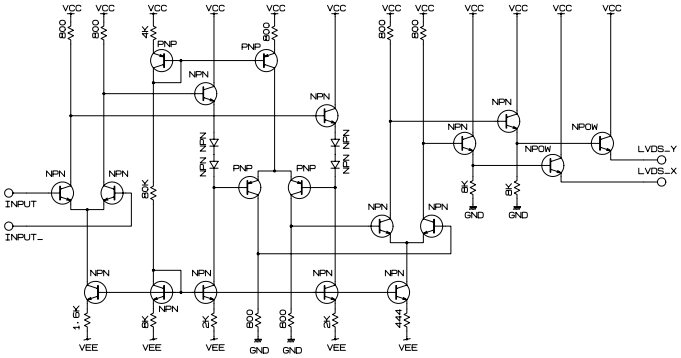

Figure3 : Comparator circuit schematics.

Table 1 : TGC ASD chip characteristics

Process	SONY Analog Master Slice bipolar semi-custom
Specification	preamplifier with a gain of 0.8 V/pC 16 nsec integration time input impedance of around 80 Ω open-emitter analog output main-amplifier with a gain of 7 baseline restoration circuits comparator with LVDS outputs ENC ~ 7500 electrons at C_b = 150 pF 4 channels in a QFP48 plastic package threshold voltage common for all 4 channels required voltage : +/- 3V, GND 59 mW/ch when driving a 100 Ω load (46 mW in ASD chip and 13 mW at LDVS receiver end)

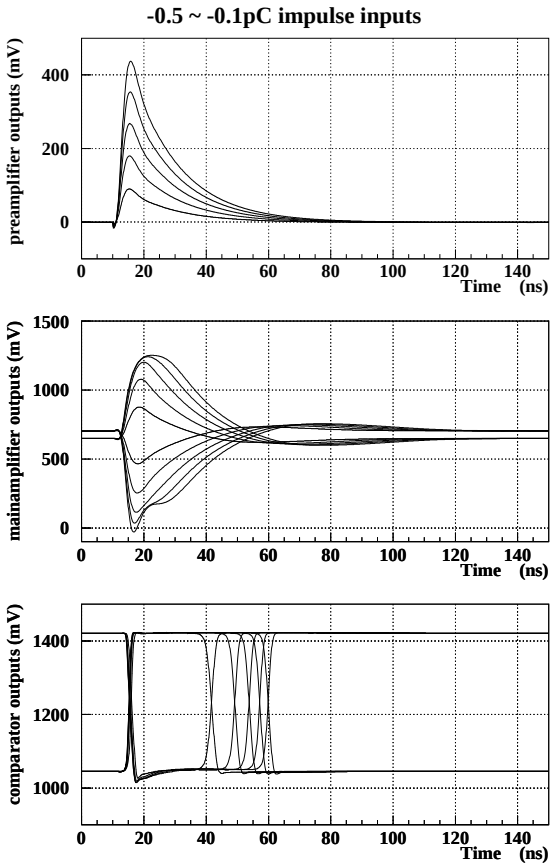

Figure 4: PSPICE simulations of the preamplifier, main-amplifier and comparator outputs.

A block diagram of the ASD chip is shown in Figure 1, with schematics in Figure 2 and 3. Its first stage is a common-emitter cascade charge amplifier. The input stage of the preamplifier is implemented with the low-noise NPN transistor with $r_{bb'}$ of 17.5 Ω. The relatively large capacitance (higher than 10 pF between the collector and substrate) of the transistor disfavors the use of the transistor in common-base configuration which is usually employed in preamplifiers for chambers [7]. The collector current of the head transistor is set high (0.9 mA) to achieve large g_m, which have advantage to achieve lower noise at large detector capacitance. The integration constant is set to 16 ns. The gain of the preamplifier stage is approximately 0.8 V/pC. An emitter follower output of this preamplifier stage is provided for monitoring.

The second stage consists of a main-amplifier with a baseline restorer and differential outputs. The main-amplifier section has a gain of 7. Depending upon the output differential signal level seen by the switch control section, the switch connects to the "A" side or to the "B" side of Figure 1. When the switch is connected to the "A" side, the capacitor C_b will be charged from the current source by the amount of '*i*'. When the switch is connected to the 'B' side,

the capacitor will be discharged by the amount '*i*', resulting in stabilized DC output levels, or a baseline restoration. In other words, the circuit makes the baseline level of the differential outputs from the main-amplifier to be equal.

Following the main-amplifier is an offset setting which transforms the main-amplifier outputs to the levels required at the inputs to the comparator, where offset voltage is controlled by DC voltage (V_{th}) supplied from outside of the chip. The comparator is shown in Figure 3. Its outputs conform to the Low Voltage Differential Signalling standard, LVDS, to assure drivability and immunity against noise and minimizing power.

By design, this circuit can be used for both wire and strip signals by setting an appropriate threshold level. Table 1 is a summary of this chip's characteristics.

Figure 4 shows the result of a PSPICE simulation of the preamplifier output, the main-amplifier differential outputs and the comparator LVDS outputs against impulse inputs of -0.1 ~ -0.5 pC charge. Dynamic range (non-saturated range) of the preamplifier is negative / positive impulse charge input of from -1.2 to +2.0 pC. The slewing rate of the preamplifier also limits the linearity for large positive charge inputs. The dynamic range and the gain of the preamplifier observed at the buffered direct output depends on the external load and is less than the internal one. The circuit can successfully accept signals of 5 MHz or higher frequency.

4 channels of ASDs was fabricated on a 3.1mm X 3.1mm die. The threshold voltage is common to 4 channels. In the layout work of the IC, we paid much attention to reduce interference between analog and digital signals and cross-talk among channels. Both ground and power patterns and I/O pads for the analog part are separated from those for the digital part. The chip is housed in a QFP48 package. For the protection from static charge, diodes are attached between all I/O pads and the most positive / negative voltage excepting those for ground and DC powers.

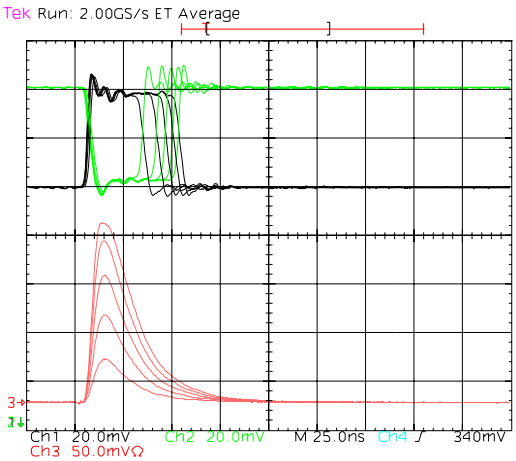

Figure 5 : Analog and digital signals from the ASD for impulse inputs from –0.1 to –0.5 pC.

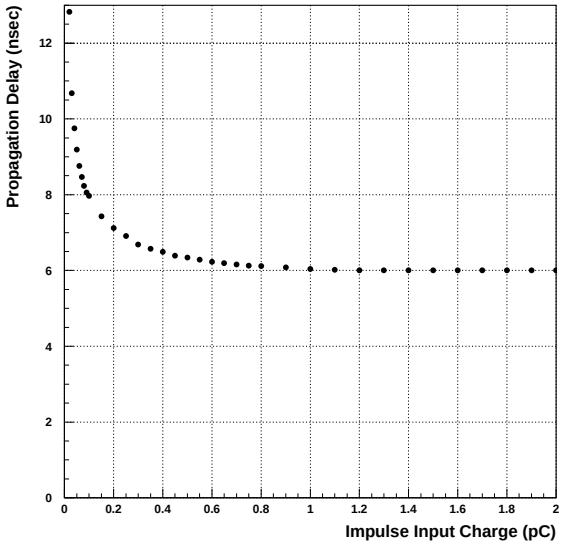

Figure 6 : Overall time walk of the ASD outputs due to the input charge variation.

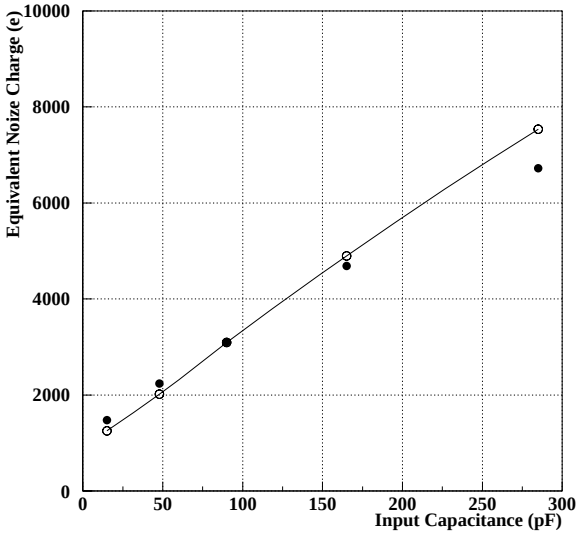

Figure 7 : Measured the ENC (closed circle) and calculated ENC (open circle) using design parameters of the preamplifier and measured impulse response of the evaluation system.

III. PERFORMANCE

The analog and digital signals from the ASD chip for impulse inputs from -0.1 to -0.5 pC are shown in Figure 5. The overall time walk of the comparator outputs due to the input charge variation of between -0.1 pC to -2 pC is less than 2 ns, when the threshold is set at 0.01 pC equivalent, as shown in Figure 6.

We also tested the performance of the main-amplifier and comparator using prototype chips where the preamplifier, the main-amplifier and the comparator were fabricated separately for independent study. In order to check comparator characteristics, we measured propagation delay

while changing conditions such as: varying over-the-threshold-voltage of the input pulse that has fixed rise time / varying over-the-threshold-voltage of the input pulse that has fixed slope / varying rise time while input pulse height was kept constant. The result show that the time walk of the comparator was within less than 2 ns under these conditions. These results agree with predictions by the PSPICE. Temperature dependence of the preamplifier gain was approximately -0.08 %/°C. The feedback capacitor of the preamplifier is supposed to be the major contributor to temperature dependence. The ENC was measured as a function of the input capacitance as shown in Figure 7. We calculated the ENC using design parameters of the preamplifier and measured impulse response of the evaluation system. The calculation reproduces the measured data with the $r_{bb'}$ of 15 Ω and the h_{fe} of 90. Cross-talk among channels were less than 0.5 % when analog output pins are left open. If the open-emitter buffer for the analog output drives 50 Ω load, the cross-talk became 3 times larger. Influence of the digital part on the analog part was much less than the cross-talk between channels.

IV. ASD Board

The 16-ch ASD board was designed for wire signals and strip signals from the TGC. Each board contains 4 ASD ICs with protection circuits and a test pulse circuit that receives a test pulse and distributes a charge impulse to each channel. The board design is common for all TGC chambers. LVDS logic signals from the ASD board are transmitted through a 20-pair twisted-pair cable and a preamplifier output through a LEMO type connector. DC power, ground, threshold voltage (common over a channel) and test pulse are supplied back to the ASD board via the same twisted-pair cable. In order to reduce the production cost, the board was designed as a 2-layer PCB. Devices are surface mounted except for connectors on only one side.

V. Beam Test

We tested TGCs with the ASD ICs at KEK and CERN in 1998. We used pion beams with essentially no background hits at KEK. Whereas at CERN the chamber was tested using muon beams under gamma irradiation. The time jitters and the efficiencies were measured varying the high voltage to the TGC and the gamma irradiation rate. The threshold voltage was set at 5 times of the ENC of the ASD. The time jitters measured are consistent with the ones using hybrid ASD circuits tested before. The rate dependence of the efficiency at applied voltage of 3.0kV is shown in Figure 8. The efficiency is high enough even at five times the predicted background rate (150 Hz/cm^2) at the inner station (the worst place). The ASD boards together with the Module-0 TGC chambers perform as expected in the real ATLAS environment. During the beam tests, we could operate the ASD boards very stably and enough performance was proved.

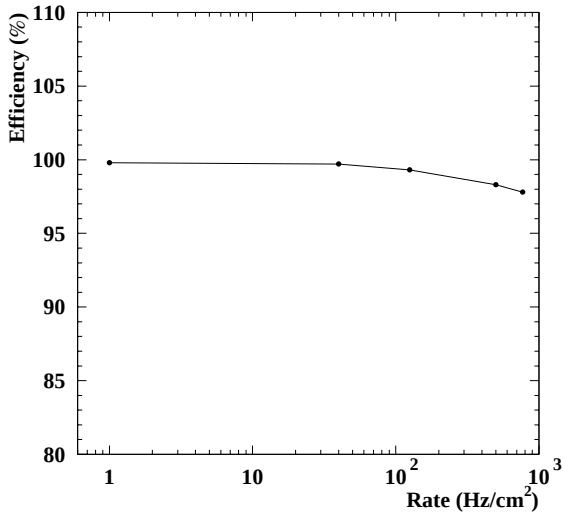

Figure 8 : Efficiency versus background rate for the wire signal.

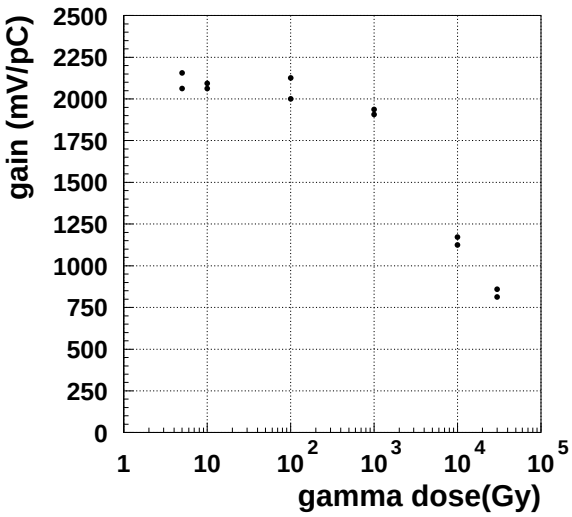

Figure 9 : Gain changes of the ASD chips versus gamma dose.

VI. Irradiation Test

According to the simulation of the expected radiation environment in ATLAS [8], radiation levels at the TGC wheels are an ionization dose of 0.62 Gy/yr and 1.0 x 10^{10} 1MeV equivalent neutron/cm^2/yr. Taking into account the uncertainty in the estimation, a safety factor of four is required [8]. The bipolar transistors, which have a higher sensitivity to radiation damage, require an additional factor of 1.5 for the neutron flux and a factor of five for the ionizing dose. The radiation tolerance criteria at the worst location of the TGC trigger station for 10 years running is an ionization dose of 130 Gy and 1.2 x 10^{12} 1MeV equivalent neutrons/cm^2.

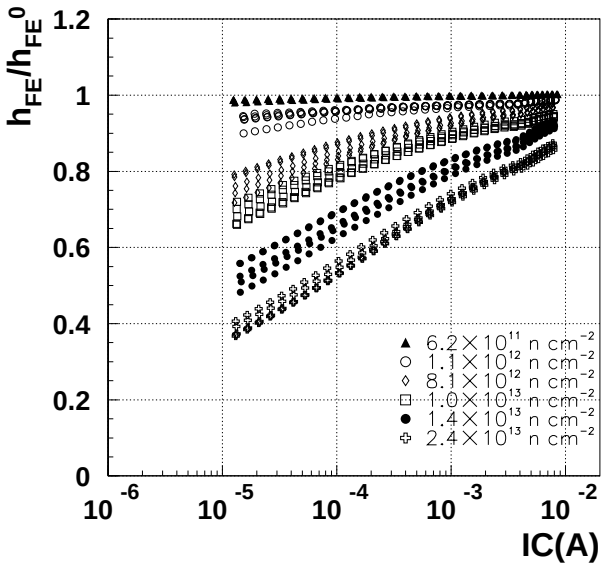

Figure 10 : Normalized h_{FE} values as a function of I_C for NPN transistors for various neutron fluences.

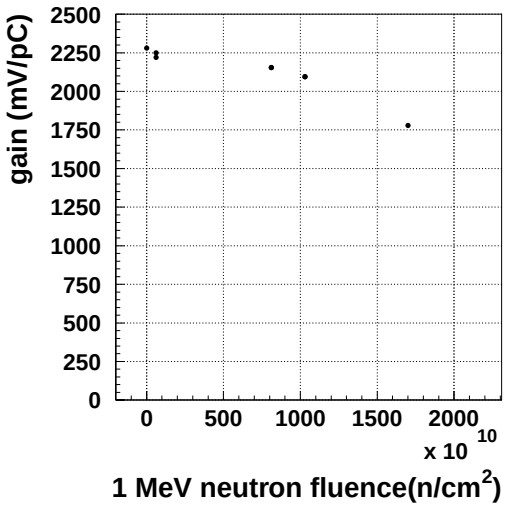

Figure 11 : Gain of the ASD chips versus neutron fluence.

The gamma irradiation tests were performed using ^{60}Co and ^{137}Cs gamma ray sources at the rates of 6.7 kGy/hour and 5 Gy/hour. The h_{FE} parameters of the transistors, and the gain and the ENC of the ASD ICs were measured. The result showed that the degradation in h_{FE} at the dose of 100 Gy is within 10%. The gain change of the preamplifier part of the ASD chip were measured up to the total dose of 30 kGy, as shown in Figure 9. Changes in both the gain and the ENC after 100 Gy irradiation are within the range of the piece-to-piece variation.

The neutron irradiation tests were performed using 12GeV Proton Synchrotron at KEK and the Prospero facility in France. Figure 10 shows the h_{FE} values normalized to the ones before the irradiation as a function of I_C. After the irradiation of $1.1\text{x}10^{12}$ 1MeV equivalent neutrons/cm^2, the decrease of the h_{FE} at the nominal value of I_C was found to be less than 10%. Figure 11 shows the gain difference after the irradiation of $1.2\text{x}10^{12}$ 1MeV equivalent neutrons/cm^2 is within 5%. There was no apparent difference in the ENC up to $1.7\text{x}10^{13}$ 1MeV equivalent neutrons/cm^2.

It was proved that the ASD chips and the components of the ASD board retain the properties required for the TGC readout after 10 years of LHC running even at the location of the worst background condition.

V. Summary

We have designed and built a chip containing 4 channels of ASDs for the TGCs of the Atlas LHC experiment using SONY semi-custom Analog Master Slice bipolar process. We also developed 16-channel ASD boards and performed beam tests with real TGCs at both KEK and CERN. Irradiation test using gamma ray and neutrons were performed and then radiation tolerance of the chip has been assured. The mass-production (100k pieces) of the chips has been done in summer of 1999 and the assembling of the ASD boards (23k) is scheduled in the first quarter of 2000.

VIII. References

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