PRELIMINARY IRRADIATION TESTS OF THE APVD CIRCUIT FOR THE CMS TRACKER

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ABSTRACT

The APVD circuit, developed in the 0.8µ radiation hard SOI DMILL technology [2][3][4] from ATMEL/TEMIC-MHS Nantes, for the front end electronic of the CMS tracker, has been irradiated at CERN using a 10KeV Xray beam up to a total dose of 20Mrad. The main performances of the APVD like gain, pulse shape, noise are presented as a function of the radiation dose. In particular the cause of the DAC non linearity in the bias generator part is discussed.

1. INTRODUCTION

The APVD circuit is a 128 channels CMOS analogue pipeline readout ASIC intended to be used on the CMS tracker. This mixed signal circuit is developed into two derived products, the APVD_AC version (the default version) and the APVD_DC version. Those two circuits mainly differ from the front end part. Whereas the AC version is dedicated to AC coupled Silicon detectors or MSGC detectors , the DC version concerns mainly the DC coupled Silicon detectors.

This DC version circuit contains an additional circuitry intended to compensate for the Silicon detector leakage current.

The level of hardness required on the central tracker sub-detector section makes the DMILL technology [2][3][4] use an inevitable choice.

1.1 APVD Chip Overview

The circuit functionality and architecture is well described in [1] and [5]. We just give there a quick overview.

The circuit consists of a 128 preamplifier-shaper array followed by a 128x160 analogue memory operated at 40MHz. A data access mechanism allows the marking and queuing of requested memory location for output processing. The output processing is made by a switched capaci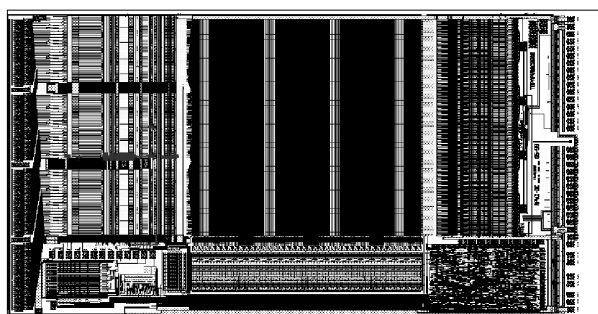tor network which deconvolutes signal off the 50 ns shaping. An output multiplexer ensure the serialisation of the analogue data onto a unique output. Other control functions such as I2C slow control communication interface, programmable bias generator, internal calibration and error checking are also included on this circuit.

> 141 analogue I/O
> 19 digital I/O
> Chip size : 12 x 6.24 mm
> Supplies : +/- 2V
> package : hybrid report

fig 1 : APVD chip overview

2. EXPERIMENT DESCRIPTION

2.1 Irradiation conditions

The irradiation test have been carried out with the 10KeV X ray beam at CERN. The advantages of such equipment for circuit radiation level estimation are numerous [6][7] :

- Dose rates ranging from 10^2 up to 10^5 rad/min
- No residual activation after exposure, due to the low energy level involved.
- Test set up simplicity (the radiation can be located on a region of the PCB)
- Short test duration and low cost

The obvious constraint is the obligation to use non-closed package, in order to have direct access to the top surface of silicon .

A couple of APVD chips, run 04 /98 directly bonded on a PCB have been irradiated under the following conditions :

- Distance between X ray tube and top die : 30 mm
- Dose rate : 15Krad/minute

(High voltage : 40 KV ; current : 28 mA)

2.2 Test Bench Description

The hardware bench is illustrated in fig2a. It is based on a full automated system driven by a PC through LABVIEW.

The APVD mother board is introduced into the X ray machine and is linked to the external world by a set of cables of approximately 4 meters long. The APVD driving capability is limited in the I2C output, and doesn't allow the use of such a cable length. An additional buffer has been introduced on the mother board in order to overcome this problem. This mother board is driven by a SEQSI sequencer, in conjunction with an I2C board (clock, trigger, and slow control). All the measurement instruments are driven by LABVIEW via the GPIB and VXI (MXI-2) buses.
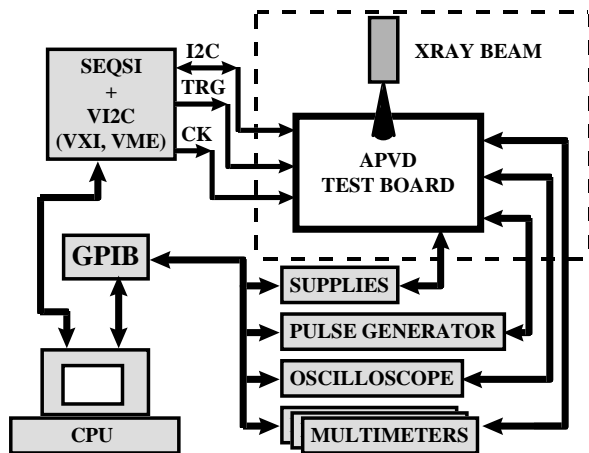

fig 2a : Hardware test set up

2.3 Measurement sequence description

The acquisition for the measurement is shown in fig2b .

The radiation dose rate was set at 15Krad/min. A complete measurement was done each 22 minutes, which gives approximately 330Krad per step. At each step the following measurements were recorded :

- Shape reconstruction under nominal bias settings with external charge injection, in peak mode.
- Noise figures,
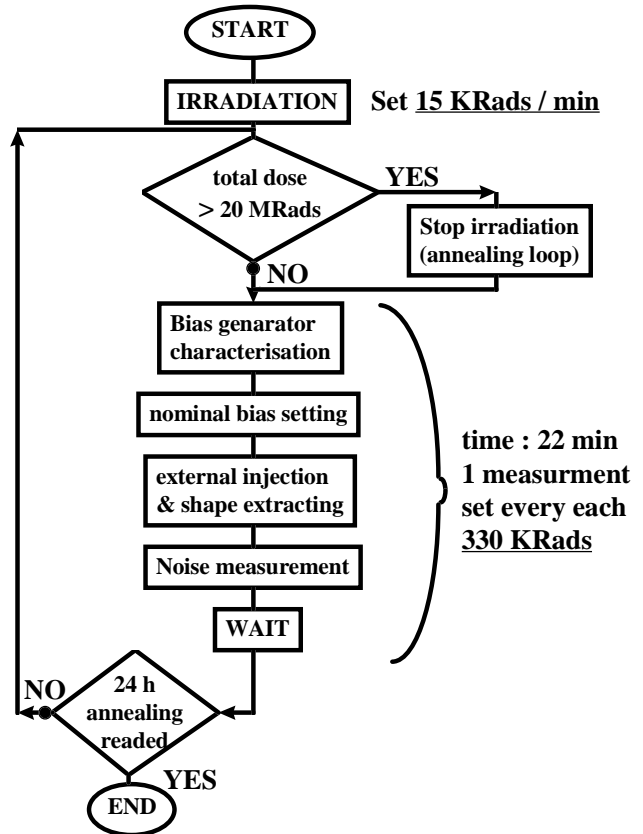- Bias generators DAC transfer function.

fig 2b : measurement acquisition flow chart

3. EXPERIMENTAL RESULTS

3.1 Peak Mode Readout Shape

Fig 3a shows the effect of radiation on the pulse shape in peak mode for a 3Mips input signal. It can be noticed that the peak amplitude decrease slowly with the radiation dose from 88mV at 0rad down to 65mV at 20Mrad. The peaking time increases slightly with radiation dose from 50ns at 0rad up to 59ns at 20Mrad. The shape tail also tends to increase with radiation dose.

The shape distortion is the result of the shift of electrical characteristics on elementary devices mainly transconductance (Gm) and voltage controlled feedback resistors in the preamplifier and in the shaper. During radiation those two characteristics are affected twice - by the mobility reduction effect - and by the bias condition changes . As will be shown in the bias generator current plots, in 3.3, the circuit bias conditions are not intrinsically the same at each measurement step, and cause additional shifts on the OTA operating point.

It is important to note that: although the external bias I2C settings had remained the same during the

irradiation test, the internal biases were not stable, due to the radiation effect on the bias generator function itself.
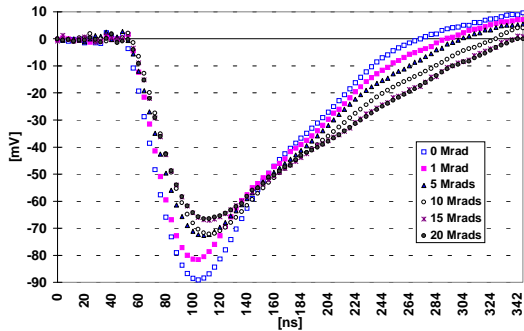

fig 3a : pulse shape reconstruction for a 3MIPs input signal

RADIATION DOSE [Mrads]	0	1	5	10	15	20
PEAKING TIME [ns]	50	51	54	56	58	59
AMPLITUDE 3 Mips [mV]	88	82	74	73	66	65

table 3a : pulse shape characteristics

In the real application, this will be possible to compensate for the radiation effect on the bias generator and, up to a certain extend, for the radiation effects on the pulse shape. This is the role of the slow control functions.

3.2 Noise Figures

Noise Measurement Method

At each radiation step the baseline noise for all channels is recorded with no input signal applied to any of the channel for 500 consecutive triggers. Then the pedestal noise of a peculiar channel is measured taking 50 samples over 25ns. From the pedestal noise voltage the common baseline noise is substracted to give the inherent RMS noise of the channel. The noise in ENC electrons is then calculated from the extracted channel gain which is itself calculated at each radiation step with a known pulse injection.

Noise Measurement Results and Comments

The simple estimation of the noise performance degradation under irradiation is not easy to achieve. On one side an 1/f noise spectral density increase is expected, and on the other side the Gm of the preamplifier input device should decrease whereas the time constant τ of the CR-RC shaping should increase.

In fact, the variation of τ is small compared to the gm degradation, so the 1/gm coefficient should dominate in the ENC formula :

$$\left(ENC \right)^2 = \frac{e^2 \, C_{sensor}{}^2 \, K \, T}{3 \, gm \, \tau}$$

The ENC versus radiation dose curve is plotted on fig 3b. It corresponds to the ENC in peak mode with a 1pF input capacitor. A quasi linear increase of the noise can be noticed in the range 0-20Mrad with a slope of around 32 rms electrons per Mrad.

As mentioned before, those measurements have been done without bias correction during radiation which is, in fact a worst case estimation.
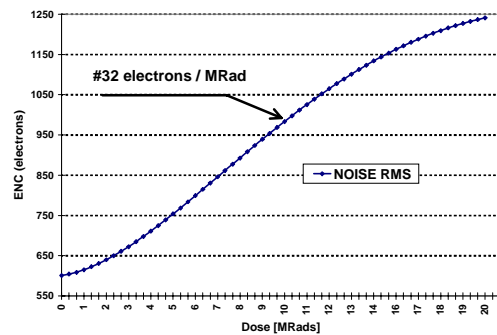

fig 3b : noise measurement in peak mode

It is interesting to note on fig 3c that after 24hours of recovering at ambient temperature the ENC falls to around 800 electrons.
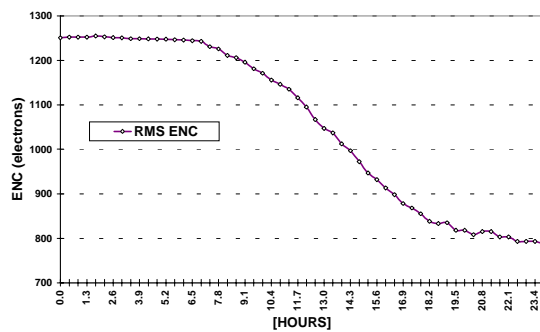

fig 3c : noise measurement during 24 hours annealing

3.3 Bias Generator

Two bias generator channels of the 11 used in the AVPD chip have been characterised these are the IPRE current channel and the VPRE voltage channel. These generator outputs are reachable via special test pads. Thanks to the I2C slow control it is possible to register

the digital to analogue transfer function of the bias generator internal DAC.

It is important to keep in mind the measurement acquisition flow chart (fig2b) for further understanding on the radiation effect on the current DAC. That is a fixed digital value was loaded into the data register during most of the radiation exposure duration. The data register was scanned over the full range only during the DAC transfer function acquisition whose duration is negligible compared to the duration of the rest of the loop. Two different values were set into the IPRE data register and the VPRE data register, the values which produce the optimal shaper output wave form at 0rad:

- IPRE data = 55 → IPRE = 230µA
- VPRE data = 255 → VPRE = -0.7V

3.3.1 IPRE DAC channel

The IPRE DAC transfer function is plotted on fig 3d. This plot reveals two important things; the existence of steps on certain digital code positions and a continuous step height increase with radiation dose.
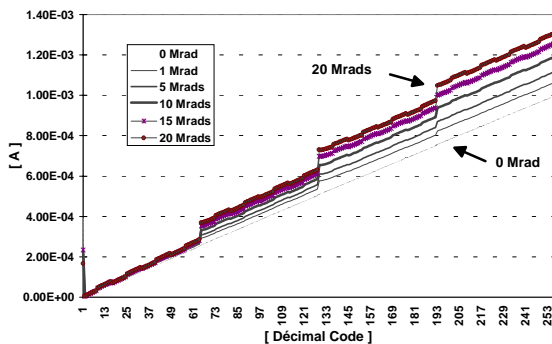

fig 3d : IPRE DAC transfer function

These phenomenon are clearly understood and are the result of different threshold voltage (Vt) shifts on the elementary devices which compose the DAC. This lack of robustness can be corrected by a small design change and is further discussed in chapter 4.

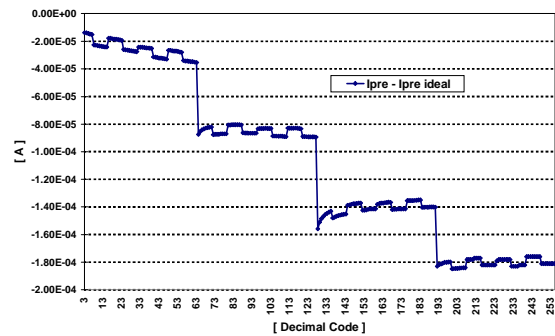The IPRE DAC channel non-linearity at 10 Mrad is plotted on fig3e.

fig 3e : IPRE DAC non-linearity @10Mrad

3.3.2 Is non-Linearity a Real Problem for the Application ?

During LHC operation it will be possible to tune the circuit bias in order to optimise the readout shape and to reach the highest possible S/N ratio. The biases programmable capability is the key element for this tuning. A moderate resolution DAC architecture can fully match this tuning requirement. That's why the DAC used in the bias generator function are designed with economical means.

Anyway, the differential non linearity must however be kept in a reasonable range (ie, 2 to 3 LSB at maximum). As can be seen on fig 3e, the apparent step of #60µA at the digital values 64, 128, 194..., corresponds to around 15LSB. That is, in those regions, the DAC resolution is 15LSB which is more than the allowed non-linearity range.

In the next APVD run, the DAC design will be modified in order to reach the non-linearity limit of 2 LSB.

3.3.3 VPRE DAC channel

The voltage DACs is made of the same current mode DAC bloc that composes the current DAC. For the voltage to current conversion P+ resistors are used via sink or source current mirroring depending on the voltage polarity required.

Thus one could expect that the bias generator voltage should reveal under irradiation the DAC current imperfections and in addition the P+ resistor variation. In fact this last term is small (<5%) thanks to the high doping level of this resistor .

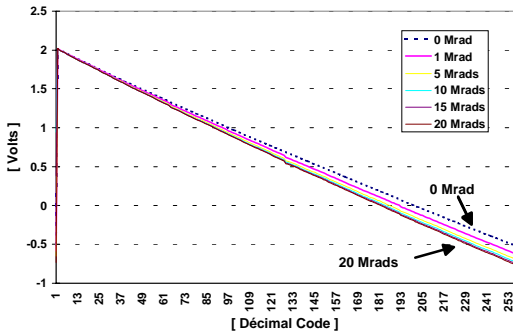The VPRE voltage transfer function is plotted in fig3f.

fig 3f : VPRE DAC transfer function

We can notice an obvious transfer function slope variation with radiation dose, but curiously, the non linearity and the curve steps differ completely from the IPRE DAC current counter part. That is, the VPRE voltage DAC seems to be far more robust to radiation than the IPRE DAC. This result is in fact deceitful because the voltage DAC was into a peculiar state during radiation exposure (VPRE data register set at the value 255).

The data register initial setting is responsible for this difference in the DAC behaviour. Let's consider the key elements :
- In the VPRE DAC, the data register was full range (data=255) in this case all the elementary transistors that compose this DAC were in the same ON state, and thus have exhibited matched Vt shifts.
- In the IPRE DAC, the data register was somewhere between zero and full range (data=55), in that case, some devices were ON while others were OFF, and thus the ON transistors and the OFF transistors have exhibited different Vt shifts.

Concerning the transfer function slope change, it has two origins :
- Small P+ resistor value variation with radiation dose
- Layout configuration ; the master chip reference current function is situated far away from the front end and from the DAC arrays. The X ray beam was rather centred on the front end part, and this reference current function has been probably irradiated differently than the front end part due to non homogeneity effect on the beam itself .

4. DESIGN ASPECTS

This chapter describes the present current DAC architecture, the cause of degradation under irradiation, and the design modifications implemented in the next version.

4.1 Current DAC architecture

The basic principle of conversion is illustrated on fig 4a. The DAC comprises a eight bit digital data register and eight weighted current generators. Each current generator delivers a known current, which is a multiple ratio of the reference current Iref. This built-in current ratio depends on the current mirror weight. Each current generator are individually switched ON or OFF by the data register corresponding bit.

The output current expression can be written as:

$$I_{OUT} = I_{REF}\left(128 \times b_7\right)\left(64 \times b_6\right)\left(32 \times b_5\right)\left(16 \times b_4\right)\ldots$$
$$\ldots\left(8 \times b_3\right)\left(4 \times b_2\right)\left(2 \times b_1\right)\left(1 \times b_0\right)$$
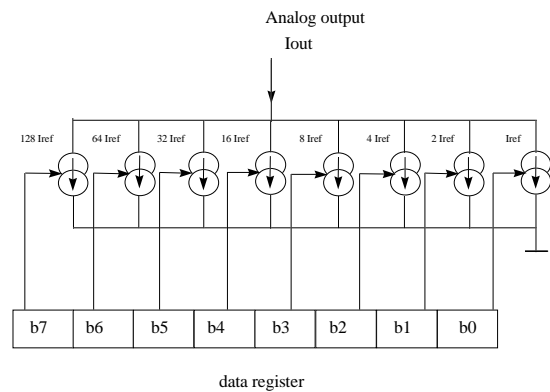

fig 4a : Basic DAC architecture

The practical realisation of the DAC is shown on fig 4b.

The operation principle is straightforward. Transistor M1 is the reference transistor for all the current mirrors, it is drain to source connected. The recopy part of each current mirror is built with the same transistor (identical to M1), duplicated as many times as necessary to get the required current ratio. These slave mirrors are switched by analogue multiplexers driven themselves by the data register. The analogue multiplexer switches the gate of the concerned slave mirror to that of M1 when its current raw is asked to be ON ; or switches it to ground potential when it is asked to be OFF.

4.1.1 Why is this Architecture not Rad Hard Enough ?

The effect of the radiation on the MOS devices is an ageing effect which is to modify their threshold voltage Vt. This is mainly due to the mechanisms of trapping charges in the gate oxide and is directly connected to the quality and the thickness of the oxide. Moreover, the charge trapping mechanism in the gate oxide is also

dependent on the biasing conditions. That is to say that two identical MOS devices biased at two different gate to source voltage do not exhibit the same Vt shift after radiation exposure.
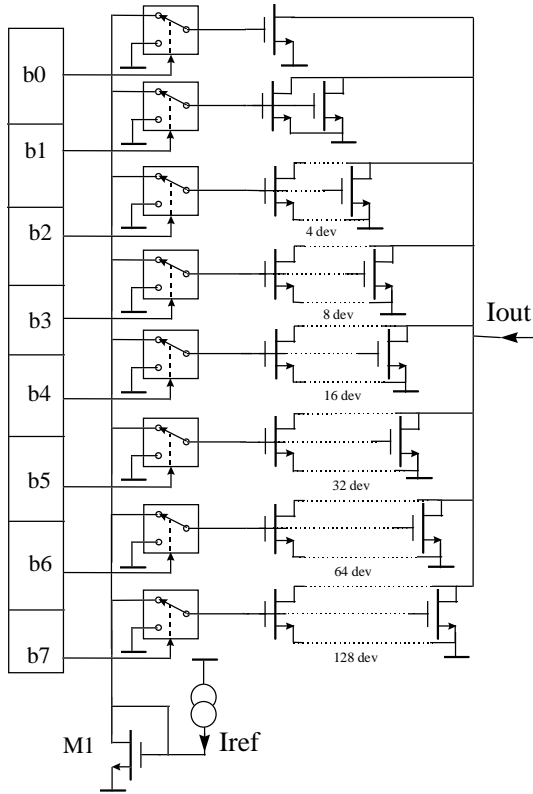

fig 4b :present DAC practical realisation

That's exactly what happens in the DAC shown on fig4b. In the case where the data register takes the value $00 or $FF, all the transistors which compose the current mirrors are in the same bias condition. In contrast, for all other data register values, some devices are ON whereas others are OFF. It results that if the DAC is exposed to radiation in this last condition (data register somewhere between $00 and $FF) that damages the matching between the different current mirror raw. This mismatching effects cause non linearity and produce steps on the DAC transfer function This is clearly illustrated on fig 3d and 3f. The IPRE channel DAC transfer function, with a data register set at $37 during radiation exposure, exhibits steps. In contrast, the VPRE channel DAC, with a data register set at $FF during radiation exposure, reveals no steps.

4.2 New proposed structure

In order to overcome the radiation damage on the DAC, we propose the following design modifications, fig 4c.

In this new scheme, the gate to source voltage remains identical on all the elementary devices whatever the data register value is. The current source raw selection is now done by switching the drain of the devices. When a current source is called to be ON, it is switched to the output node, and when it is asked to be OFF its output drain remains open.
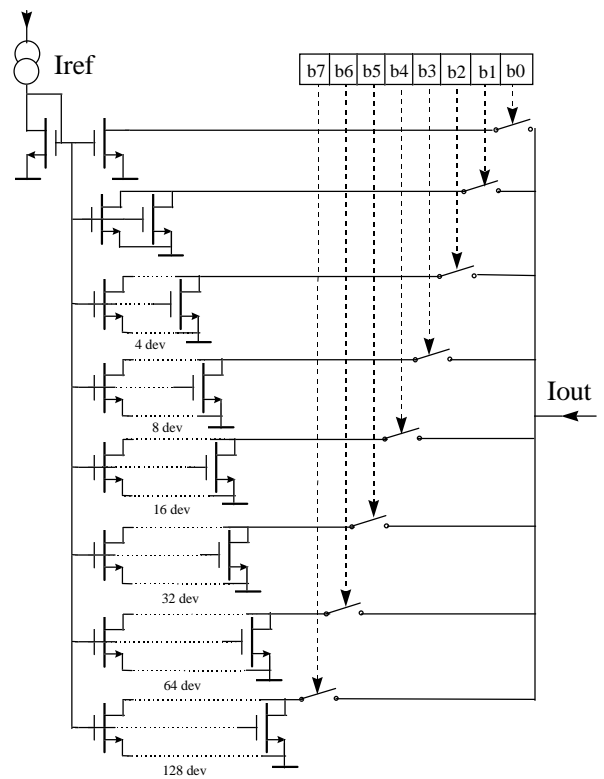

fig 4c : New DAC realisation proposed

The switches in the different current mirror outputs have finite ON resistance and, at high current, can cause DC errors in the digital to analogue transfer function, by the so-called Early effect. So, all switches are not designed with the same geometry. The switch size is adapted to the output current scale in order to produce the same voltage drop on each current mirror output.

4.2.1 Residual non Linearity Effects

Very little steps can, nevertheless, be observed on the DAC transfer function before radiation exposure. This residual effects are due to the mirrors array layout themselves :

- The different current mirrors are basically of different size and are not all closed to the master current source reference transistor.
- It has not been possible, for layout constraints, to draw each mirror with dummy devices.

5. CONCLUSIONS

These preliminary radiation test results on the APVD_AC version are encouraging. The circuit is still fully functional after 20Mrad. This confirms the hardness of both DMILL technology and the APVD design.

Some design weaknesses have been pointed out and corrections have been implemented in the new APVD version, now under foundry processing.

A more complete radiation hardness characterisation will be needed on the final product in order to guaranty the product quality for the LHC.

AKNOWLEDGEMENTS

REFERENCES

[1] R.Turchetta et al, « APVD :a CMOS Mixed analogue digital circuit for the silicon tracker in CMS » Proceedings of the 3rd Workshop on Electronics for LHC Experiments, London, September 22-26 1997, pp. 163-167.

[2] M.Dentan et al, « DMILL, a mixed analogue-digital radiation hard technology for high energy physics electronics ». CERN/LERB/97-15/Projet RD29 ststus report, March 1997.

[3] M.Dentan et al, « Results of the industrial transfer of DMILL, a rad hard mixed analogue-digital technology for high energy physics applications » . Proceedings of the 3rd Workshop on Electronics for LHC Experiments, London, September 22-26 1997, pp. 134-138.

[4] M.Dentan et al, « Final acceptance of the DMILL technology stabilised at TEMIC/MHS ». Proceedings of the 4th Workshop on Electronics for LHC Experiments, Rome, September 21-25 1998, pp. 79-85.

[5] C.Hu et all, « APVD_AC a 128 channels analogue readout chip for DC coupled silicon detector of the CMS tracker ». Proceedings of the 5th Workshop on Electronics for LHC Experiments, Snowmass, September 20-24 1999.

[6] O.Flament, « The use of X ray source for hardness study, control and optimisation of process for microelectronic devices ». L'onde electrique mai-juin 95 vol 75 n°3.

[7] F.Faccio, « Etude des transistors MOS avances sur technologie SOI : bruit, degradation en environnement radiatif et application ». Thesis report nov 97.