LARGE-SYSTEM EXPERIENCE WITH THE ASD-8 CHIP IN THE HERA-B EXPERIMENT

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Abstract

The amplifier-shaper-discriminator chip ASD-8, developed by the University of Pennsylvania for drift chamber applications in high rate environments, is used in large detector systems in the HERA-B experiment. We report on the results of tests performed on some 25 000 chips and on the design and tests of the PC-boards. The so far largest system employing ASD-8 chips is the HERA-B Outer Tracker with about 120 000 drift chamber channels. We present first experience with the grounding scheme, noise suppression and the slow control system as well as first measurements with the full readout chain in the HERA-B experiment.

1. INTRODUCTION

HERA-B is a fixed target experiment for studying CP violation in B-meson systems using an internal wire target in the proton beam of HERA [1]. To reach the necessary production rate of b quarks an average of 4 interactions per bunch at a frequency of about 10 MHz (96 ns bunch separation) has to be generated. This leads to a high particle density with a radial distribution of the particle flux (R is the distance from the beam):

$$\phi \approx \frac{10^{14} \ldots 10^{15}}{R^2 \cdot \text{year}}$$

The main detector components are a silicon vertex detector, a magnet (2.2 Tm), a main tracker with MSGCs in the inner and drift tubes in the outer part, 'High-P_T' Chambers, a RICH, an electro-magnetic calorimeter and a muon detector with drift tubes. The detector covers a forward angular range of 220 mrad in the bending plane of the magnet and 160 mrad vertically.

The amplifier-shaper-discriminator chip ASD-8 [2], developed by the University of Pennsylvania for drift chamber applications in a high rate environment, is used in different detector systems of the HERA-B experiment (Outer Tracker, RICH, Muon System, High-P_T Chambers) with a total of about 200 000 channels.

In the following we refer mainly to the Outer Tracker which is with about 120000 channels the largest ASD-8 application in HERA-B.

2. THE OUTER TRACKER SYSTEM

The Outer Tracker of HERA-B [1] consists of 13 planar superlayers of drift tube modules. The detector acceptance starts at a radial distance of 19 cm to the beam. Together with the Inner Tracker it allows a precise momentum measurement and provides fast track recognition on the first trigger level.

The drift tubes are folded from gold-coated polycarbonate foil with an hexagonal cross section (honeycomb tubes). The inner diameter of the cells is 5 mm in the most exposed sections and 10 mm further outside. As drift gas $Ar/CF_4/CO_2$ (65/30/5) is chosen. Operating at a gain of about $4 \cdot 10^4$ the drift velocity is about 100 μm/ns which allows the track signals to be collected within the bunch crossing time of 96 ns.

The particle densities and radiation levels in the Outer Tracker are comparable to those in similar detectors for LHC. In the hottest area the particle flux is about $2 \cdot 10^3\,\text{mm}^{-2}s^{-1}$. The drift tubes are longitudinally subdivided to limit the single channel occupancy to about 20% (the shortest segmentation near the beam is 20 cm). Because of the planar detector geometry the front-end amplifiers can be placed away from the beam pipe yielding a radiation load below about 50 Gy per year at the location of the ASD-8 boards.

Pattern recognition in a dense particle environment and a precise momentum measurement require a position resolution of about 200 μm. The corresponding good time resolution can be achieved by triggering on the first electron cluster arriving at the anode. At a gain of $4 \cdot 10^4$ a cluster results in about 1.5 fC after fast shaping. Such a low threshold requires low noise and low crosstalk in the system. The first level trigger requires a high hit efficiency and a fast signal collection within the bunch separation of 96 ns.

In order to fulfil the requirements on tracking and triggering in a large system of about 120 000 channels the tracker front-end electronics should have the following characteristics:

- High integration density at low power consumption;
- low per-channel costs;
- fast signal shaping and precise timing;
- low noise: threshold sensitivity of about 2 fC;

Table 1. Performance figures of the ASD-8 chip

integration density	8 ch. on $2.7 \times 4.3\,\mathrm{mm}^2$ die
power consumption	0.3 W / chip (incl. output)
cost	about 4 DM / channel
signal shaping time	about 10 ns
tail cancellation	$t_0 \approx 1.5\,\mathrm{ns}$
double pulse resol.	25 ns
intrinsic noise	(900 + 70/pF) electrons
on-chip crosstalk	analog: $\sim 0.1\%$
threshold	$\sim 2\,\mathrm{fC}$
baseline shift	0.5 - 1.0 fC/MHz

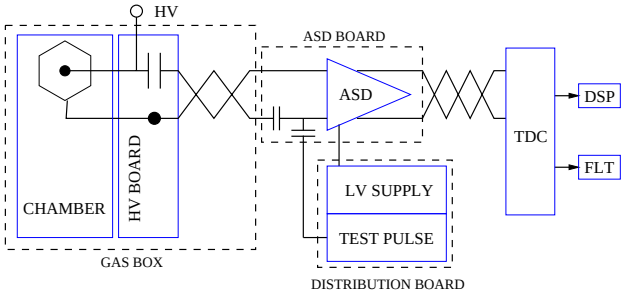

Figure 1. The front-end electronics of the Outer Tracker.

- low crosstalk, required dynamic range: total charge / threshold charge = 40;
- small rate dependence of the threshold up to about 2 MHz;
- radiation hardness up to a level of about 1 kGy.

These requirements were found to be met by the ASD-8 chip as shown by the actually achieved performance figures listed in table 1.

3. THE OUTER TRACKER FRONT-END ELECTRONICS

For the Outer Tracker drift tubes the anode wires are on high voltage and the cathode foils on ground. The anode signals are AC coupled to the amplifier via coupling capacitors which are placed inside the gas volume (discharge protection). For better accessibility the ASD-8 board is mounted outside the gas box.

The whole readout chain of the Outer Tracker (Fig. 1) consists of an HV board with coupling capacitors for the chamber signals, a connecting twisted pair cable, a feed-through board to transfer the signal through the wall of the gas box, the ASD-8 board, a twisted pair cable and TDCs. The TDCs are read out by digital signal processors. In addition the hit information of 4 selected superlayers (trigger layers) are transferred to trigger link boards.

FEE Components:

HV board: The HV boards are printed circuit boards connecting the chamber wires to the high voltage and to the pre-amplifiers. The anode signals are AC coupled to the amplifier via 330 pF capacitors. The boards are located inside the gas volume.

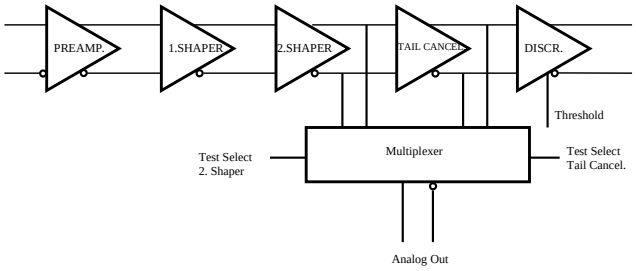

Figure 2. Principal functions of the ASD-8 chip.

Feed-through board: The signal cables (twisted pair, length 25 or 50 cm) from the HV boards are plugged from the inside of the gas-box to the feed-through boards. On their outside the feed-through boards hold the ASD-8.

ASD-8 board: On the ASD-8 board the drift chamber signals are transformed to a digital output which is transmitted via shielded twisted pair cables to the TDC's. The board is described in detail below.

Time-to-digital converter: The customized 8-channel TDC chip digitizes the time in 0.5 ns bins with an 8 bit output. Each TDC channel has a GTL receiver on chip. The differential, open collector output of the ASD-8 is terminated at the receiver side (see sect. 5).

The crates housing the TDC boards are mounted on the cable frame of the detector superlayers. The maximal cable length between the ASD-8 boards and the TDC crates is 5 to 10 m.

ASD-8 power distribution board: These boards serve three purposes: distribution of the +/- 3V power, slow control of thresholds, currents, voltages and switching of the test pulser.

A distribution board supplies 6 groups with 8 ASD-8 boards each. The threshold is the same for all ASD-8 boards in a group and can be selected out of two threshold values provided on the distribution board. Tests pulses can be sent to selected groups.

The boards are controlled by a SLIO processor and are connected to the slow control system via CAN bus.

4. THE ASD-8 CHIP

4.1. Technical Data

The amplifier-shaper-discriminator chip ASD-8 [2] (fig. 2) has been developed by the University of Pennsylvania for drift chamber applications under high radiation (specifically for SSC). The 8-channel chip is designed in a bipolar process which combines high speed with a low noise level and low power consumption.

Amplifier: The ASD-8 input is a preamplifier with a sensitivity of 2.5 mV/fC, a bandwidth of 100 MHz and an input impedance of 115 Ω. The input is differential

Table 2. Technical data of the ASD-8 board

channels	16 (2 chips)
dimensions	4 layers, 67 × 56 mm^2
pickup suppression	all supply voltages RC filtered
spark protection	diode protection $\geq$3 kV
cross talk (analog)	$< 0.5\%$
gain uniformity	$\pm 15\%$ per board
output	2 mA into 62 Ω
voltage supply	+3 V, 100 mA
	−3 V, 100 mA
power	600 mW

and symmetric for positive and negative pulses.

Shaper: The two-stage shaper with tail cancellation yields a double pulse resolution of 25 ns. The tail cancellation compensates the ion tail of the drift chamber pulses. Analog outputs are provided for 3 channels per chip, selectable after the 2nd shaper or after the tail cancellation. The output pulse is proportional to the input signal up to about 50 fC (20 mV/fC).

Discriminator: The discriminator is a two-stage differential amplifier with positive feedback. The threshold is voltage programmable for each channel (with 250 mV / fC, maximal about 1.4 V). The differential, open collector output is current programmable to adjust the swing.

4.2. Series chip tests and selection

HERA-B ordered a total of 90 wafers, each with about 335 chips. The yield per wafer was on average 77%. Each chip was tested according to a scheme which evaluated the general functioning, the threshold behaviour and the noise level.

For each channel the threshold U_{eff} to record a standard 4 fC test pulse with 50% efficiency was determined. The noise behaviour of a chip was characterized by the threshold U_{noise} for which the noise rate exceeded 2 kHz. The difference $U_{eff} - U_{noise}$ is a measure for the signal-to-noise distance and thus of the quality of a channel.

The chip tests revealed an appreciable range for the U_{eff} threshold from about 900 to 1400 mV (fig. 3). With this variation it is not possible to define a common threshold for the whole system if a homogeneous sensitivity to the first arriving electron cluster should be obtained. On the other hand, to keep the front-end electronics simple and compact, individual threshold settings for each channel should be avoided. Therefore 4 categories of threshold ranges were defined:

$$U_{eff} = 860...950,\ 960...1050,\ 1060...1150,\ > 1150\,\mathrm{mV}.$$

To account for the signal-to-noise variation for a given U_{eff} (fig. 3) in each of the 4 gain categories, 3 noise categories corresponding to noise distances had to be defined:

$$\overline{U_{eff}} - U_{noise} = \geq 550,\ 500 \pm 50,\ 400 \pm 50\,\mathrm{mV},$$

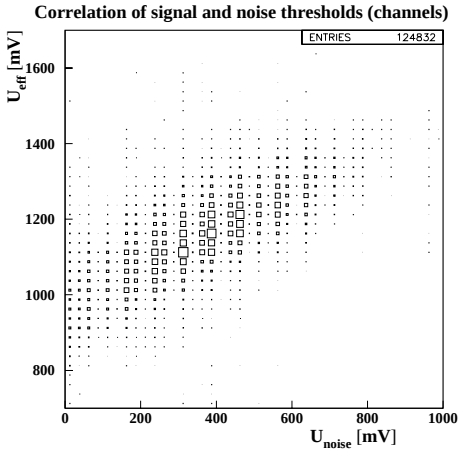

Figure 3. Threshold U_{eff} plotted against the noise threshold U_{noise} for each channel of the tested chips.

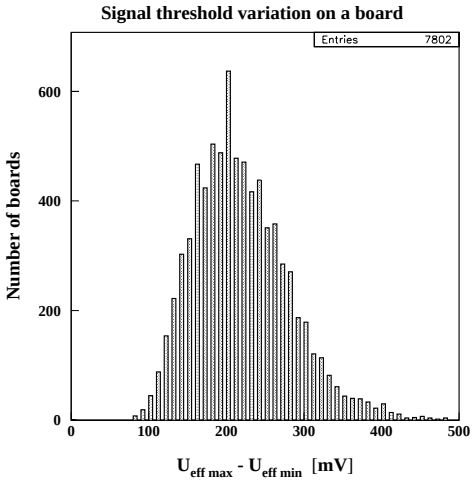

Figure 4. Threshold uniformity on an ASD-8 board: distribution of the difference between maximal and minimal reference threshold U_{eff} on a board.

where $\overline{U_{eff}}$ are the mean values of the signal categories ($\overline{U_{eff}} = 900$, 1000, 1100, 1200 mV). A chip was assigned to one of the 12 categories according to its minimal U_{eff} and maximal U_{noise} values. The assignment was used to mount similar chips on a board (carrying two chips) and combine similar boards to groups which are supplied with the same threshold. Chips with worse noise performance are used in less sensitive areas (lower rates, 10 mm cells).

5. THE ASD-8 BOARD

5.1. The Board Design

Design considerations: The analog inputs of the ASD-8 chips have a very high sensitivity in the order of 1 fC which makes them susceptible to noise and RF pickup. Because of the combination of analog inputs and digital outputs on the chip one has in particular to worry about feedback from the output to the

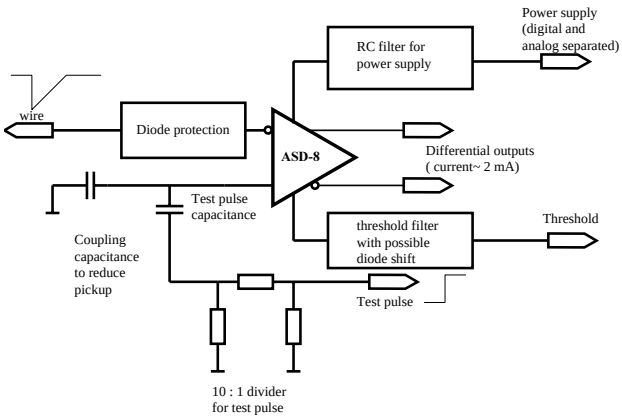

Figure 5. Schematic of the ASD-8 board.

input. In the design of the printed circuit boards carrying the ASD-8 chips special care was taken for a good grounding scheme, decoupling of the analog and digital parts, noise rejection from power sources and noise and crosstalk separation of different channels in a densely packed environment.

The board design: Two ASD-8 chips with 8 channels each are mounted on a multilayer board (table 2, fig. 5).

The chip has a fully differential input: the anode signal is fed into the negative input and the positive input is connected via 10 pF to the chamber ground which reduces the RF pickup.

All supply voltages (± 3 V) are separated into analog, digital and output drive supplies and have RC filters at the input. Between the analog and digital part of the chip is a gap in the groundplane. Both grounds are connected via an inductance at the input connector. The analog ground is extended to rails along the sides of the board which slide into the holding brackets on the chambers. The brackets are made of Cu Be springs providing a fine-mashed shielding between the boards in the densely packaged front-end electronics on the chambers.

Since it was found that the ASD-8 inputs survive voltage spikes only up to about 300 V a diode protection was added. Tests have shown that the diode in combination with an input resistor of 50 Ohms protected the input transistors for discharges of 3000 V fed into the input via a 1 nF capacitor.

Only one voltage level for the thresholds is provided per board. The two chips on each board were therefore matched according to their gain and noise quality class (see chip tests, sect. 4.2). The maximum difference of the reference thresholds U_{eff} of two channels of a single board should be less than 300 mV. In some cases Schottky diodes ($U_f = 200$ or 380 mV) were used to shift the threshold of chips or single channels to avoid more categories or to reduce the rejects. The variations of the threshold sensitivities for different boards will be compensated by a threshold correction table.

The differential open collector output is current progammable. Pull-up resistors on the TDC boards of 62 Ω yield at the chosen current of 2 mA a swing of 120 mV (an offset of 1.25 V is added by the receivers on the TDC board). The analog outputs of the chips are not enabled.

Testpulses can be coupled to the positive input via a 1:10 divider (reduction of noise pickup via the test pulse system) and a 1 pF capacitance. The pulses fire all channels on a board at the same time.

5.2. Board Tests

The 11000 produced boards had to undergo quality tests and were then sorted according to 12 categories as done for the single chips: 4 categories (1, 2, 3, 4) according to the threshold of 50% efficiency for 4 fC U_{eff} and 3 categories (green, blue, red) of signal-to-noise distance $U_{eff} - U_{noise}$. A board enters into a category according to the channels with minimal U_{eff} and maximal U_{noise}.

Table 3 shows the distribution of the boards in different categories. For each board the two chips belong to the same category. The remaining variations of U_{eff} within the 16 channels can be seen in fig. 4 which shows the difference between the maximal and minimal U_{eff} on the boards. Differences larger than 300 mV have been decreased by Schottky diodes as described above. With this procedure the threshold uniformity on the bords is about $\pm 15\%$. The variations between different boards are accounted for by the threshold setting on the distribution boards.

The board quality is mainly determined by the $U_{eff} - U_{noise}$ category. Table 3 shows that more than 80% are in the two better categories 'green' and 'blue'.

6. ELECTRONICS INSTALLATION AND COMMISSIONING

The ASD-8 boards of the different categories were installed such that for the high-occupancy, innermost detector parts amplifiers with a large signal-noise difference (e.g green) are chosen. The outer detector parts, contributing less to the acceptance, are equipped with boards which have a small signal-noise difference (e.g. red). The CAN bus controlled distribution cards allow to set individual thresholds for groups of 8 ASD-8 boards (see sect. 3).

Cu-Be rails soldered to the gas box are used to provide good ground connection between the gas box and the individual ASD-8 boards. In addition shielding of the output signal cables is necessary to minimize the capacitive feedback of the digital output signals to the amplifier inputs. Care is taken that the shielding has a very good, low impedance contact to the digital ground potential of the ASD-8 board. Bad ground connections between either amplifier and gas box or amplifier and cable shielding leads to oscillations of the amplifiers with their characteristic frequency of about 40 MHz.

Table 3. Distribution of the tested ASD-8 boards in signal-noise categories, 4 categories (columns) for different gains, 3 categories (rows) for different signal-noise distance ($\overline{U_{eff}} = 900, 1000, 1100, 1200\,\mathrm{mV}$).

$\overline{U_{eff}} - U_{noise}$ [mV] ↓		U_{eff} [mV] 850–950	960–1050	1060–1150	>1150	whole range
> 550	(green)	4.6 %	12.6 %	20.3 %	4.4 %	42.0 %
500 ± 50	(blue)	4.2 %	18.0 %	12.1 %	4.4 %	39.0 %
400 ± 50	(red)	4.0 %	6.1 %	8.2 %	0.6 %	19.0 %
whole range		12.8 %	36.7 %	30.6 %	9.4 %	

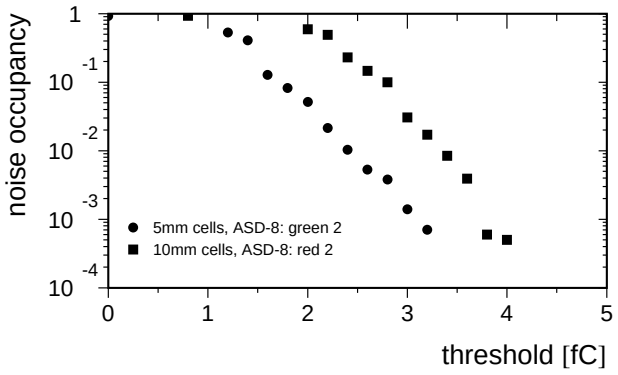

Figure 6. Noise occupancies for two different sectors of a superlayer after installation in HERA-B: The 5 mm cells are equipped with ASD-8 boards from the best noise category (green) while the 10 mm cells are connected to boards of the worst noise category (red).

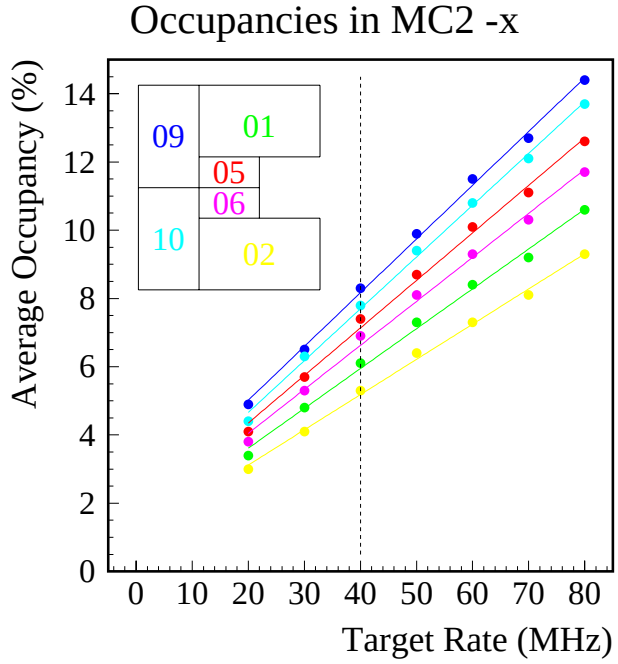

Figure 7. Hit occupancies per channel as a function of the primary interaction rate in sectors of a superlayer at different distances to the proton beam. In the upper left corner the position of the sectors is indicated; the proton beam goes through the cut-out on the right.

The above measures lead to very low noise of the readout chain. Operated at the threshold values U_{noise} from the laboratory tests the complete chain consisting of ASD-8 boards, plugged to the gas box, 5 m long twisted-pair cable for the connection to the TDC, and TDC boards for the digitization, showed noise occupancies of less than 1 % (96 ns large readout windows).

The connection of the honeycomb modules to the amplifier leads to a higher noise level. To compensate the antenna effect of the up to 2 m long wires, an increase of the threshold voltage by 150 to 200 mV, corresponding to about 0.8 fC, is necessary.

The noise occupancies (readout window of 96 ns) for two sectors of a superlayer after installation in HERA-B are shown in fig. 6. The plot shows a sector with 5 mm cells equipped with ASD-8 boards with low noise threshold (green) and a sector with 10 mm cells and ASD-8 boards from the worst noise class (red) is shown. For the 'green' ASD-8 boards the threshold can be set as low as 2 fC, while for the 'red' category the threshold has to be increased to about 3 fC to achieve a similar noise level ($< 10^{-2}$).

The well-functioning of the readout chain for large particle fluxes is illustrated in fig. 7. The hit occupancy for the different sectors of a superlayer (magnet chamber) is shown for different target interaction rates (primary proton-nucleus interaction rate). The measured occupancies depend up to 80 MHz linearly on the interaction rate, well above the nominal interaction rate of 40 MHz. There is no saturation effect at high occupancies observed (the offsets at zero target rate results from electronic noise and background from the HERA accelerator)

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