THE HERA-B HIGH-P_T LEVEL-0 TRIGGER LOGIC ELECTRONICS

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Abstract

The high-p_t trigger has been proposed for broadening of the HERA-B physics program. A dedicated logic system is needed to select events out of a data stream with typical rate of 10^{12} hits/sec. The paper describes the trigger logic electronics system and data processing which provide necessary speed and flexibility for the level-0 trigger selection criteria.

1. INTRODUCTION

One of the main goals of the HERA-B experiment is the measurement of the asymmetry in B $\rightarrow$ J/ψK^{0}s decay mode. The high-p_t 'hadron' trigger considerably broadens the HERA-B physics program. It provides the experiment with the ability to measure CKM unitary triangle angles α and γ by detection of the B $\rightarrow$ $\pi^+\pi^-$ and   B $\rightarrow$ K π decays [1], the expected numbers of reconstructed events are 500 and 750 per year correspondingly. The high-p_t trigger allows either to measure the Bs mixing frequency in B$s \rightarrow$ Dsh mode, where the expected number of reconstructed events is about 400 per year.

The high-p_t Level-0 trigger (pretrigger) selects candidates for particles with large transverse momentum and provides the First Level Trigger (FLT) with initial information to start the track finding process. It is able to detect and encode approximately 10^8 track candidates out of 10^{12} possible combinations per seconds.

A description of the main components of the High-p_t pretrigger system can be found in [2]. This paper mainly describes the logic electronics.

2. PRETRIGGER HARDWARE IMPLEMENTATION

The high-p_t pretrigger is organised using approximately 19000 pads of different size distributed among three layers of chambers located in the magnet. There
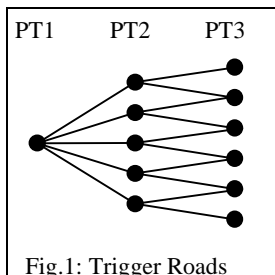
is a projectivity between position and size of correspondent pads in three layers with respect to the vertex position. Pad sizes are varying in correspondence with their distance from the beam.

Fig.1: Trigger Roads

For the high-p_t pretrigger the following track selection algorithm has been implemented (s. fig.1): each pad of the first chamber layer (PT1) maps to up to five adjacent pads in the second

layer PT2, and each pad of PT2 maps to two adjacent pads of the third layer PT3. The tracks with large transverse momentum produce signals in projective or adjacent pads of three chamber layers.

The pretrigger logic electronics has sectional structure and consists of three types of boards, the Link Board, the Pretrigger Board and the Message Generator (Master Card). Each section is covered by one Master Card and up to 8 Pretrigger Boards, while each Pretrigger Board is connected to 6 Link Boards.

The Link Board is located near the detector and provides via optical fibres the fast data transfer to the main trigger Logic.

A Pretrigger Board receives the data of two complete pad rows of all three detector layers. Data which match to the trigger algorithm are encoded and transmitted to the Message Generator on a dedicated bus.

The Message Generator acquires data pattern from a group of connected Pretrigger Boards, transforms them by means of a look-up table into some messages, which are sent to the Track Finding Unit (TFU) of the HERA-B Level-1 Trigger system.

3. LINK BOARD

Fig.2 shows the block diagram of one link channel on the Link Board. It transmits the digital data of two
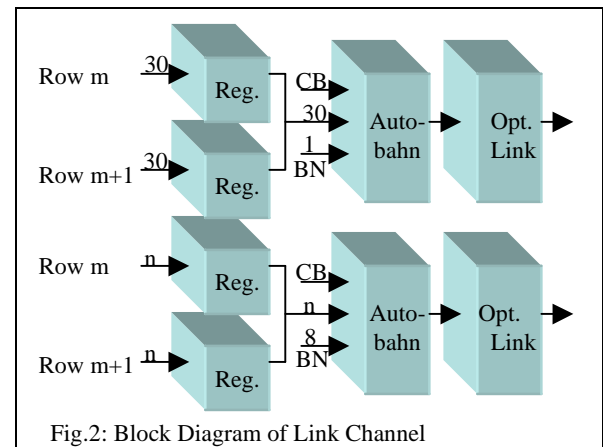

Fig.2: Block Diagram of Link Channel

half chamber rows during one bunch crossing interval of 96 nsec. Therefore at first the incoming data have to be stored in registers. With a period of 48 nsec the register outputs are multiplexed to two Autobahn transmitters (Motorola MC100SX1451), which are 32-bit parallel-to-serial transceivers with an effective data rate of 800 Mbit/sec. On the first transfer channel 30 pad bits are sent together with one Bunch Number bit and a Cycle Bit CB, which distinguishes between the two detector rows. The second transmitter sends the

remaining pad bits, the complete Bunch Number BN and again the Cycle Bit.

The serial Autobahn output is connected to an optical transmitter [3], which sends the data to the Pretrigger Board over a distance of about 45 m.

One Link Board contains three link channels. It is operating synchronously with the Bunch Clock. It has been designed as piggy back on the Front End Driver Card, which collects the pad bits for data acquisition.

4. PRETRIGGER BOARD

The Pretrigger Board PTB searches for coincidence pattern as trigger candidates and combines for each trigger road the involved pads to data packages, which are sent to the Message Generator. Fig.3 shows a block diagram of its main components.

4.1 Data Transfer from the Detector

During one HERA bunch crossing interval the Pretrigger Board has to receive and process the complete pad information of two detector rows of all three planes. Since the maximum number of pads per row is 96, every 48 nsec in total 278 detector bits together

clock period of 48 nsec. With the first strobe a data set of 3*96 bits is stored in the Input Register. For each pad of the first layer, which is found to be a starting point of a trigger road, a Road Starting Flag RSF is set. The resulting RSF pattern together with the pad information of the other layers then is stored with the next strobe. Only if at least one RSF has been detected, a Road Flag (R-Flg) is set and the complete data set is written to the Event FIFO with the third strobe (Zero Suppression).

The Coincidence Logic has been implemented by means of 6 large CPLD's (Vantis, MACH466), which are in-system programmable. So the coincidence algorithm easily can be modified by reprogramming the firmware. A VME access to the Coincidence Logic is provided for a Mask Register, which allows to disable each input bit individually, and for a Test Register, which in Test Mode emulates the detector input.

4.3 Bunch Number Comparison

On each of the 12 transfer channels to the PTB some Bunch Number bits are transmitted. Since these are the only predictable information, they are used to monitor
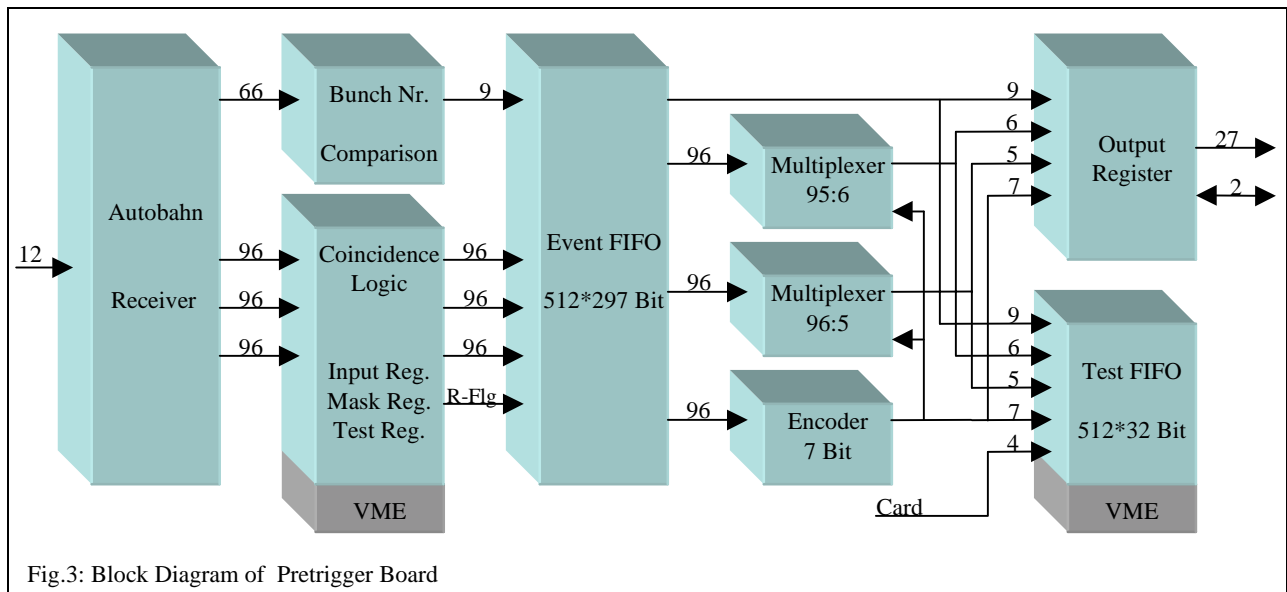

Fig.3: Block Diagram of Pretrigger Board

with redundant bunch number information are sent to the PTB on 12 transfer channels. Each channel consist of a pair of Autobahn transceivers (Motorola, MC100SX1451) and an optical link between their serial ports [3].

4.2 Coincidence Logic

The Coincidence Logic is able to combine each pad of the first detector layer with up to 5 pads of the second and up to 6 pads of the third layer. Fig.1 shows an example of a possible Trigger Road structure. The Logic has been designed as a 3-stage pipeline with a

the reliability of data transfer by comparing 66 bits in real time. If a comparison fault is detected, an error flag is set, and an interrupt can be generated.

4.4 Event FIFO

The Event FIFO stores data sets consisting of a 96 bit RSF pattern, two 96 bit pad pattern of the second and third chamber layer, the 8 bit Bunch Number and the Cycle Bit. It decouples the system clock on the input side, which is synchronised with the Autobahn clock and has a period of 48 nsec, from the output system clock with a frequency of 25 MHz. Addition-

ally it acts as data buffer, because one input data set can generate more then one output data package. The Event FIFO has a depth of 512 words and is built of 17 chips SN74ALVC7804 (Texas Instruments).

4.5 Output Data

The output system clock drives a Finite State Machine controlling the output data generation, which again is organised as 3-stage pipeline process. In the first step a 7-bit Priority Encoder generates a binary code for the actual most significant RSF bit. Then that code is used to address two Multipexers selecting the corresponding up to 5 pads of the second and up to 6 pads of the third layer. The resulting data together with the 8 bit Bunch Number and the Cycle Bit are written to the Output Register in the last step.

4.6 Data Transfer to Message Generator

Since up to 8 Pretrigger Boards have to be connected to one Message Generator, the output data are transmitted on a bus. The communication protocol has been implemented by 8 dedicated 2-wire handshakes providing fast identification of data source. The data transfer time is 40 nsec.

4.8 Additional Features

There are some other important features of the PTB, which for reasons of simplicity are not shown in the block diagram:
⇒ A Veto Logic accept Bunch Numbers distributed by the HERA-B Calorimeter in order to inhibit certain events.
⇒ A 29-bit counter monitors the number of generated output data sets. It can be read-out by VME.
⇒ The maximum number of output data sets per event can be programmed by VME.
⇒ The input system clock is monitored by a watch dog circuit.

5. MESSAGE GENERATOR

The Message Generator receives data sets from several Pretrigger Boards and transforms them to messages, which contain all necessary information according to a standard, which is accepted by the Track Finding Unit TFU of the HERA-B Level-1 Trigger. Fig.4 shows a block diagram of the main components.

5.1 Handshake Logic

The Handshake Logic is responsible for the data
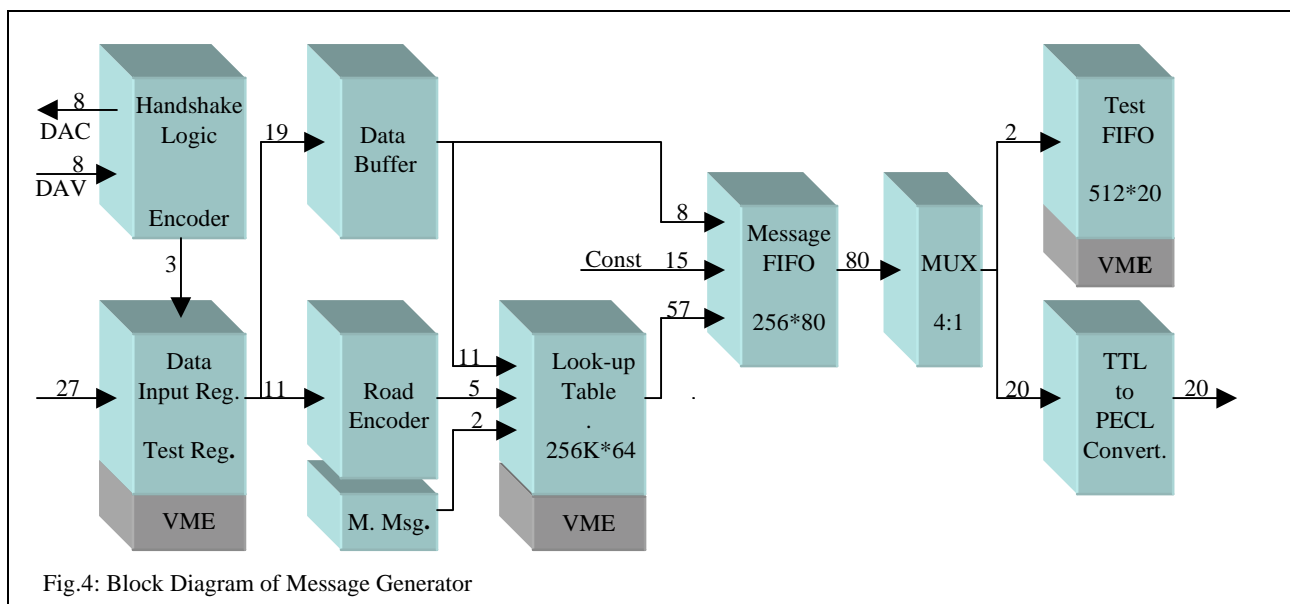

Fig.4: Block Diagram of Message Generator

4.7 Test Facilities

In order to be able to test the Logic of the board, there are Test Registers implemented, which cover the complete input range of 288 bits. The test pattern stored via VME is processed in real time, and the resulting output data are written to a Test FIFO, which can be read-out by VME for comparison with the expected values. The Test FIFO also is useful for monitoring the data stream during data acquisition.

transfer protocol between connected Pretrigger Boards and Message Generator. The eight DAV flags indicating on which PTB a data set is available are stored periodically into the input register of an 8-bit Encoder. If there is at least one flag set, the Encoder starts to select the PTB with the highest number by issuing the corresponding DAC signal, which open the connected PTB data port and enables the 27-bit data set to arrive at the Data Input Register, where it is stored together with the 3-bit code of data source (PTB Code). Then the next DAV flags are selected one after another, until

the Encoder Input Register is empty and the next DAV pattern is stored. That method ensures, that all PTB's are selected with equal probability.

The data transfer rate between Pretrigger Board and Message Generator is 25 MHz.

5.2 Data Input Register

The Data Input Register is the first stage of a 3-stage pipeline. It has a width of 30 bits and distributes 19 bits (RSF Code, PTB Code, Bunch Number, Cycle Bit) to the Data Buffer and 11 bits (pad bits of the second and third detector layer) to the Road Encoder.

5.3 Road Encoder

Together with the Data Buffer the Road Encoder builds the second stage of the process pipeline. It sequentially encodes up to 18 possible combinations between the 11 input pads, Every 40 nsec a new 5-bit code is provided. Together with 11 bits of the Data Buffer (RSF Code, PTB Code, Cycle Bit) and two additional bits, which have been introduced for multiple message generation, it forms the 18-bit address of a Look-up Table, which contains all information necessary to compose the message.

5.4 Look-up Table

The Look-up Table is a 256K*64 bit static RAM with an access time of 15 nsec (IDT7MP4045). For each possible road 57 out of 64 available bits are used to provide all relevant parameters. The table can be written and read-out by VME.

5.5 Message FIFO

The Message FIFO (IDT72205) receives besides the data bits of the Look-up Table the Bunch Number and some 15 constant bits reserved for each subdetector. It is the last stage of the pipeline, which is clocked with 25 MHz frequency. It also acts as message buffer, because the output data stream may be disabled by the connected TFU's for short times.

5.6 Data Transfer to TFU

The Message Generator is connected to several TFU's by a 20-bit bus. Therefore the messages have to be split into four parts by a multiplexer. The resulting packages are converted to PECL level and transmitted with a frequency of 100 MHz.

5.7 Test Facilities

Again the complete Logic of the board can be tested in real time by writing data pattern to the Test Register, starting the evaluation process and reading the resulting message packages from the Test FIFO, which monitors the output data stream.

6. SYSTEM LAYOUT

Pretrigger Board and Message Generator are VME boards of 9 height units and 340 mm depth. Two clusters each consisting of one Message Generator and up to eight Pretrigger Boards are located in one VME crate. Four such crates are sufficient for the complete High- P_t Level-0 Trigger.

In order to reduce the power consumption 3.3V technology has been used as far as it was available. Nevertheless the power consumption adds up to about 1 KW per crate mainly because of the large number of Autobahn chips used..

7. STATUS

Prototypes of all three boards have been built and tested successfully. Series production has been started and the complete system will be available at the end of 1999.

8. REFERENCES

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