CHARGE AMPLIFIER AND ANALOG MEMORY FOR SILICON DRIFT DETECTORS IN ALICE

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ABSTRACT

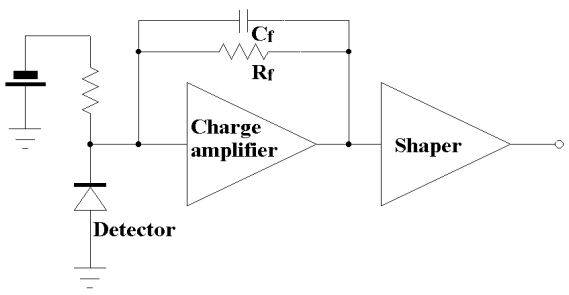
In Silicon Drift Detector front-end the signals coming from each anode of the detector are sent to one input of a Preamplifer-Shaper whose outputs are connected to the inputs of an Analog Memory (AM). The AM continuously samples the analog signals at 40 MHz (the bunch-cross rate) and stores all the data. When some suitable conditions are detected, a trigger signal stops the write phase. Then a read phase begins to transfer, at lower rate (1 MHz), the data to another device that performs digitalisation.

SUMMARY

According to our simulations [1], a preamplifier-shaper has been designed. It has 8 channels. Each channel consists of a charge preamplifier and a CR-RC shaper to limit noise. Thermal and shot noise has been simulated as 300 e-. Since the foreseen leakage current is not more than 10 nA, the preamplifier has a sensitivity of 155 mV/MIP, in order to achieve the assigned 7 Mip range. The shaper has a gain of 1 V/V and a driving capability of 7 pF as required by the 256-cell Analog Memory.
A 16 channels 256 cells analog memory has been realised as a switched capacitor array. It works as an analog delay line. The read frequency is 1 MHz driving 15 pF output load and the write frequency is 40 MHz. This device has to be tested. A previous prototype (64 cells 4 channels) working at the same write and read frequency showed during tests the expected performances. Dynamic Range 3.5 V Dc gain 0.9988.

CHARGE AMPLIFIER

Analog front-end has been designed with a traditional scheme, as shown fig. 1. It consists of an integrator and a CR-RC shaper plus an output buffer to drive the analog memory.



Both preamplifier and shaper stages are based on a single-ended folded cascode as shown fig 2. This solution offers better performances in term of stability and gain compared with standard cascode [2] . For preamplifier stage a choice of PMOS input transistor was addressed for better result in term of flicker noise.

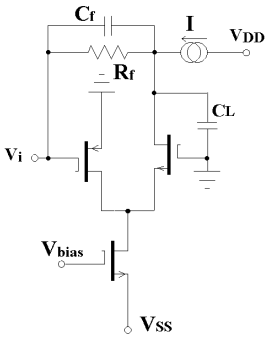


Figure 2 Schematic diagram of core amplifier

Accurate noise analysis was performed to sizing input transistor taking into account detector capacitance and power dissipation. Coupling capacitor of 20 pF was implemented inside the chip.

Main characteristics are:

Table 1 Amplifier Simulation Results

Noise	< 500 e-
Input range	7 MIP
Output range	1 V
Sensitivity	155 mV/MIP
Shaping time	55 ns
Driving capability	7 pF
Power dissipation	2.2 mW

Amplifier test results

A 8-channels amplifier has been realised in 0,8 micron AMS CMOS technology. Test results agree with simulations results showed in Table 1. We have some problem with noise performance that is worse compared with simulations, probably due to the parasitic effects of the coupling capacitance at the input of the preamplifier.

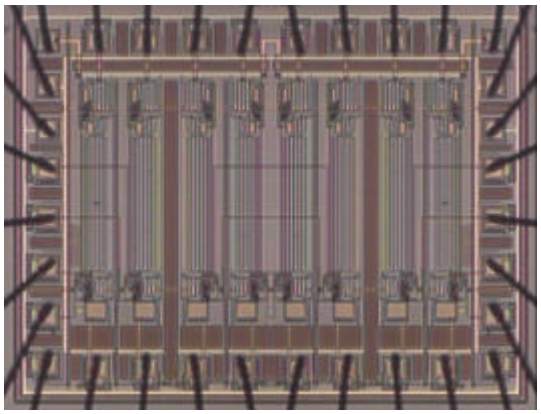


Figure 3 Microphotograph of the chip

Figure 4 shows measured output transient responses of the amplifiers .
This work suggests a new solution for DC coupling amplifier with the compensation of the leakage current.

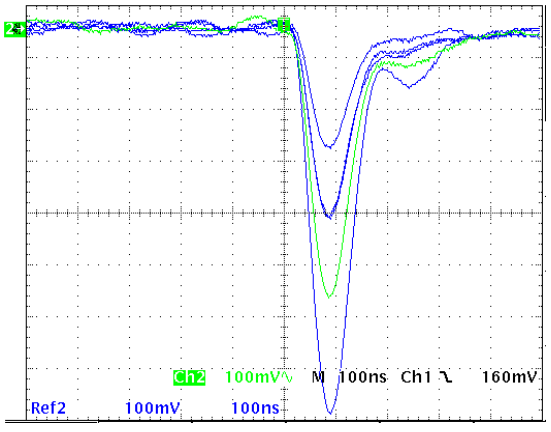


Figure 4: Amplifier measured output response

ANALOG MEMORY

We have designed different prototypes of the ADeLine family Analog Memories. In this section we merely describe the characteristics of ADeLine4 and ADeLine5 chips.
Table 2 ADeLine summarises family main characteristics.

Table 2 ADeLine Family

Chip name	Ch. n°	Cell x ch.	Tot. Cells	Resolution	Tested
ADeLine1	8	256	2048	Not working	*
ADeLine2	1	8	8	<1 mV	*
ADeLine3	3	64	192	6 mV	*
ADeLine4	4	256	1024	< 1 mV	*
ADeLine5	16	256	4096	Not avail.	*
ADeLine6	16	256	4096	Not avail.	Not avail.

Within the overall system, the Analog Memory operates as an analog delay line, sampling the voltage at its inputs at 40MHz rate and storing its values for each channel in a switched capacitors array. This array acts in parallel as a circular memory rewriting new samples over the cells when the overall channel depth has been reached.
Each channel uses an output buffer for the readout of the stored samples. The maximum rate of this phase is 1MHz because of power dissipation constraints.
The Control Unit simply selects cells in a sequential way at different rates for the write and the read phase. This unit consists of a ring shift register whose outputs lines are fed into one input of an array of two inputs AND cells. The other input of the AND cells of this array is an internally generated validating “enable” signal (Figure 5).

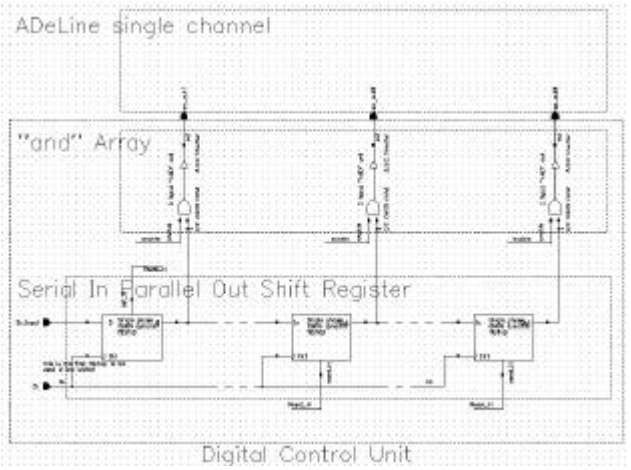


Figure 5. Analog Memory overall structure

The purpose of this "and" array is to guarantee a non overlapping addressing scheme for all cells along the channel. Two different feed control signals are used during the write and the read phase: while in the write phase it is a fixed 50% duty cycle 40MHz system clock, an external acknowledge-based mechanism is used in the read phase. The digitizing device, following the memory in the read-out chain, requires next cells data whenever ready, while memory reacts with a valid data signal. That scheme goes on until all memory cells are read.

Main design constrains for the memory as well as for the whole system has been power dissipation and resolution.

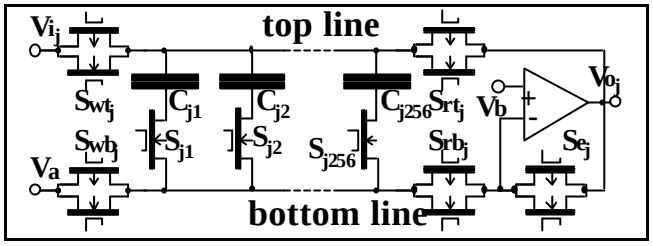


Figure 6: Single ADeLine channel simplified schematic.

Memory Design

ADeLine5 memory chip is an analog full custom VLSI ASIC designed in AMS 0.8µ CMOS 2 metal/2 poly process. Its sizes are 3,3x3,6 mm^2.
The design of the sampling capacitors has been carefully studied to achieve the best matching in order to have high resolution. Dummy capacitors structures was implemented as well.
The memory cells structure (Figure 6) has been designed for a sampling period of 25ns because of the expected input signals whose rise time exceed 50 ns. This fact imposes an upper constraint to the size of capacitors and input switches size while technology and matching considerations impose a lower constraint.
The output buffers use folded cascode transconductance amplifiers for the readout of the selected cell together with a 3 switches configuration.
The design of the digital control part is completely static, advantaging of the low-power characteristics of CMOS gates design. A binary tree clock distribution scheme was implemented as well.
Mixing on the same chip digital and analog parts has conduced to an accurate grounding scheme to avoid unwanted signals coupling that worse resolution.

Memory simulation and test results

Tests have been performed on ADeLine4 and ADeLine5 chips. They show a resolution of 10 bit with a noise of 0.821 mV in a voltage range of 3.5 V.
The new ADeLine5 chip is a 256 cells 16 channels analog memory and it is currently under test but preliminary results are it similar to the ADeLine4 chip tests.
A new chip, ADeLine6, has been designed and sent to the foundry: it will be available at the end of November. It has the same characteristics of ADeLine5 but a new standard cells control unit has been added. To reduce the external signals needed generates the acknowledge signals inside the chip.

CONCLUSIONS

Test measurements show that both preamplifier and analog memory need some adjustments to fit the experimental requirements. Anyway their measured performances are quite near to specifications.
The next step will be a chip containing both preamplifier and analog memory in order to test the whole electronic chain.

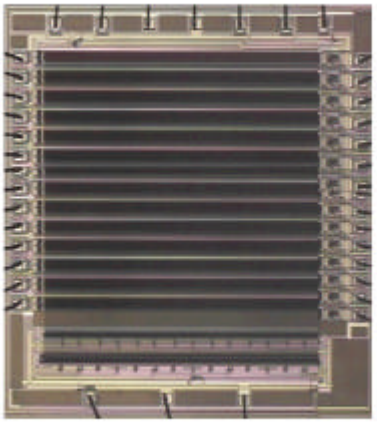


Figure 6 ADeLine5 chip microphotography

REFERENCES

[1] C.Petta, U.Becciani, G.V.Russo, "Simulation and characterisation of the front-end of SDD in ALICE ITS" ,Proc. of 4th LHC Electronics Conf., Rome, 21-26 Sept. 1998, pp.610-614
[2] M. Ismail, T. Fiez – Analog VLSI – Mc Graw Hill
[3] S. Panebianco et al. "Switched capacitor arrays analog memory for sparse data sampling", to be published in Nuclear Instruments and Methods in Physics Research.