The ALICE Detector Data Link

György Rubin[1], Pierre Vande Vyvre
CERN, CH-1211 Geneva 23, Switzerland
Péter Csató, Ervin Dénes, Tivadar Kiss, Zoltán Meggyesi, János Sulyán, György Vesztergombi
KFKI-RMKI, H-1525 Budapest, P.O.Box 49, Hungary
Bertalan Eged, István Gerencsér, István Novák, Csaba Soós, Dénes Tarján, Attila Telegdy, Norbert Tóth
Technical University of Budapest (BME), H-1111 Budapest, Műegyetem rakpart 3-9, Hungary

Abstract

The ALICE detector data link has been designed to cover all the needs for data transfer between the detector and the data-acquisition system. It is a 1 Gbit/s, full-duplex, multi-purpose fibre optic link that can be used as a medium for the bi-directional transmission of data blocks between the front-end electronics and the data-acquisition system and also for the remote control and test of the front-end electronics. In this paper the concept, the protocol, the specific test tools, the prototypes of the detector data link and the read-out receiver card, their application in the ALICE-TPC test system and the integration with the DATE software are presented. The test results on the performance are also shown.

Introduction

During the preparation of the ALICE Technical Proposal **[1]** the need emerged for a common interface between the *front-end electronics* (FEE) of the different detectors and the *data acquisition system* (DAQ). A dedicated working group was formed to collect in a document **[2]** the needs of the detectors and the DAQ. The following main requirements have been identified:

- only one standard link, named *detector data link*, for the information transfer between the FEEs of all the sub-detectors and the DAQ;
- standard protocol;
- point-to-point full-duplex optical connection;
- high-speed transmission of event data;
- remote control and test of the FEEs from the DAQ;
- bi-directional data block transfer between the DAQ and the FEEs.

Concept

The detector data link (DDL) and the read-out receiver card (RORC) constitute together the detector read-out chain. The DDL transfers the event fragments from the experimental pit to the computing room and stores them in the input buffer of the RORC. The RORC interfaces the DDL to the front-end digital crate (FEDC). The DDL consists of the following components:

- *source interface unit* (SIU), connected to the FEE;
- *destination interface unit* (DIU), connected RORC;
- physical medium (two fibre optic cables).

The FEDC is responsible for the sub-event building. The RORCs, plugged-in the FEDC, are controlled by a SBC. The *local data concentrator* (LDC) reads-out the event fragments from the RORCs and assembling them into sub-events. Then the sub-events are sent to the central event building switch. If it is reveals to be needed, separate I/O busses could be used for the control and the read-out functions in this crate, because of the speed limitation of the available standard backplanes. We hope, however, that in a few years high-performance channel-based I/O busses (e.g. *System I/O*) or really fast standard backplanes (e.g. *VME320* or *VME1000*) will be available. In this case the two I/O busses will be merged and the final version of the FEDC will have only a single I/O bus.

Figure 1 shows a part of the ALICE DAQ, consisting of a detector read-out chain and a sub-event building system.

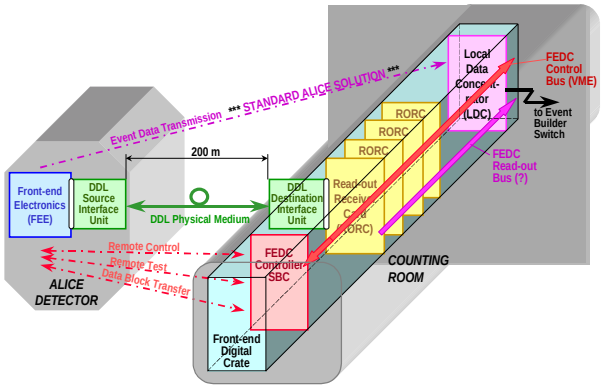


Figure 1 Part of the ALICE DAQ

[1] **E-mail:** ***Gyorgy.Rubin@cern.ch***

In most applications, the SIU will be connected directly to the FEE (see Figure 2).

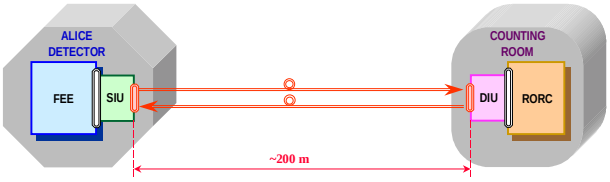


Figure 2 Direct connection to the FEE

In some of the applications (for example, where the level of the radiation is too high for the SIU), the SIU will be placed outside of the detector with a distance of several meters. In this configuration a radiation hard medium-speed transceiver shall be used inside the FEE. The DDL is connected to the FEE through a DDL. This configuration is foreseen for the Si-Pixel detector.

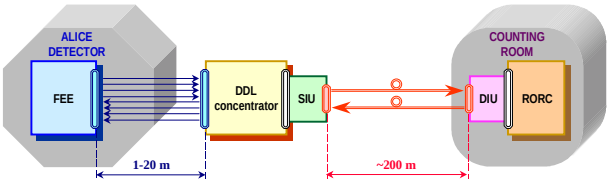


Figure 3 Indirect connection to the FEE

Figure 4 shows another possibility for the indirect connection. In this case the DDL concentrator is implemented as a VME interface, and the information is transmitted between the two VME crates by using two DIUs and two RORCs. This configuration is foreseen for the trigger detector, because the trigger unit will be placed in a VME crate. Dedicated software will emulate the behavior of the SIU and the FEE, so from the DAQ point of view this configuration will be identical to the basic configuration.

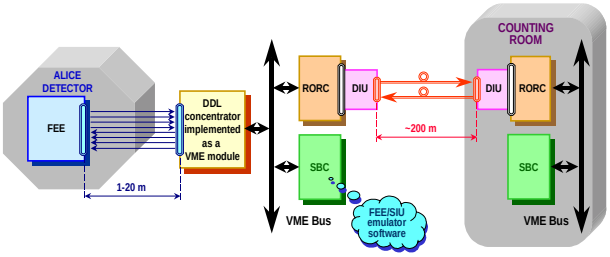


Figure 4 Indirect connection through VME bus

The DDL is connected to two external systems (e.g. FEE and RORC). The RORC-DIU interface consists of 2 uni-directional busses for the full-duplex information transfer (see Figure 5). It is, for example, possible to send commands to the FEE or the interface units, while event data are transmitted from the FEE to the DAQ.

The FEE-SIU interface consists of a bi-directional bus and a JTAG controller port **[3],** which can be used for the remote testing and control of the FEE via the TAP.

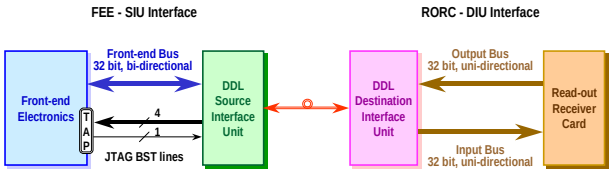


Figure 5 The DDL interfaces

Main technical parameters

The main data flow will take place from the FEE to the RORC. The DDLs will be able to read-out the complete ALICE events (40 MB) within less than 2 ms, transmitting event data from the FEE to the RORC with a detected bit error rate of $\leq 10^{-15}$. Each DDL will be able to transmit data at a rate of 100 MB/s. As the zero suppression algorithm requires downloading big blocks of data into the FEE, a throughput of 10 MB/s is needed in the opposite direction. Both the FEE and the SIU will be remotely controlled from the FEDC through the DDL, since their placement inside the detector will not allow using any other cabling apart from the DDL physical medium. Therefore, commands and status information will also be transmitted between the FEE and the RORC. Since the SIU is located inside the detector, the requirements for the lifetime ($\geq$ 10 years), the power consumption ($\leq$ 5W) and the footprint ($\leq$ 50 cm^2) of this unit are key issues. More strict requirements have been identified for the ITS **[2]** sub-detectors where radiation tolerant electronics is needed and the footprint of the SIU shall be less than 20 cm^2. To achieve the high reliability of the experimental apparatus, efficient test of all the sub-systems will be provided. The DDL will allow testing the FEE remotely by using JTAG controller port of the SIU. The DDL itself will also have a powerful self-test mode.

DDL protocol

1. Protocol layers

The DDL protocol consists of four layers: the DDL interface layer (most upper), the signaling and framing layer, the coding layer and the physical layer.

The DDL interface layer is described in the *Interface Control Document* (ICD) **[4]**. It includes the physical and electrical description of the interface units. The ICD defines also the interface signals, the information structures, the transactions and the timing.

The signaling and framing layer is described in the *Physical and Signaling Interface Specification* **[5]**. It is

a mixture of the FC(2) layer of the Fibre Channel Standard **[6]** and DDL specific solutions.

The coding layer is compatible with FC(1) layer of the Fibre Channel Standard (FCS), where the well known 8B/10 coding scheme is used **[7]**.

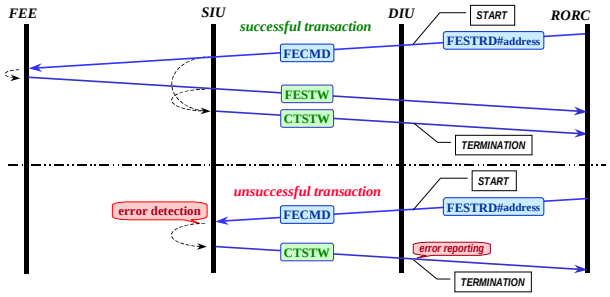
The physical layer is compatible with FC(0) layer of the FCS. For the DDL prototype the ***100-M5-SL-I*** nomenclature is used, having the following main parameters: 100 MB/s transmission speed, 50 μm multi-mode optical fibre, 850 nm laser transmitter, data transmission up to 500 m distance.

2. Transactions

The information transfer on the DDL is organised in control-status transactions and block transfer transactions. The control-status transactions are simple, while the block transfer transactions are complex, consisting of several control-status transactions. All the transactions are started by a command and terminated by a *command transmission status word*. It indicates, if any errors have occurred during the transaction.

The following control-status transactions are defined:
- front-end electronics control;
- front-end electronics status read-out;
- interface unit control;
- interface unit status read-out.

Figure 6 shows the FEE status read-out transaction, as an example of the control-status transactions.



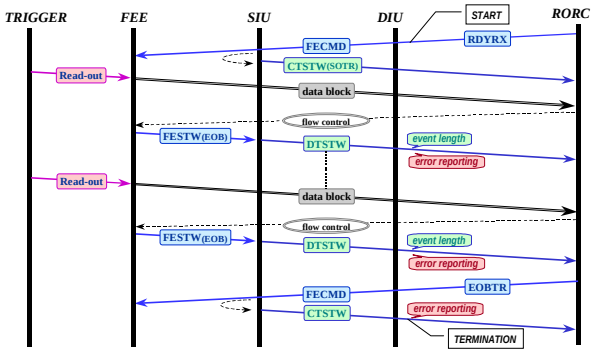
Legends:

FECMD	*- Front-end Command*
FESTRD	*- Front-end Status Read-out (FECMD)*
FESTW	*- Front-end Status Word*
CTSTW	*- Command Transmission Status Word*

Figure 6 The FEE status read-out transaction

The following block transfer transactions are defined:
- event data transmission;
- data block downloading;
- data block read-back;
- self-test.

Figure 7 shows the event data transmission transaction, as an example of the block transfer transactions.



Legends:

FECMD	*- Front-end Command*
SOTR	*- Start of Transaction flag*
RDYRX	*- Ready to Receive (FECMD)*
CTSTW	*- Command Transmission Status Word*
FESTW	*- Front-end Status Word*
EODB	*- End of Data Block flag*
DTSTW	*- Data Transmission Status Word*
EOBTR	*- End of Block Transfer (FECMD)*

Figure 7 The event data transmission transaction

Prototype project

The main goals of prototype development project are:
1. build a prototype of the complete read-out chain;
2. develop hardware and software tools for the test;
3. integrate the read-out chain with DATE **[8]** software;
4. try out the system in normal working conditions.

1. Components of the read-out chain

The following tasks are included in this project:
- experimental *media interface* (MI) design and test;
- DIU development;
- RORC development;
- SIU development.

Within the MI test sub-project, the design and the test of an 1.06 Gbit/s MI circuits and an experimental PCB layout and stack-up have been accomplished and the main functional components have been selected and tested. The results of these tests **[9]** allow us to safely integrate the high-speed serial MI directly on the DDL cards.

Within the DIU development sub-project a first prototype version and an improved prototype version have been designed, built and tested. The DIU photos can be found on the WEB **[10]**. The DIU consists of two main functional parts: the protocol engine and the media interface (see Figure 8). In the protocol engine the three upper layers of the DDL protocol are implemented. The MI interfaces the protocol engine to the physical medium. It realises only the lower protocol layer. It is able simultaneously to send and receive serial data stream with a transmission speed of 1.06 Gbit/s, so some

signals in this sub-system can have harmonics up to 7 GHz. The PCB layout design is quite critical here, this is the explanation why a MI test project was necessary. The main technical features of the DIU are:

- multi-volt system (+5V and +3.3V supply voltages);
- 48 cm^2 footprint;
- 9x1 OT[2] with duplex SC fibre optic connector;
- FC[3] electrical transceiver (53 MHz reference clock);
- protocol engine is in two FLEX10K50A PLDs:
  - 4 clock signals are used
  - single port FIFO is available only
  - 240-pin RQFP package
  - +3.3V core logic;
- two EPC1 configuration PROM;
- passive serial configuration.

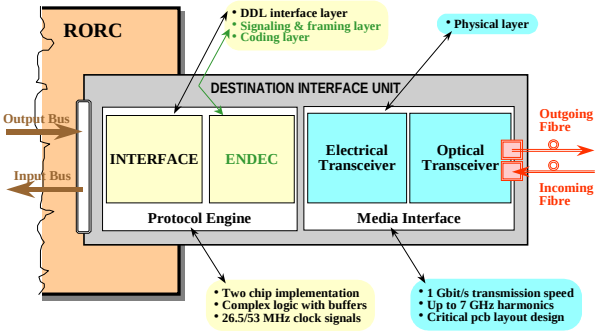


Figure 8 The architecture of the DIU

The prototype SIU now is under development. The components have been selected, the mechanical, the PCB layout and the digital designs are ready. The SIU has similar architecture as the DIU. The main technical features of the SIU are:

- single +3.3V system;
- 27 cm^2 footprint;
- 5x2 SSF[4] OT with VF45-RJ fibre optic connector;
- serial backplane electrical transceiver:
  - 53 MHz reference clock
  - built-in elastic buffer
  - 106 MHz reference clock
  - built-in 8B/10B encoder/decoder
- protocol engine is in one FLEX10K100E PLD:
  - 2 clock signals are used
  - dual port FIFO is available
  - 256-pin FineLine BGA package
  - +2.5V core logic;
- single EPC2 configuration EPROM;
- ISP configuration via JTAG chain.

[2] **optical transceiver**
[3] **fibre channel**
[4] **small form factor**

Within the RORC development project, a first prototype and an improved prototype version have been designed, built and tested **[11]**. The photos can be found on the WEB **[10]**. The main task of the RORC is to receive and store temporary the event fragments, coming from the FEEs through the DDL **[1]**. When the LDC is free, the event fragments are read out from the RORC by the LDC for the sub-event building. The RORC is also able to transmit data blocks and commands to the FEEs and receive status information from them through the DDL.

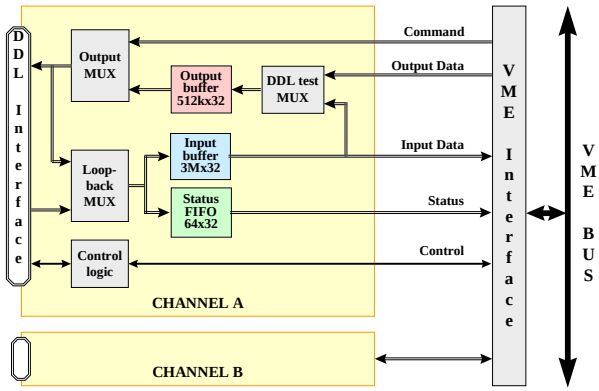


Figure 9 The architecture of the prototype RORC

The RORC consists of two memory buffers for the high-speed transmission of the incoming and the outgoing data blocks and a FIFO for the incoming status information. For the testability, a loop-back multiplexer and a DDL test multiplexer are used, supporting the RORC and the DDL self-test working modes. Figure 9 shows the architecture of the prototype RORC. The main technical features of prototype RORC are:

- normal, RORC and DDL self-test modes;
- two DDL channels;
- up to 3M x 32 bit input buffer;
- 512k x 32 bit output buffer;
- 64 x 32 bit status FIFO;
- VME64x (VITA 1.1-199x) module and connectors;
- 6U board height;
- A32, D8-32, D32_BLT, D64_BLT transfer types;
- 50 MB/s block transfer rate;
- slave and interrupter building blocks;
- programmable base address;
- interrupt event: status FIFO is not empty.

2. Hardware and software tools for the test

For testing and monitoring of the DDL and the RORC, the following hardware tools have been developed:

- DIU extender (DIUEXT);
- SIU extender (SIUEXT);
- SIU simulator (SIMU);
- FEE emulator (FEMU).

The DIUEXT is an extender board, having the same footprint as the DIU. It can be inserted between the DIU and the RORC. There are five connectors on this board, providing connection for logic analyzers for the monitoring all the RORC-DIU interface signals. The photo of the DIUEXT can be seen on the WEB **[10]**.

The SIUEXT is an extender board, having the same footprint as the SIU. It can be inserted between the SIU and the FEE. There are four connectors on this board, providing connection for logic analyzers for the monitoring all the FEE-SIU interface signals.

The SIMU is a manually controlled simple device, having the same footprint as the SIU. It can be used for the basic hardware tests of the FEE. The SIMU is able to execute all the FEE transactions, according to the DDL protocol.

The FEMU is able to emulate the behavior of all the ALICE detectors. It is based on a HP logic analyzer system (see Figure 10). An interface card has been developed for the connection of the HP-LA to the DDL.

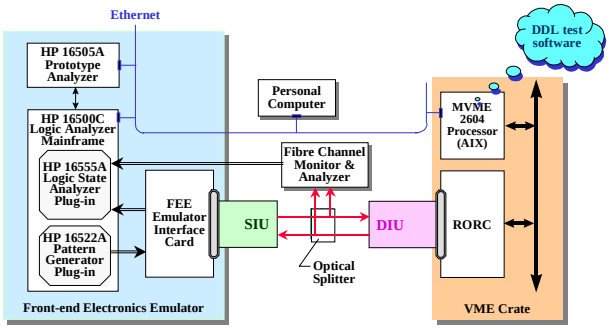


Figure 10 The DDL test setup

Figure 10 shows the DDL test setup, consisting of:

- a FEMU system;
- a MVME 2604 SBC, running on AIX platform;
- a fibre channel line monitor and analyzer.

The DDL test software is running on MVME2604 and MVME4604 processors under AIX 4.2. It has been developed for the functional, the performance and the qualification tests of the DDL **[12]**.

The data traffic on the optical fibres can be studied by using a FCS monitor and analyzer device.

System test within normal working conditions

The DDL first has been tried-out within normal working conditions in the ALICE-TPC test system **[13]**. In this test setup (see Figure 11) the DDL has been used in indirect configuration (see Figure 4). For requesting the transmission of event data block, a command is sent from the *read-out crate* to the *front-end crate*. This action is followed by an event transfer in the opposite direction.

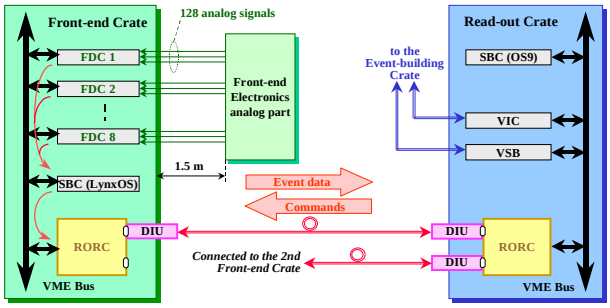


Figure 11 Integration in the ALICE-TPC test system

Integration with DATE software

The DATE **[]** is currently used by the NA57 experiment as data acquisition software. In the future, most of the ALICE sub-detectors will use the DATE for the FEE tests and the beam tests as well. Since the DDL and the RORC will also be key elements of these tests, the integration of the complete read-out chain with the DATE software is a high priority task. Therefore DDL software library has been integrated with DATE during the Q2/1999 **[14]** and the complete read-out chain has successfully been tested by transmitting several TB of data with different patterns and block lengths.

Performance Tests

The system performance has been tested in DIU-DIU configuration. The task-to-task command delivery time between two MVME 2604 processor is about **6 µs**. The read-out speed has been measured in 64-bit block transfer mode by using both MVME 2604 processors and MVME 4604 processors. Table 1 shows the test results of the for the MVME 2604 processor, while Table 2 for the MVME 4604 processor. It was identified in both cases that the block transfer speed is limited by the DMA speed of the processor, but not by the RORC.

block size [MB]	400	4k	40k	400k	1M
speed [MB/s]	5.0	19.1	26.4	28.7	28.9

Table 1 Data transmission speed with MVME 2604

block size [MB]	400	4k	40k	400k	1M
speed [MB/s]	5.7	23.3	33.7	38.0	38.3

Table 2 Data transmission speed with MVME 4604

References

1. The ALICE Technical Proposal; CERN/LHCC 95-71, ISBN 92-9083-07708
2. “ALICE-DDL User Requirement Document”; ALICE/96-42 Internal Note/DAQ, 12.12.1996, edited by: G.Rubin
3. Joint Test Action Group Boundary-Scan Testing Architecture; IEEE 1149.1-1990
4. G.Rubin and P.Vande Vyvre: “ALICE-DDL Interface Control Document”; ALICE/96-43, Internal Note/DAQ, 12.12.1996
5. G.Rubin: “ALICE-DDL Physical and Signalling Interface Specification”; ALICE/97-04, Internal Note/DAQ, 14.02.1997
6. Fibre Channel Physical and Signalling Interface (FC-PH); ANSI X3.230-1994
7. A.X.Widmer and P.A.Franaszek: “A DC Balanced, Partitioned-Block, 8B/10B Transmission Code”; IBM Journal of Research Development, Vol. 27, No 5, September 1983
8. ALICE DATE User's Guide; ALICE 98/44, Internal Note/DAQ; November 1998
9. T.Kiss e. a.: “Electrical and Signal-Integrity Design of a 1.06 Gbit/s Fiber-optic Media Interface”; Proceedings of the LEB'97 Workshop, p. 500-503, London, September 22-26, 1997
10. http://www.cern.ch/ALICE/pictures/daq/
11. G.Rubin and J.Sulyán: “VME Read-out Receiver Card (RORC) for the ALICE-TPC Test System”; ALICE/97-14, Internal Note/DAQ, 05.05.1997
12. P.Csató e.a.: “Test of the ALICE DDL”, Proceedings of the LEB'98, Rome, September 21-25, 1998
13. J.Bracinic e.a.: "Status Report on the ALICE Prototype TPC with Ring-Cathode Readout" ALICE/Internal Note
14. R.Divia: "DATE/DDL integration"
http://consult.cern.ch/alice/ALICE_Weeks/1999/15/abstract