A 40 MHz clock and trigger recovery circuit for the CMS tracker fabricated in a 0.25 μm CMOS technology and using a self calibration technique

P. Placidi[1], A Marchioro[2], P. Moreira, K. Kloukinas
CERN/ECP, CH-1211 Geneva 23, Switzerland

ABSTRACT

In the CMS central tracker, the LHC clock and the first level trigger decisions are distributed encoded as a single signal. This paper describes an ASIC for clock recovery and first level trigger decoding to be used in the tracker data acquisition and slow control systems. The IC was implemented in a 0.25 μm CMOS technology using a rad-tolerant layout. It recovers the clock and trigger signals meeting the CMS tracker power budget and radiation hardness constraints. In the design of this ASIC a self-calibration techniques was adopted to accommodate for process parameters spread and device parameter changes due to radiation induced damage.

1 INTRODUCTION

The CMS central tracker electronics operates synchronously to the 40.08 MHz LHC master clock. In this system, the clock and the first level trigger decisions are encoded and distributed as a single signal as shown in *Figure 1*.

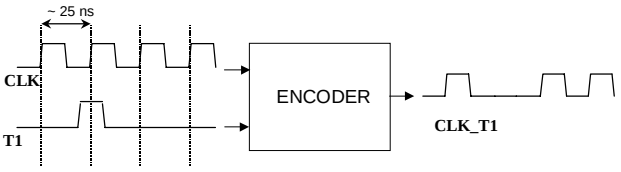

Figure 1 Clock coding scheme

This signaling scheme minimizes the bandwidth and the power requirements of the transmission system. However, a dedicated circuit is required to recover the clock and the trigger signal in the front-end and control modules (*Figure 2*). The recovered clock is used in the front-end APV ASIC for data sampling and therefore jitter less than 0.5 ns is required to maintain the precision of the analog measurements. As the circuit has to be used in an environment close to the sensitive analogue front-end electronics, it is necessary to reduce the switching noise generated by the IC. Moreover, this circuit has to operate in an environment where, due to the large number of readout channels, the power consumption has to be minimal. Finally, the central tracker is a detector region that exhibits severe radiation conditions [1, 2]. It is thus required to guarantee a total dose tolerance that can be as high as 10 Mrad over a period of 10 years.

To meet the requirements described before and the tracker radiation constraints, the IC has been implemented using radiation tolerant layout techniques [3] in a 0.25 μm CMOS technology.

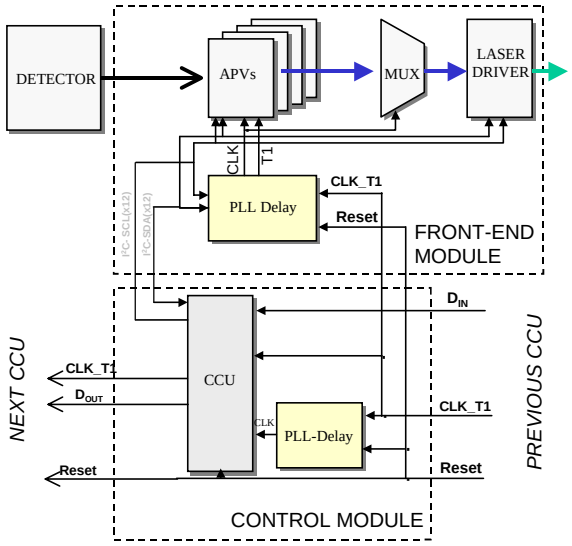

Figure 2 The PLL-Delay IC as used in the front-end and in the control modules of the CMS tracker

2 PLL-DELAY CHIP ARCHITECTURE

Besides the clock recovery and trigger decoding functions, mention before, the developed ASIC (*PLL-Delay IC*) implements phase deskewing for the clock and trigger signals. The clock phase can be adjusted in steps of 1.04 ns (fine deskew) up to a maximum delay of 25 ns, while the trigger signal phase can be delayed up to a maximum of 16 clock cycles also with 1.04 ns resolution.

The major blocks of the ASIC are shown in *Figure 3*, they consist of: a 40 MHz Phase-Locked Loop (PLL), a trigger decoder, a programmable delay line, a calibration

[1] *On leave from INFN and University of Perugia, Italy*
[2] *e-mail:* Alessandro.Marchioro@cern.ch

state machine and an I²C interface that allows programming various parameters in the IC internal registers.

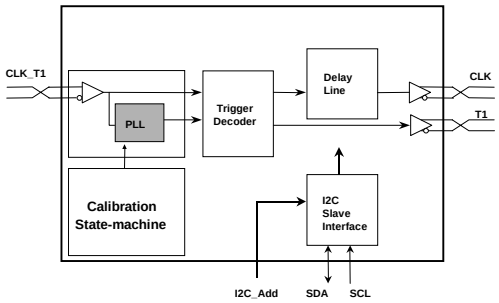

Figure 3 PLL block diagram

The core of this ASIC is the PLL [1,3, 4]; it consists of the following major blocks:

- a double mode digital phase detector, working, during the lock acquisition, as a 3-state Phase Frequency Detector (PFD) and, once lock is achieved, as a 2-state Phase Detector (PD);
- a charge-pump circuit, converting the signals from the PFD/PD into a control current. The charge pump circuit consists of two 10 μA current sources and four switches controlled by the phase detector outputs;
- a loop filter integrating the charge-pump current and controlling the loop dynamics.
- a 12 stage differential Voltage Controlled Oscillator (VCO). To ensure proper power supply noise rejection and also to minimize the generated noise, a differential constant amplitude VCO, similar to the one described in [3], was used. Each stage is a current–controlled differential delay cell. To optimize the jitter behavior of the VCO, a linear relationship between the VCO control voltage and the VCO frequency was implemented. The signal amplitude of the VCO cell is held constant by means of a replica bias circuit and a power supply independent reference generator.

  As shown in *Figure 4*, clock phase shifting is implemented by selecting the output of one of the twelve VCO stages using a multiplexer.

Two conflicting requirements exist in the design of a low jitter PLL. On one hand the smallest possible PLL gain is desirable to ensure the lowest possible jitter in the presence of input noise and of suppressed clock cycles. On the other hand, to cover the whole range of process and temperature variations a high loop gain is necessary to ensure locking. Phase noise filtering is one of the major goals of this design and, consequently, a low loop gain PLL was implemented. In the IC process chosen and with the required low loop gain, it is not possible to guarantee phase locking under all conditions. To circumnavigate this problem a digital circuit implementing an auto-calibration procedure was implemented. This calibration process (to be described later) compensates also for process parameter spreads and device parameter changes due to radiation damages.

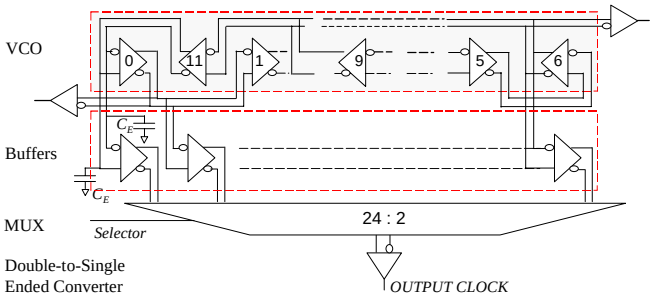

Figure 4 Representation of the clock delay selection

2.1 SYSTEM STABILITY

The loop filter consists of a series, resistor/capacitor in parallel with a smaller capacitor. This last capacitor, is added to mitigate the frequency ripple of a second order loop. It introduces an additional pole in the PLL open loop transfer function

$$G_0(s) = \frac{w_c(1+sT_2)}{T_2 s^2 (1+sT_2/b)} \qquad (2)$$

where, $w_c=K_{VCO}I_pR(b-1)/2\pi b$, K_{VCO} is the VCO gain, $b=(1+C_2/C_1)$, I_p the charge pump current and $T_2=R\,C_1$.

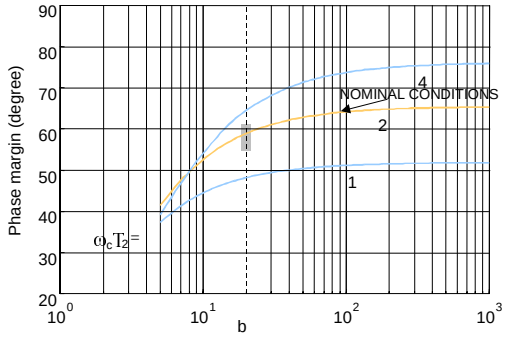

Figure 5 Phase margin of the loop as a function of b parameter. The gray area delimits the variation region of the parameters.

The location of this additional pole must be chosen in such a way that the steady state and the dynamic response should stay practically unchanged. In addition, the presence of this pole has to be chosen to guarantee stability. By inspection of the Bode diagram it was verified that for the chosen design parameters the stability of the system is maintained over the entire range of process parameters, power supply voltages and temperature.

In *Figure 5* the phase margin as a function of b with w_cT_2 as parameter is shown. For small values of b the phase margin becomes small indicating a poorly damped system with a conjugate pole pair close to the imaginary axis.

2.2 NUMERICAL MODEL

Phase Locked Loop circuits are difficult to simulate at the circuit level. The complexity of the complete ASIC and the long time required for the PLL to achieve lock (several microseconds of real time) typically demands prohibitively long computing time (> 24 hours) with tools such as Spice. Therefore, a behavioural discrete time model of the PLL has been implemented allowing quick study of the system design space and optimization of the critical circuit components. A model has been developed and coded in C.

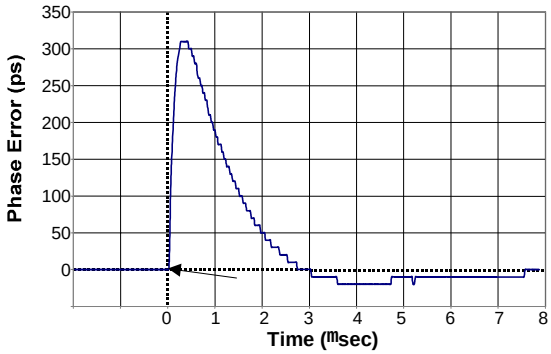

Figure 6 Simulated PLL jitter when a trigger pulse occurs

The system stimulus can be chosen clean or noisy to study the low frequency noise filtering properties of the PLL. Random triggers, i.e. missing clock pulses, can also be programmed in the clock sequence to simulate real LHC conditions. The simulated response to a missing clock pulse is shown in *Figure 6* when filter parameters corresponding to the actual implementation are used in the simulation model.

2.3 AUTO-CALIBRATION PROCEDURE

To accommodate for process variations and devices parameters changes due to radiation damage an auto-calibration procedure has been implemented. In *Figure 7*-(a) it is represented a typical relation between the VCO frequency range and the loop filter voltage. In *Figure 7*-(b) it is represented the type of transfer characteristics implemented in this design. The VCO has a small gain (K_{VCO}) and its operation frequency is a function of the PLL control voltage (V_C) and of an offset current (I_p) such that

$$f_{VCO} = K_{VCO}\, Vc + f(I_p).$$

As can be seen in the picture only some of the curves will allow the PLL to lock at the required 40.08 MHz frequency. Therefore at the start-up (or each time a reset is received) it is necessary to select the suitable locking range. To do this the calibration procedure shown in *Figure 8* is executed.

The offset current (I_p) of the VCO delay cell is initially set to a minimum value (I_p^0) and the PLL is allowed enough time to lock.

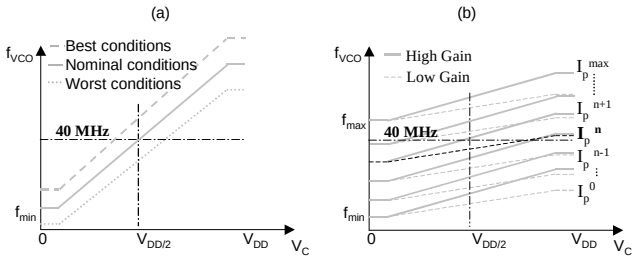

Figure 7 (a) Typical VCO characteristic when power supply, temperature and process variations are considered; (b) implemented VCO characteristic

If the lock is not achieved this means that the VCO is in one of its characteristics curve (*Figure 7*-b) that does not cross the operation frequency and, consequently lock might not be possible. In this case the offset current is increased and the whole process repeated until the circuit is able to acquire lock at the right frequency.

In the case the offset current is set to the maximum value (I_p^{max}) and the lock is not achieved, the PLL gain is increased (*High Gain* mode) and the calibration sequence is started again.

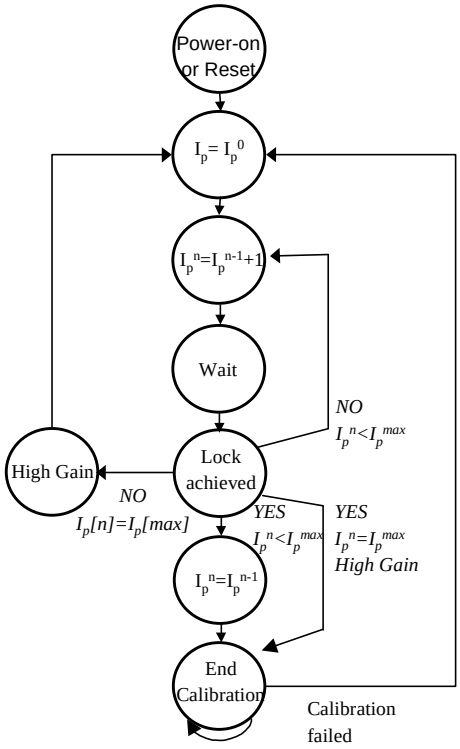

Figure 8 State transition graph for the autocalibration procedure

Once the lock is achieved the phase detector - which up to now has been operating in the phase-frequency mode - is switched to the phase detector only mode.

The auto-calibration process is stopped and all the ASIC functions are enabled.

3 IMPLEMENTATION

The IC has been submitted for fabrication using a 0.25 μm CMOS technology (*Table 1*) and implemented using rad-tolerant layout techniques [5, 6].

Radiation tolerance of integrated circuits is a primary concern in future high-energy physics experiments.

Prototype version in 0.8 μm	*Prototype version in 0.25 μm*
BiCMOS, 2 level of metal, 2 poly	CMOS, 3 level of metal, 1 poly
Power supply=4 V	Power supply=2.5 V
Area $_{\text{Chip core}}$ = 1.6x1.3 mm^2 Area $_{\text{Standard Cell}}$ = A Area $_{\text{Full custom part}}$ = Ac	Area $_{\text{Chip core}}$ = 0.9x0.8 mm^2 Area $_{\text{Standard Cell}}$ = A/8 Area $_{\text{Full custom part}}$ = Ac/2
Available	Submitted for fabrication

Table 1 Technology features

Although radiation hard technology exists, they do no always provide:

- adequate density;
- high volume, high yield and low cost per wafer.

In addition, in a deep submicron technology just because the power supply scales down the power consumption decreases.

On the other hand the ultra thin oxide of deep submicron technologies is inherently tolerant to total dose effects reducing significantly the radiation-induced changes of transistors parameters. Moreover, by employing enclosed geometry and P+ guard-rings around N-channel devices the radiation-induced leakage paths along the edge of the devices and between devices are eliminated.

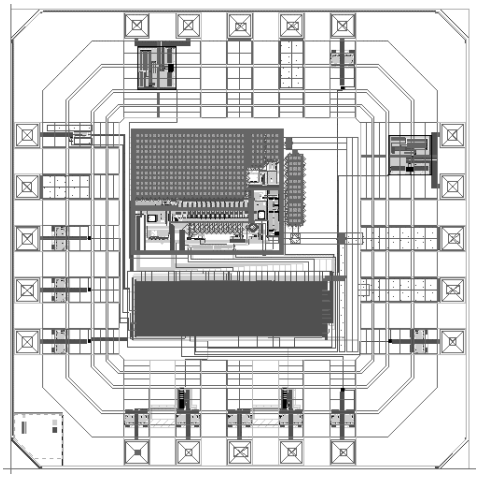

Figure 9 PLL-Delay prototype layout

Simulations and experimental results on test structures demonstrate that the use of standard static architectures should be robust enough not to experience a significant rate of Single Event Upset (SEU) in LHC [7].

Recent results have confirmed the potential of this approach, and have demonstrated design solutions in deep submicron technology that minimize total dose effects and the risk of Single Event Upset (SEU).

A previous prototype version of this IC was fabricated in a commercial 0.8 μm BiCMOS technology [8], resulted in an area of 2.6x2.1 mm^2, where roughly half of the area was used by digital standard cells. In this new version (*Figure 9*) the area occupied by the digital standard cells has been reduced by a factor of 8 while the full custom part is reduced by a factor of 2. Moreover, due to the reduction of power supply voltage the power consumption has been reduced by about 40 %.

4 CONCLUSIONS

A PLL-Delay ASIC for clock recovery and first level trigger decoding in the CMS tracker has been designed. The IC has been submitted for fabrication using a standard 0.25 μm CMOS technology with a rad-tolerant layout. The ASIC provides a clock signal with adjustable phase in steps of 1.04 ns and a trigger signal with phase programmable in multiples of the clock period. An auto-calibration circuit is used to obtain low jitter avoiding dependency on process and radiation induced damages. A numerical PLL model was implemented to study the dynamic behaviour of the PLL and to allow optimization of the loop parameters.

5 REFERENCES

[1] A.Marchioro et al. "*A system for timing distribution and control of front end electronics for the CMS tracker*", Third Workshop on Electronics for LHC Experiment, London, 1997

[2] For complete references on the RD12 project, see http://www.cern.ch/TTC/intro.html.

[3] F. Faccio, *Total Dose and Single Event Upset Measurements of Test Structures in a Deep-Submicron Technology*, Fourth Workshop on Electronics for LHC Experiments, Rome, September 21-25, 1998.

[4] I. Young et al., " *A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors*", IEEE Journal of Solid State Circuits, vol. SC-27, November 1992, p.1599

[5] B. Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuit*, IEEE Press, New York 1996

[6] G. Anelli et al., *Total Dose behavior of submicron and deep submicron CMOS technologies*,

[7] K. Kloukinas et al., *Development of a radiation tolerant 2.0 V standard cell library using a commercial deep submicron CMOS technology for the LHC experiments*, Fourth Workshop on Electronics for LHC Experiments, Rome, September 21-25, 1998.

[8] P. Placidi et al., *A PLL-DELAY Asic for clock recovery and trigger distribution in the CMS* , Third Workshop on Electronics for LHC Experiments, London, September 22-26, 1998.