TESTABILITY ISSUES IN THE CMS ECAL UPPER-LEVEL READOUT AND TRIGGER SYSTEM

Carlos Beltrán Almeida, INESC, Lisboa, Portugal (email: cfb@inesc.pt)
Isabel Cacho Teixeira, INESC/IST, Lisboa, Portugal (email: ict@inesc.pt)
Joao Paulo Teixeira, INESC/IST, Lisboa, Portugal (email: jct@inesc.pt)
Joao Varela, CERN/LIP, Geneve, Switzerland (email: Joao.Varela@cern.ch)
José Augusto, INESC/IST, Lisboa, Portugal (email: jasa@dalton.inesc.pt)
Marcelino Santos, INESC/IST, Lisboa, Portugal (email: mabs@inesc.pt)
Nuno Cardoso, INESC, Lisboa, Portugal (email: nmvc@abaco.inesc.pt)

Abstract

This contribution describes the work carried out by the INESC team, in collaboration with LIP, in order to increase testability features on the CMS ECAL upper-level readout and trigger system. To accomplish this purpose, (1) extension of boundary scan test of electronic boards to system level, (2) introduction of self test in ASICs, (3) defect-oriented test effectiveness evaluation and (4) system-level modeling and simulation have been addressed and are reported. This work is consistent with the one carried out by Politecnico di Torino and CAEN in collaboration with CERN, in order to improve testability and reliability of the upper-level readout and trigger system.

1. INTRODUCTION

The CMS ECAL upper-level readout and trigger system [1] is composed of about one thousand boards installed in sixty 9-U VME crates. The complexity of the design and implementation of such a system requires the use of Design for Testability Techniques (DFT), in order to achieve a testable system during all the phases of its lifetime.

In collaboration with LIP, INESC has been evaluating the implementation of the ANSI IEEE 1149.1 Standard at different modelling levels (component, MCM, board, system), the inclusion of self-test techniques and in-system test procedures, as well as the specification of the system with a high level modelling technique.
Based on this study, a proposal of extending the use of the IEEE 1149.1 standard to system level emerged. To accomplish this goal, a boundary scan controller board is being designed. The architecture and the main features of this board are described in section 2.
The introduction of Built-In Self Test (BIST) in components, namely ASICs, and test effectiveness experiments are reported in section 3. A BISTed version of the synchronisation `Tx/Rx` IC, under development by TECMIC, is presented. Section 4 introduces the concepts behind a high level modelling technique used to specify the system. Finally, section 5 summarises the main conclusions.

2. APPLICATION OF BOUNDARY SCAN AT SYSTEM LEVEL

The upper-level readout and trigger system is controlled, during the normal operation of the acquisition system, by a controller board housed in each crate. The main objective of this task is to develop a VME based JTAG controller (hardware/software) enabling the application of a boundary scan test to the sub-system crate during idle time or when a maintenance operation is required.
This task has two components:

A. Development of a boundary scan test module – boundary scan controller board - being the interface between the sub-system controller and the VME dedicated lines to implement the IEEE 1149.1 test bus.
B. Development of the software for downloading the test and for getting back to the controller the test results.

2.1 Architecture of the Boundary Scan Test System

There are two main approaches to interconnect the test bus of a system composed by several IEEE 1149.1 compatible boards: the ring configuration and the star configuration. The ring configuration, figure 1a), uses the same control signals (TMS and TCK) for all boards and a single scan path in series with all the boards (TDI/TDO). The star configuration, figure 1b), uses also the same control signals for each board and a common TDI/TDO. Both configurations require the same amount of information to control and test the entire system. However, the ring configuration has a scan chain longer than the star configuration. This configuration has some advantages over the first one, requiring less test clock periods to get the test response. Moreover, if one board is removed or is faulty, the controller will still be able to

test the system. Hence, the star approach was selected for implementation.

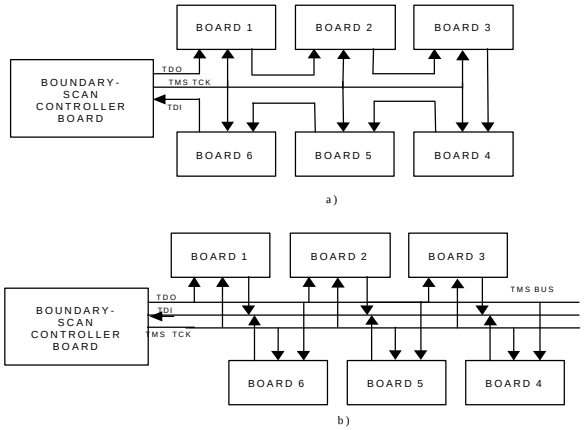

Figure 1 – a) Ring configuration; b) Star configuration.

The star configuration requires the use of a special device, called *Scan Bridge* [2], to interface each board with the test bus. This device, developed by National Semiconductor, has one 1149.1 test port connected to the backplane test lines and three 1149.1 secondary test ports connected to a maximum of three local scan chains. Addressing one of these circuits in a system allows testing a particular board in the system. Unlike other approaches (for example, the MTM bus standard), the *Scan Bridge* provides an addressing scheme using a 1149.1 compatible protocol.

2.2 Boundary Scan Controller Board

The Boundary Scan Controller Board under design is a VME bus slave board with dimension 6U. This board will interface the VME bus using the P1/J1 and P2/J2 connectors, which include the test and maintenance signals [3], namely the MCLK (Module Clock) equivalent to the signal TCK of the IEEE 1149.1 standard, MCTL (Module Control) equivalent to TMS, MMD (Module Data) equivalent to the signal TDI, MSD (Module Slave Data) equivalent to the signal TDO and MPR - bus pause request (TRST#). These signals are used to apply the boundary scan test at system level.

The boundary scan controller board receives VME bus commands, generated by the master VME board, to download and configure the test procedure, and drives the 1149.1 test signals in order to apply a boundary scan test to a single board inserted in the VME backplane.

As depicted in figure 2, the controller board contains the following functional blocks:

VMEbus Interface Circuits - These circuits, used to interface with the VME bus, implement the VME64 bus protocol to transfer data between the master board and the slave board. The loading of the local memory and the configuration of the local registers are done using the VME64 data transfer protocol.

Local Test Controller (LTC) - This circuit, implemented by a programmable logic device (PLD from ALTERA), is responsible for controlling the functionality of the test board. This circuit is divided in four sub-modules:

Test Control State Machine - State machine that controls the state of the board and the execution of the tests.

VME Circuits Configuration - Module responsible for configuring the operation mode of the VME bus interface circuits.

Data Transfer Controller - Module that manages the data transfer between the local memory, the boundary-scan controller (PSC100F) and the LTC itself.

Status/Instruction/Configuration Registers - Registers accessed by the VME bus master board, that allow to start and to stop the running test, and to monitor the current state of the test.

Local Memory - This memory is divided into two parts. One, stores the serial output test vectors (bit patterns for TDO and TMS) and the input vectors captured during the test execution (TDI bit patterns). The second part contains the state of the TRST# and other control data concerning the test flow.

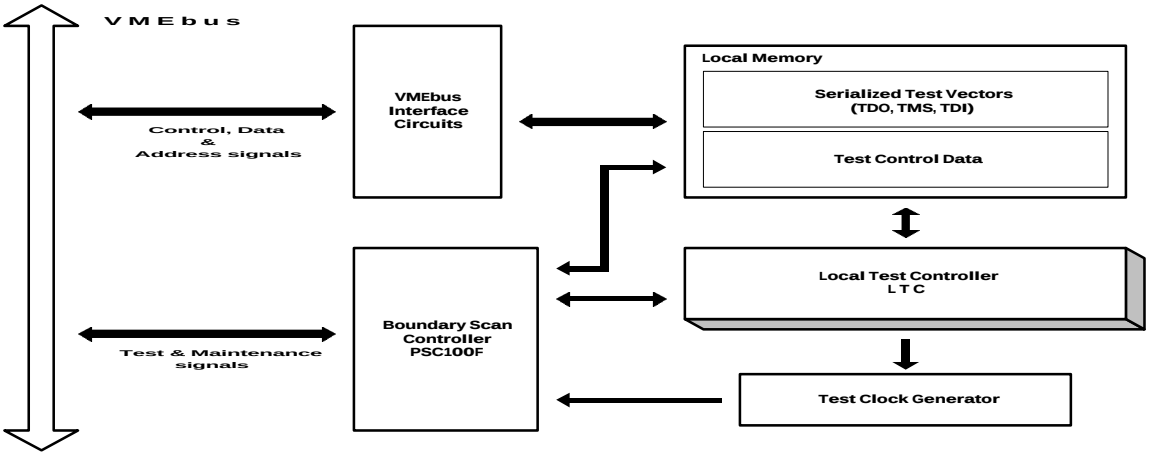

Figure 2 – Block diagram of the boundary scan controller board.

Boundary Scan Controller (PSC100F) - This circuit, developed by National Semiconductor [4], is designed for interfacing a parallel processor bus with the serial boundary scan test bus. The circuit is divided in a serial interface, that includes a buffer for each of the test signals (TDO, TDI and TMS), and in a parallel interface accessed by the Local Test Controller.
Test Clock Generator - This programmable clock generates the test frequency applied to the TCK test signal. The generator is programmed by the LTC.

2.3 Boundary Scan Controller Software

Tests are generated for each board with the TERADYNE's VICTORY software package [5]. This software is currently in use at CERN and will be re-used when generating the test for each board in the system level configuration. All VICTORY modules generate test vectors in SVF (Serial Vector Format), widely accepted by suppliers and users of boundary-scan test tools. The VICTORY software package includes a toolkit that allows the conversion of SVF code into a truth table containing the logic levels of the five test signals. Software to be developed will transform that truth table into a format suitable to download into the Boundary Scan Controller Board. The software is also responsible for configuring the board registers.

The VICTORY software package includes also a diagnostic tool (BSID) that uses the test results to diagnose eventual failures in the system. The Boundary Scan Controller Board software will convert the test results to a format suitable for the diagnostics tool.

3. ASIC BIST, QUALITY AND RELIABILITY

A second area of R&D includes the INESC support for test and reliability of key system components, namely a synchronization circuit, the Sync Tx/Rx [6]. A FPGA prototype of the circuit was under development by TECMIC, and must include testability features, namely BoundaryScan (BS) [7] and Built In Self Test (BIST). The final version of the IC is to be implemented using ASIC (Application-Specific IC) technologies; hence, the envisaged solution should apply to both layout styles. Here, we present some relevant aspects of the proposed solution [8] (Fig. 3).
BIST, combined with BoundaryScan, allows the IC self-test without the need to load complex data patterns and without the need to analyze individual circuit output. In BIST operation mode, the circuit automatically generates test patterns (through Linear Feedback Shift Registers (LFSRs)) and compresses its outputs. These compressed outputs, referred as *signatures*, are serially shifted out when the test ends and then compared with the fault-free circuit signature. BIST capability is relevant for production and lifetime testing, especially for complex, not easily accessible system modules, like the ones to be expected in the CMS electronics.

The proposed 1149.1 BS [7] architecture comprises:

- loop 0 - a boundary-scan register loop made of Boundary Scan Cells (BSCs),
- loop 1 - a test register (TR) loop with
  - two LFSRs and
  - the Sync Tx/Rx Status Register,
  - Data error counter,
  - Synchronization error counter;
- a TAP (Test Access Port) controller with
  - an instruction register (IR),
  - a bypass register (BP R) and
  - a controller (JTAG [7] state machine);
- a BIST controller
- a LFSR and EDC (Error Detecting Code) encoder

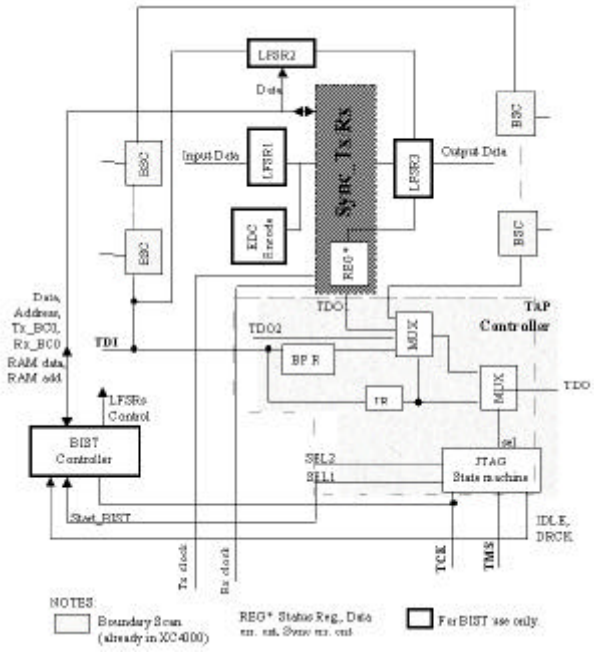

Fig. 3 - BISTed version of the Tx_Rx ASIC.

LFSR1 (Fig. 3) generates the Input Data without the Hamming Code for the BIST session. The EDC Encoder generates the bits with the Hamming code. The Sync_Tx Input Data must be clocked and multiplexed by the BIST Controller, in order to allow normal (transparent) operation or LFSR stimuli injection. LFSR2 is used for signature analysis (SA) of the data stored in the Accumulator during each Read Accumulator cycle of the BIST session. LFSR3 is used for SA of the Sync_Rx Output Data. These LFSRs are transparent in circuit normal operation. Loop 1 must include also the Status Register, Data Error Counter and Sync. Error Counter as part of the signature of the circuit BIST operation.

An interesting feature of the proposed solution has to do with time requirements. The JTAG/IEEE1149.1 specification [2] requires that testing should be performed under control of a test clock TCK, independent of the main system clock. In general, system clocks (Tx and Rx_clock) should be interrupted and test clock TCK applied. However, for this synchronization ASIC, this clock gating has several disadvantages:

- introduction of delays in Tx and Rx_clock,
- important area overhead due to the required clock signal buffering and
- BIST speed limitation to the TCK rate (much smaller than "at speed" operation).

The proposed alternative (not fully compliant with 1149.1), is to fed system clock pins directly to the on chip system logic as they would be during non-test operation of the component. The deviation from the 1149.1 standard is due to BIST other than TCK clock requirements. However, all other BIST interface is kept 1149.1 compatible. Tx_clock must clock LFSR1 and 2; Rx_clock must clock LFSR3. Implementation details, namely for Xillinx™ XC4000 FPGA devices, are given elsewhere [9]. The FPGA prototype realization of the Tx_Rx synchronization IC is currently being carried out by TECMIC. The 40 MHz operation speed has been the main implementation problem in the FPGA technology; nevertheless, the problem can be easily solved in ASIC technologies, like GA (Gate Array) technologies. A standard cell design will be performed by INESC.

A complementary question to test generation and application is product quality and reliability. Product quality is usually measured by the Defect Level [10], defined as the percentage of defective devices that pass successfully the production test and thus are built into the numerous PCBs of the ECAL system. Reliability is a key factor of success for the CMS experiment, as long lifetime and low down-time are system specifications. Both issues are associated with the ability to predict and monitor the impact of physical defects, induced during IC manufacturing or lifetime operation, on IC behaviour.

The INESC QTHS Group [11] has developed a Defect-Oriented (DO) methodology and tools that allow layout dependent physical defect extraction, sampling and simulation, using `lobs` and `VeriDOS` tools [12,13]. In order to show the usefulness of the approach for the CMS electronic system, a preliminary experiment was carried out with CAEN using a module of the Level 1 (L1) filter.

The module is the filter tap, comprising a carry save multiplier and adder working at 40 MHz. It has 79 PIs, 54 POs (with registers), and was laid out using a commercial 0.8 µm CMOS technology. The module has 1368 logic gates and uses 21 library cells. A standard ATPG (Automatic Test Pattern Generation) tool generated 108 test vectors that cover 100% single Line Stuck-At (LSA) faults. However, BRI (bridging) and LOP (line-open) realistic fault extraction reveal 14,624 physical defects, likely to occur (the `lobs` tool computes their probability of occurrence, based on critical area evaluation and defects statistics data). Fault simulation results are shown in Fig. 4. Here, DC stands for Defects Coverage, which is the weighted percentage of defects uncovered by the LSA test set.

Fault class	FI (%)	DC (v) (%)	DC (I) (%)	DC (v+I) (%)
BRI Y-Y	54.55	98.05	0.93	98.98
BRI A-B	17.09	88.40	11.60	100.00
BRI A-Y	7.83	97.23	2.77	100.00
BRI Y-x	4.35	85.22	14.78	100.00
BRI x-Vdd	0.77	69.50	30.50	100.00
LOP A-Y	9.65	99.24	0.0	99.24
LOP Y-Vdd	0.92	100.0	0.0	100.00
LOP x-Vdd	3.94	97.23	0.0	97.23
total	100.00	95.57	3.69	99.26

Fig. 4 - L1 Filter Defects Coverage (DC) results.

Results clearly show that 100% coverage of LSA faults does not guarantee 100% DC. In fact, using logic (voltage) detection only, DC(v)=95.57%. For certain classes, v-detection is quite low, as it is the case of BRI A-B (between logic gate inputs) and BRI x-Vdd (between gates internal nodes and power supply nodes). Fortunately, the Fault Incidence (FI) of some defects, like BRI x-Vdd, is low. Additionally, current (I_{DDQ}) detection is shown to be very important, if high DC is required. Additional test effectiveness evaluations will be carried out for the ECAL electronic system.

4. SYSTEM-LEVEL MODELING AND SIMULATION

Another aspect of INESC collaboration on CMS experience is related with the need to assess the coherence and completeness of technical specification against system requirements [1]. To achieve this goal, high level specification models have been used, that not only allow that assessment but also are a vehicle to test communication protocols under different possible architectures [14]. For accomplishing this purpose, a high-level model of the ECAL Front - End and Trigger Primitives Generators has been developed [15]. Beyond functionality, this model has focused on timing constraints and communication requirements among the different modules that constitute the system under consideration. CASE tools, Rational Rose [16] and Objectime [17], have been used for model development.

Objectime allows the animation and simulation of different aspects of system behavior. Additionally, it automatically generates sequence diagrams corresponding to envisioned scenarios of execution. These diagrams are, in fact, graphic representations of protocol dialogs among the different components (objects) that model the system. It is possible to assign time (real or virtual time) to those dialogs, and consequently, to test the correctness of a given protocol against timing requirements. If timing requirements are not fulfilled, the modification of either the protocol or the architecture and the evaluation of the impact of those modifications in system behaviour are straightforward.

The use of these models may save considerable development time and efforts since, in most cases, there is not a need to use (and develop) physical prototypes to test different solutions. Models are independent of the implementation; therefore, architecture components or modules can be finally implemented in hardware, software or both.

5. CONCLUSIONS

A Boundary Scan Test Board Controller providing an hierarchical test application compatible with IEEE 1149.1 standard was proposed.
It was shown that product quality and reliability, as well as monitoring through its lifetime, can be enhanced by combining 1149.1 (BS) and BIST at component level, and by evaluating, in the IC design environment, test effectiveness. This was carried out with a BISTed version of the Sync Tx/Rx ASIC, under development by TECMIC, and with the evaluation of the ability of a LSA test to uncover physical defects likely to occur in the L1 filter IC, being developed by CAEN.
The complexity of the hardware/software system, under development by a large design team located in different sites, and with very different backgrounds, clearly points out the usefulness of using system level modeling techniques and simulation to monitor the coherence and completeness of the technical specification and to validate its implementation. This has been shown through the development of models of the ECAL Front - End and Trigger Primitives Generators.

6. AKNOWLEDGEMENTS

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