

# Generic hardware for DAQ applications

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## Abstract

In the context of large data acquisition systems (DAQ) for LHC experiments, flexible and uniform interfaces between subsystems is a key feature to ensure best possible system integration/maintainability and a clear system upgrade policy. This approach is widely used in CMS at the border between sub-detectors front-end and the DAQ. Common requirements and reconfigurable hardware used in CMS DAQ are presented in this article.

## 1. Introduction

A basic block diagram of the CMS DAQ is shown figure.1. Its constitutive elements are the detector front-end, the trigger logic, the readout units (RU), the event builder, the event filter units (EFU), the computing services, and the event manager.

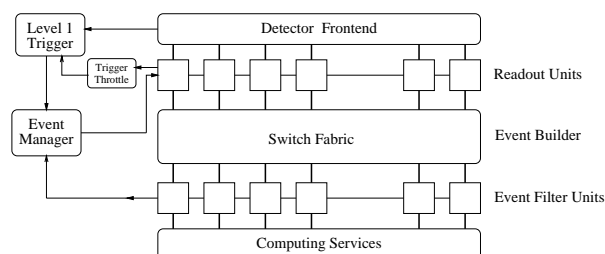


Fig. 1. CMS DAQ block diagram

The front-end electronic acquires data every bunch crossing and the trigger logic selects the data to be sent to the readout units. A readout unit is constituted of 1 DPM and several Detector Dependent Units (DDU). A DDU is controlling the associated front-end electronic and receives the trigger selected data. As a DDU is receiving data on several data links, a data packet is built locally (DDU event). The DDU event is kept available for the DPM. As a DPM is reading out several DDUs, a DPM event is also built. Then the DPM event (also called Event Fragment) is sent through the event builder to the requesting EFU. The association of the RU with an EFU is the task of the event manager.

## 2. Interfaces and standardization

The DAQ is the natural convergence point of the data produced by the sub-detectors. In the case of CMS, there will be about 12 different data sources providing data to the DAQ. Interfacing these sources with the DAQ is a critical point given the overall size and complexity of the final system (on-detector electronic, counting room electronic and DAQ). Reducing the diversity in the electronic devices is a valuable approach regarding the system integration (especially during the initial debug phase) and later the maintenance/upgrade operations.

Looking at hardware interfaces between heterogeneous systems, one can find a generic architecture often encountered in DAQ applications (see figure 2).

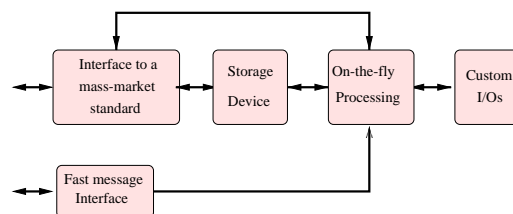


Fig. 2. Generic interface architecture

As soon as a "popular" hardware has to drive (or be driven by) a specialized one, this generic architecture is used (with some variations).

The DDU, part of the Readout Unit (see figure 3), can be seen as the interface between the DAQ and the sub-detector readout systems. Below the DDU, no sub-detector specific hardware is foreseen in the DAQ architecture. The task of the DDU is to deal with a given sub-detector with its specificities on one side and make available the data on the Front End Bus (FEB) according to its specification/protocol on the other side. More informations about the DDU functionalities are available in [1].

The principle of a common DDU for all sub-detectors in CMS is proposed for a long time now. A common functional specification document [1] is adopted by all CMS data producers. The next step is to study the feasibility

of a common hardware platform that can suit the sub-detectors needs. Architecturally speaking, the part of the DDU in touch with the FEB can be common for every sub-detectors both at the functional and physical level. Regarding the sub-detectors, two families can be distinguished: analog detectors and digital detectors. Concerning the analog detectors (Pixel, Silicon and MSGCs), a unique hardware development is underway and made by the Rutherford Appleton Laboratories [2]. The standardization is eased by the fact that the detectors are using the same data link and/or Front End chip [3]. About the digital detectors, the situation is not as easy due to the fundamental differences between detectors. However, the CMS DAQ group designed a versatile board that has been first used for specific DAQ applications. But during the design phase, special care have been taken to allow other applications outside the DAQ area to be implemented: especially DDU-type applications were considered. In the next parts of the article, the generic block diagram of a DDU will be shown and compared to the block diagram of the versatile DAQ board. Then a quick overview of the different applications running on that board will be listed and finally, the next generation of versatile board, currently in the assembly/debug phase, will be presented.

### 3. Generic DDU

As reminded before, the DDU is in charge of interfacing a sub-detector environment with the central DAQ environment. One part of the DDU deals with the sub-detector specificities and the other part deals with the so-called FEB. This later part must be common for all sub-detectors on the functional level and can be common on the physical level. Architectural/functional flexibility is a major feature of the common part as the DAQ will follow the technological evolution of the telecommunication industry during its life time. Therefore, reconfigurable logic (FPGAs) and a layered approach are used wherever it is possible.

Generically speaking, the DDU must acquire the data of the FES, control/manage the FES and make available the data on the FEB after a specific processing (if any). The data encapsulation format and the communication protocol with the DAQ will be unique through CMS. The DDU generic block diagram is shown Fig.3.

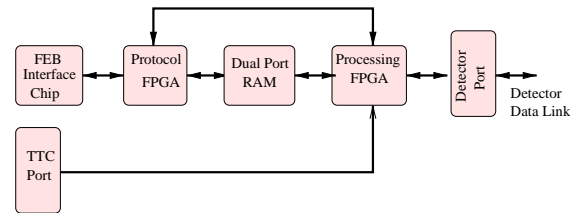


Fig. 4. Generic DDU block diagram

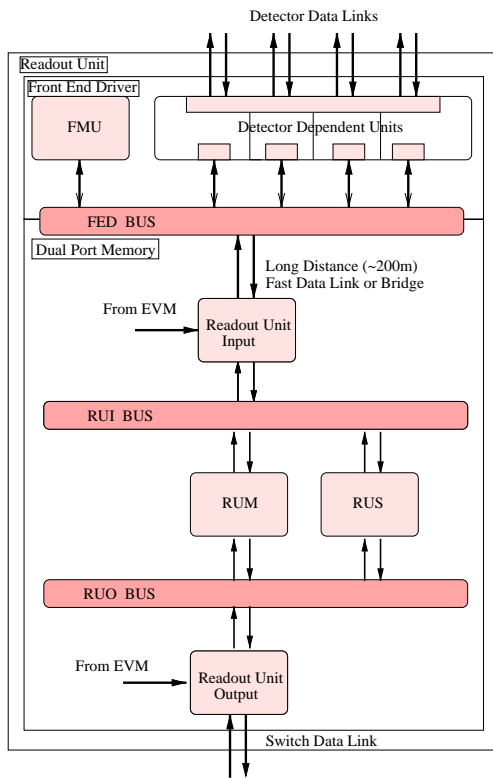


Fig. 3. Readout Unit Structure

### 4. Generic DAQ platform

A DAQ hardware platform has been designed and developed last year in order to provide a prototyping facility for testing other DAQ boards (mainly the Dual Port Memory [4]) and evaluate architectural options within the CMS DAQ project.

#### 4.1 Description

The architecture of the board features total reconfigurability thanks to the on-board FPGA (50Kgate-equivalent) 100% available to user-application. The FPGA [5] is linked on one hand to a commercial PCI interface [6] (initiator and target) and on the other hand to a 77 pins user port through bi-directional TTL drivers. The drivers are fully controlled from the FPGA allowing custom I/Os to be implemented. The FPGA has also access to 32 KBytes of nvRAM. Finally, the same access port to the TTC signals defined by RAL has been implemented on the board.

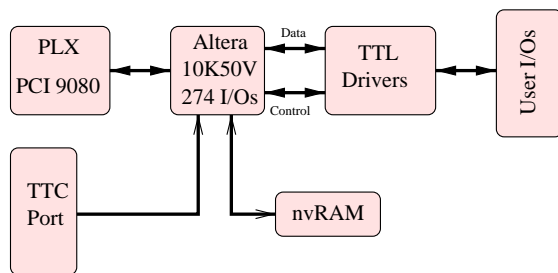


Fig. 5. DAQ generic platform block diagram

This architecture allowed numerous applications to be developed. Detailed description and engineering documents are freely available on the WEB [7] to anyone interested by such hardware.

## 4.2 Applications

- **DPM exerciser**  
In the previous version of the DPM named P25++, the data input port was a custom development and the output port was a standard PCI. The generic board has been programmed to readout data through the output port (the generic board was initiator of the DMA) and to reinject these data into the input port. The data were cycling at 128 MB/sec. sustained (97% of the maximum possible performances of PCI 32bit/33MHz)
- **DDU emulator**  
Always with the P25++, the generic board has been configured to emulate a DDU. Under the control of the PCI bus, the FPGA was translating on the fly a PCI data stream (DMA) to the input format of the DPM. The throughput was again close to the maximum PCI speed.
- **FERA to PCI interface [8]**  
The generic board is in charge of transferring the data on the FERA bus (Fast Encoding and Readout ADC developed by Lecroy Corp.) to the PCI bus by means of DMA. The PCI destination address is controlled via a register in the FPGA.
- **Trigger interface for CMS Muon chamber [9]**  
For test beam applications, the board is used to interface the chamber readout system on PCI with the beam signals (spill, trigger). The busy and veto signals are controlled by the board.
- **Fast Messaging network based on IEEE-1394 [10]**  
Still under design, it is an extension of the previous application to several PCI based readout units. The

network is Firewire at 400Mbit/sec. The triggers are tagged and broadcasted to all readout units to ensure the correct event fragments to be merged during the event building process. For that, a transition module has been developed to house the Firewire hardware: it plugs directly into the user connector.

- **Myrinet protocol monitor [11]**  
For LHC DAQ systems, one major piece of equipment is the event builder. The most likely implementation of the event builder is based on a multi-stage switch fabric. If the behavior of an individual switch can be measured and simulated, the behavior of a switch fabric is much more difficult to study. In order to understand what is going on in the hardware, a protocol monitor is often needed. This device allows to measure the basic parameters of the device and allow to define the simulation constants needed to tune the software model. Moreover, it helps to interpret/explain some measurements when the architecture and the test setup is getting complex, and it is the case! For CMS, one candidate is a switch from Myricom [11]. A spy/monitor based on the generic board is under development. A pre-processor board is plugged on the user connector to allow the interfacing with the low-level layers of the switch protocol. The FPGA extracts the features of the messages (destination, length, status, flow-control, time tags...) and stores them into the nvRAM. A visualization software then acquires them and process them for display and statistics.

Given the comments of the different users and the technology improvements, the need for hardware flexibility (especially for the user connector), more storage capacity and faster FPGA/PCI interface triggered the development of a new generation.

## 5. New generation of the DAQ platform

Compared to the previous version, it features:

- PCI 66MHz, 64 bits capability
- On-board 32 Mbytes SDRAM
- 800MBytes/sec. internal bandwidth
- 300Kgate-equivalent FPGA
- 148 pins high performance port for custom hardware
- JTAG support for BSCAN and FPGA configuration

The choice of the GT64120A from Galileo [12] as PCI interface enables the fastest speed on PCI (524 MBytes/sec. peak) and the usage of huge, inexpensive memory

chips (100 MHz SDRAMs). The FPGA is a Virtex 300 (the new family from Xilinx [13]) providing the equivalent of 300K logic gates.

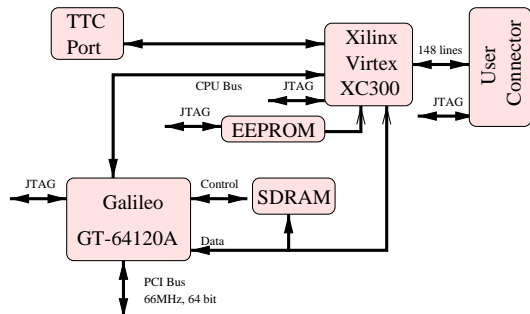


Fig. 6. Core board block diagram

Due to BGA technology used for the two previous chip, IEEE-1149.1 (JTAG) had to be implemented for test/debug purposes. The FPGA and its configuration EEPROM are compliant to IEEE-1149.1 and integrated in the JTAG chain as well. Finally the JTAG chain is available on the user connector to allow the test/debug of the application specific hardware extension. Each chip can be removed separately from the chain if the shifting time becomes "long". This feature allows also individual debug if needed. The access to the JTAG chain is either local from an on-board tap or from the PMC connectors, hence allowing remote test/debug/reconfiguration.

To increase the flexibility at the hardware level, instead of providing a connector with fixed drivers and terminations (solution adopted in the first generation), all the remaining free pins of the FPGA are available on high performance/high density connectors (Matched Impedance Connector family from AMP [14]) where a specific extension board can be plugged. Hence, the platform can match exactly the requirements of the specific application by developing only an extension module.

The form factor of the core board is PMC. With its extension, the PMC specs. are violated but still allows the operation in a standard PMC slot. Mictor edge to edge connectors are available and would allow to match the PMC form factor but the cost and minimum quantities of such connectors are dissuasive for prototyping! Again, the RAL TTC access port has been implemented but now, the FPGA has the capability to drive these lines if the application requires it: bidirectional LVDS drivers fully wired to the FPGA have been implemented on-board. This feature opens a full range of new applications that were not possible with the first generation of generic boards. As with the first generation, engineering files along with component specifications are freely

available at [7]. When the board will be fully operational, access to CAD files under Cadence will be also given.

## 5.1 Foreseen and potential applications

- The first application to be ported on that generic board will be a 200m-400MByte/sec. data link. Such performances are required to implement the so-called "DAQ link" in CMS (this link goes from the DDU's located in the underground counting rooms up to the RUM located in surface buildings along with the switch and the filter farm).
- Protocol analyser/monitor  
A faster and more powerful Myrinet analyser may be ported on the new platform. In the near future, Myrinet will more than double the speed of their link and the first board will be saturated immediately with the high speed traffic.
- Level 1 Accept generator/Control networks  
As the DAQ test setup evolves towards the final architecture, trigger generation devices and fast control networks must be developed in order to exercise the setup under more realistic conditions. The versatility of the new generation enables these developments.
- Front-End data fan-in/fan-out  
For low/high occupancy detectors, data may need to be multiplexed/demultiplexed before/after the FEB. This is needed to use the FEB bandwidth in an efficient way or reduce the load to a small part of the switch: this can be done by such board, re-designing only the extension.
- Finally, the board can be the core of a unique digital DDU (to reach the same situation as with analog detectors in CMS) or a general prototyping platform to get familiar with high speed PCI, to implement exotic interfaces to PCI... Whatever you can imagine!

## 6. Summary

In a first part, steering principles for sub-detector/DAQ communication are presented. In order to ease system integration, the concept of a uniform interface for all sub-detectors has been adopted for CMS. A set of minimum requirements has been established and a common implementation for these minimum requirements is proposed. This standardized approach will ease the integration, the debug, the maintenance and the upgrade of the

system with minimal resources consumption (financial and human).

In a second part, reconfigurable hardware platforms developed by the CMS DAQ group are presented. Thanks to the on-board programmable logic, these platforms are used by the sub-detectors but also by other groups to develop their specific applications. An overview of these applications is given.

Finally, the latest generation of the platform is presented. The versatility of the platform has been increased by using extension boards where application specific hardware can be added. A 200m-400MB/s data link based on this platform will be the first practical application.

## 7. References

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