Use of Programmable Logic in a Pipelined Trigger for ATLAS

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Abstract

We present an overview of the Jet and Energy Sum processor for the ATLAS Level-1 Trigger. The design system is based on the use of commercial off-the-shelf components, including large programmable logic devices. The architecture of the system is discussed, including implementation details that reduce latency and board complexity, and take advantage of the inherent flexibility in the design. The results of technology demonstrator programs confirm the feasibility of key elements of the processor design.

1. INTRODUCTION

The programmable logic industry has seen rapid development in recent years. Currently available programmable logic devices offer hundreds of thousands of usable gates, hundreds of user-definable I/O pins, system performance well over 100 MHz, and compatibility with a variety of I/O signal standards. These advances have been accompanied by reductions in price, making in-system programmable logic a serious alternative for applications which have previously favored ASIC solutions.

The advantages of using programmable logic are well understood. Prototyping cycles take hours or days, rather than weeks for ASICs. Belatedly discovered errors can be easily fixed, and system functionality can be modified or enhanced as requirements change. Programmable logic devices are fully tested at the factory, effectively providing 100% device yield. Finally, in-circuit programmability allows "design multiplexing", where different functions (such as data taking and diagnostics) may be performed in the same logic, reducing the number of gates needed.

The Jet/Energy Sum processor system for the ATLAS First Level Calorimeter Trigger is a multi-crate trigger processor system designed to be built using FPGAs and other commercial off-the-shelf components. FPGAs are used to calculate transverse and missing energy in the calorimeter, identify energy clusters for use in jet calculations, send information for use by the Level-1 and Level-2 triggers, and read out time slice data to DAQ for trigger validation purposes.

In this paper, we present an overview of the proposed system, followed by implementation features which enhance performance, simplify the design, and exploit the flexibility of the system. Finally, we present results from technology demonstrator programs that have been used to validate key features of the system.

2. SYSTEM OVERVIEW

2.1 The ATLAS Level-1 Trigger

The organization of the ATLAS Level-1 trigger is presented in Figure 1. Data from the calorimeters and muon detectors are transmitted to respective trigger processors, which identify and count electron, tau and Jet candidates, calculate total and missing transverse energy, and reconstruct muon trajectories. The processors send results from every bunch crossing to the Central Trigger Processor (CTP) which makes a Level-1 Accept (L1A) decision based on them. If the CTP issues a L1A, the processors read out more detailed information on the types and locations of event features to the Region of Interest (ROI) Builder for use by the Level-2 Trigger.

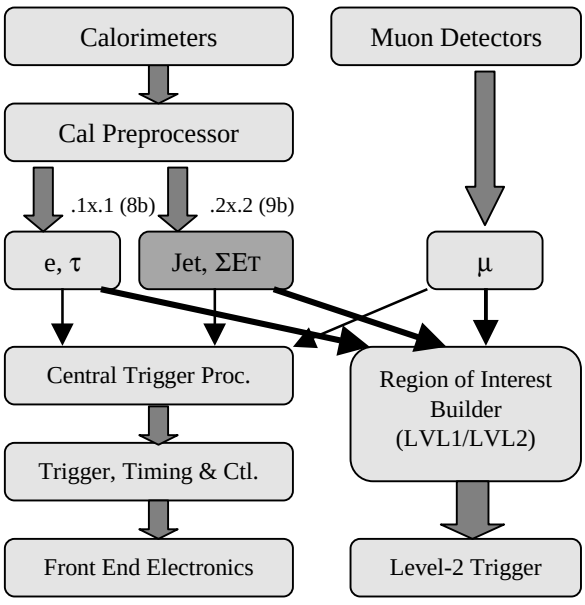

Figure 1: Organization of the ATLAS Level-1 Trigger

In the calorimeter trigger, analog trigger tower sums are first received and digitized by the Calorimeter Preprocessor system before being passed to the e/τ Cluster Processor and the Jet/Energy Sum processor. Eight-bit electromagnetic and hadronic trigger tower energies with 0.1x0.1 η/ϕ granularity and the correct bunch crossing are transmitted to the Electron/Tau cluster processor, while 9-

bit Jet elements with 0.2x0.2 granularity are sent to the Jet/Energy Sum Processor.

2.2 The Jet/Energy Sum Processor

The Jet/Energy Sum trigger space consists of 960 Jet elements in the range $-3.2 < \eta < 3.2$, as well as extra energy sums from the forward calorimeters. The system is subdivided into four quadrants in ϕ, which are each covered by a separate set of Jet/Energy Sum Modules (JEMs). Jet elements near the border of adjacent quadrants are duplicated in the preprocessor and sent to JEMs in both quadrants to provide the environmental information needed by the Jet algorithm.

Each JEM (Figure 2) receives 9-bit Jet element energy sums in 25 ns intervals via 400 Mb/s serial links (National Semiconductor LVDS). The demultiplexed input data are transmitted at 40 MHz to Energy Sum FPGAs, which sum the electromagnetic and hadronic energies. The E_T, E_X, and E_Y, of each Jet element are calculated, and sums of these are transmitted to adder trees on a separate FPGA, which merges the results and transmits them to the Sum Merger Module.

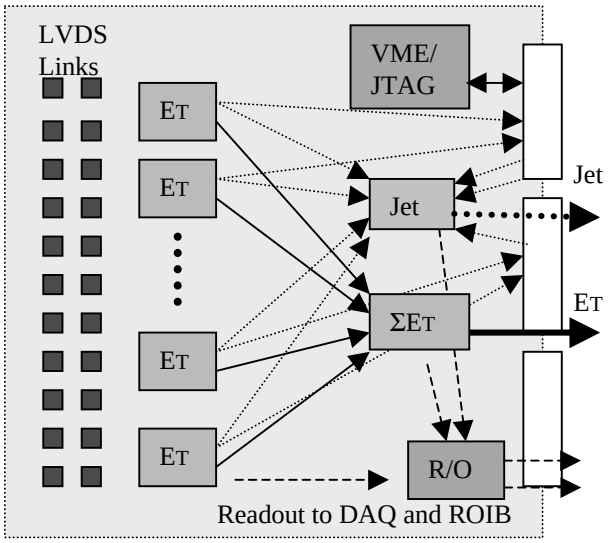

Figure 2: The Jet/Energy Module (JEM)

The Energy Sum FPGAs also distribute the 10-bit E_T values of each Jet element via 80 MHz point-to-point links to Jet FPGAs on the same module and to neighboring modules, providing each JEM with the necessary environmental information to perform the Jet algorithm.

Board-level Jet and Energy Sum results are transmitted via point-to-point links from each module to a Jet Merger Module and a Sum Merger Module in each crate. The crate-level results are merged and reduced to trigger bits, which are sent to the Central Trigger Processor.

The input and output data of each module, as well as the types and positions of clusters identified in the Jet algorithm, are stored in pipelines on the Energy and Jet FPGAs, to be read out to the DAQ and ROI Builder upon a L1A decision.

3. DESIGN FEATURES

3.1 The Energy Summation Algorithm

The Energy Sum FPGAs process input data using the algorithm shown in Figure 3. Separate 9-bit electromagnetic and hadronic energies for each Jet element are received at 40 MHz. Noise-reduction thresholds are applied, after which the electromagnetic and hadronic parts of the Jet element are summed. Lookup tables produce values of E_T, E_X, and E_Y for global summation, and the 10-bit Jet element transverse energy sum is multiplexed to 5 bits at 80 MHz and fanned out to the Jet FPGAs.

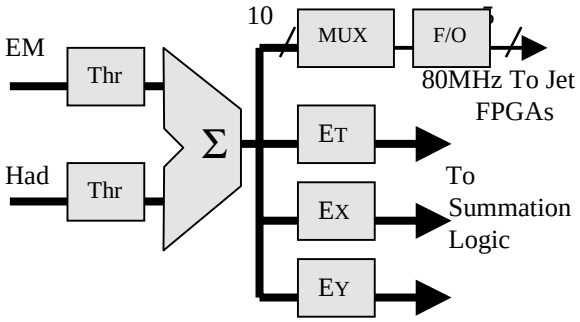

Figure 3: The Energy Summation Algorithm

The Energy Sum algorithm is foreseen to be implemented on a Xilinx Virtex device [1], with typically four Jet elements processed by each FPGA. An additional Virtex device merges the results of adder trees in the Energy FPGAs to produce E_T, E_X, and E_Y values for the entire module.

Xilinx Virtex devices were chosen for the Energy Sum algorithm implementation for a number of reasons. Virtex offers large amounts of logic and I/O resources at relatively low cost. Large amounts of distributed and block memory are available for lookup tables and other functions, and DLLs are available for internal and external clock synchronization. Maximum system speeds are far higher than the 40 and 80 MHz necessary for the algorithms, relaxing the implementation.

3.2 The Jet Algorithm

The Jet algorithm is implemented in 64 Jet FPGAs, each of which covers a 2x8 Jet element area in ηxϕ. The positions of potential Jet cluster candidates are identified by summing the energies of Jet elements in 0.4x0.4 windows sliding in increments of 0.2, and identifying

local maxima. These are referred to as ROI or decluster positions. Jet clusters are identified by comparing transverse energy sums within windows of size 0.4, 0.6, or 0.8 that exceed predefined thresholds and are associated with an ROI position. All three Jet window sizes are calculated in parallel, and 8 combinations of energy threshold and window size are available for trigger menus. The Jet cluster sizes (dark areas) and their associated ROI positions (bold outlines) are shown in Figure 4. For Jet clusters of size 0.6, the ROI position can be in one of four positions in the cluster.

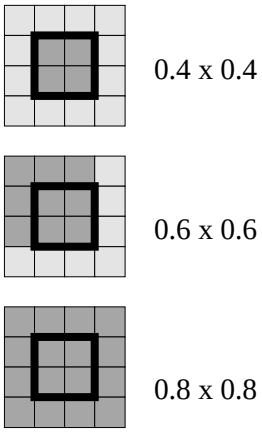

Figure 4: Jet cluster definitions

Each Jet FPGA receives 10-bit ET information from 55 Jet elements providing the 5x11 environment necessary to construct all of the needed cluster sums. To process all 550 bits of data on a single device, the information must be received at 80 MHz, halving the number of input pins necessary.

The data continues to be processed at 80 MHz after it has been received in the Jet FPGA. One reason for doing this is to reduce the latency of the Jet algorithm, which is one of the most time-critical paths in the ATLAS Level-1 trigger. The second reason for doing this is that it allows additions and comparisons to be performed by so-called "5-bit serial" calculations, where 10-bit operations are carried out in two consecutive 5-bit steps. The use of 5-bit serial calculations reduces the necessary logic and routing resources by nearly a factor of two, and also raises the maximum speed of the algorithm.

Large savings in logic and routing resources are also achieved by carefully eliminating duplicate and unnecessary calculations in the algorithm. For instance, the results of a single magnitude comparison between two adjacent decluster positions can be used by both positions to determine whether either is a local maximum. Similarly, only Jet windows that are actually associated with a local maximum need be tested against energy thresholds.

The baseline device for the Jet FPGA implementation is the Altera FLEX 10k250 [2]. The 10K series of FPGAs has a global routing architecture which is well suited for large designs with high clock rates and the large degree of data fanout and routing inherent in the Jet algorithm. It is planned to investigate alternative devices, including Xilinx Virtex and Altera Apex, before producing the final system.

3.3 Backplane Signal Transmission

The Jet/Energy Sum system has a full-custom 9U backplane. The baseline choice of card-edge and backplane connectors are 5+2 row, 2mm HM connectors which are an industry standard and commonly used in CompactPCI. The crate and front panel hardware are planned to be based on the IEEE 1101.10 standard.

All Jet element data are transmitted from the Energy Sum FPGAs to the Jet FPGAs via point-to-point links using low-voltage CMOS levels. This includes signals between FPGAs on the same board as well as data sharing between neighboring JEMs via short backplane links. Because the CMOS levels are compatible with the Jet FPGA inputs, no signal translators are necessary on the receiving end of the links. It is also considered to be possible to drive all 80 MHz signals directly from the Energy Sum FPGA output pins. This strategy promotes signal uniformity within the system, and simplifies the design of the JEM by eliminating large numbers of driver and receiver devices.

Transmission of JEM results to the Jet and Sum Merger Modules is also performed via point-to-point links. Studies of appropriate signal levels and termination schemes are currently in progress.

3.3 Making Use of Reprogrammability

It is planned to take advantage of the in-system reprogrammability of the FPGAs in the system. Configuration details-such as energy thresholds and lookup table contents-will be controlled by writing to registers implemented in the FPGA designs. However, more significant changes in functionality-such as modifications to the Jet algorithm-may be easier to make by downloading a different FPGA design altogether. It is conceivable that several FPGA configurations may be selected for different luminosity or noise conditions, for example.

The most important use of FPGA reprogrammability may be the ability to use special diagnostic configurations to perform fast and complete testing of all signal paths in the system. Such configurations could be routinely loaded and run during pauses in data taking, for example, during beam fills. They could also be used to quickly pinpoint the source of errors discovered by trigger monitoring and validation programs.

4. DEMONSTRATOR PROGRAMS

Technology demonstrator systems have been built and tested to confirm the feasibility of key elements of the design.

4.1 "Module –2" Technology Demonstrator

The JEM Module -2 was designed to study issues raised during the review of the Level-1 Technical Design Report [3]. These issues included the reliability of 80 MHz data transmission between FPGAs and across backplane links, the performance of algorithms at running at 40 and 80 MHz, and the reliability of high-speed serial links using different cable and connector options.

Each Module –2 board includes a Xilinx 4013XL and an Altera 10K50V FPGA with point-to-point links between them, and to a 2mm-pitch HM backplane connector which allows two such modules to be connected by a small 2-slot backplane. Another set of direct and backplane connections between the FPGAs pass through an ALVC buffer chip clocked at 80 MHz. Each of the four data paths is 10 bits wide. The timing of each FPGA and the ALVC buffer are independently controlled using adjustable delays.

Each board also includes a pair of HP Glink transmitter and receiver devices for link stability tests. A VME interface implemented on a separate Altera 10K30 FPGA is used for control and monitoring. A 40 MHz clock is provided by an external source.

Data transmission tests using the Module –2 system showed error-free CMOS data transmission over all paths, both with and without the use of intermediate ALVC drivers. Upper limits on bit-error rates were set at $\sim 10^{-14}$. The timing margin for 80 MHz data was measured to be 9.6 ns with buffers, and 7.3 ns with direct transmission between FPGAs. Sample "5-bit serial" calculations were tested at 80 MHz and found to work as expected.

Early experience with the use of serial links was gained, both with HP Glinks, and later with LVDS links that were added to the board using a small adaptor PCB. The results of these tests have been superseded by experiences with the Mainz Link Test Board.

4.2 Mainz Link Test Board

The Mainz Link Test Board was designed to gain experience with National Instruments LVDS serial links, and to identify and solve previously observed problems with link stability over long cables and differential PCB tracks.

The Link Test Board is a 3U card that fits in a J1 VME backplane slot. The board contains 8 LVDS receiver chips, which are read out by two Xilinx Virtex XCV100 devices. A VME interface is implemented on a Xilinx CPLD. Modified JEM Module –2 boards were used as data sources for tests.

Tests showed that an active pre-compensation circuit at the LVDS data source improves link stability and allows the cable range to be extended. Stable transmission of four links over 15m of category 5 twisted-pair cable plus 55 cm of differential PCB tracks was achieved using a pre-compensation circuit based on the Motorola MC10EL89 differential fanout gate [4]. Commercial off-the-shelf pre-compensation solutions for the final system are currently being investigated.

5. OUTLOOK

The Module –2 and Link Test Board programs have shown that the key design features of the Jet/Energy Sum processor are sound. Plans are currently underway for the first of two prototype systems planned before production.

The Jet/Energy Sum "System –1" will be a fully functional prototype system with reduced channel count. It is planned to be a single crate 6U system with JEMs, merger modules, and timing and VME modules connected via a custom backplane. It is hoped to have the system fully operational by summer 2000.

"System 0" will be a single crate, full size prototype system. It should be nearly identical to the production hardware, with only minor changes necessary. Construction and testing of System 0 should be completed by the end of 2001.

In addition to the planned prototype systems, additional technology demonstrators may also be produced to evaluate and gain experiences with new devices which appear on the market.

6. CONCLUSIONS

An overview of the Jet and Energy Sum processor for the ATLAS Level-1 Trigger has been presented. The design system is based on the use of commercial off-the-shelf components, including large programmable logic devices. The design includes implementation details that reduce latency and board complexity, and use FPGA reprogrammability to enhance system flexibility and diagnostic capability. Technology demonstrator programs have confirmed the feasibility of key elements of the processor design, and two fully functional prototype systems are planned before the start of final production.

7. REFERENCES

1. http://www.xilinx.com/
2. http://www.altera.com/
3. The ATLAS Level-1 Calorimeter Trigger Technical Design Report (1998)
4. http://scgproducts.motorola.com/