THE ATLAS CALORIMETER CALIBRATION BOARD
Tests of a first set of boards
New Developments

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Abstract

The ATLAS Liquid Argon electromagnetic calorimeter needs a very accurate calibration system in order to fulfill its physics requirements. A set of 10 calibration boards has now been produced to test the calorimeter modules in electron beam. These boards contain a programmable sequencer which allows the loading and execution of a complete calibration run (various DAC values, delays and patterns) and provide 128 signals which are injected to the electrodes through high precision resistors. Measurements have demonstrated a good uniformity and a good linearity though small distortions have been identified. Radiation tests with both neutrons and gammas have shown many shortcomings in the pulser and control logic. New developments to address these shortcomings are discussed.

1. INTRODUCTION

The precision in physics aimed in ATLAS requires a good energy resolution over the full acceptance and thus a small overall constant term, better than 0.7%. Part of this constant term is related to the ability to calibrate 200000 channels with a good accuracy [1].

Due to the fast shaping times used at LHC experiments, the readout electronics is current sensitive and thus the traditional charge calibration through a precision capacitor is no longer valid. Moreover, the parallel noise is smaller at these shaping times and thus it is possible to use a current calibration with precision resistors.

2. REQUIREMENTS

- *Signal :* it should be as close as possible to the real signal which has a triangular shape. The initial current must be very precise and injected close to the electrodes. The rise time must be 1 ns and the decay time 450 ns.

- *Dynamic range :* from 200 nA (noise level) to 10 mA (nearly 3 TeV in one cell).

- *Non uniformity between channels :* 0.25% including the board itself and the signal distribution (cables, mother boards).

- *Linearity :* the integral non linearity must be less than 0.1% for each of the 3 gains of the shaper [2].

- *Timing between the real physics signal and the calibration pulse :* within ±1 ns to keep the sensitivity to any jitter as small as possible

- *Radiation hardness :* the board must tolerate radiation fluxes of gammas (20 Gy/yr) and neutrons (10^{12} n/cm^2/yr).

- *Magnetic tolerance :* ~100 Gauss

3. CALIBRATION PULSER DESIGN

3.1 Principle:

The calibration pulses are generated by pulsers the principle of which is described on Figure 1.

The fast output voltage pulse is obtained by interrupting a precise DC current I_p that flows in the inductor. When a pulse command is applied on Q_2, Q_1 is cut off and the current is diverted to ground. The magnetic energy stored in the inductor produces a voltage pulse with an exponential decay across the parallel

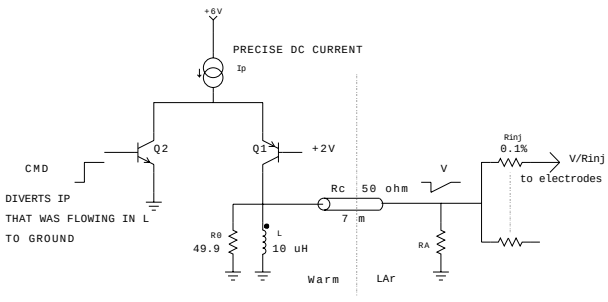

Figure 1 : Principle of the pulser

combination of the cable characteristic impedance Z_c and a termination resistor R_o of the same value. This pulse is propagated inside the cryostat through a 7 m long 50 Ω cable adapted at both ends and is applied across a precise injection resistor R_{inj} (0.1%) in the cold, directly to the electrodes. The resulting current is given by:

$$Ical = -\frac{Ro}{2\,Rinj}\,Ip\,e^{-t/\tau} \quad \text{with } \tau = 2L/Ro \quad (Ro = Ra = Zc)$$

An amplitude up to 10 mA can be achieved by applying a 5V pulse in a 500 Ω injection resistor.

The main difficulty of this calibration system is to distribute uniformly throughout the calorimeter a very precise voltage pulse. To minimise the attenuation due to skin effect, the pulsers are located close to the feedthrough.

3.2 Complete design :

The current I_p is generated from a 18 bits DAC voltage through a voltage to current converter. The current in the output branch is I_1=VDAC/R20, as negligible current flows in the gate of the JFET transistor. A low offset op amp as OP 07 must be used, as Voffset = 100 µV already corresponds to 15 LSB.

To insure good linearity, the base current of Q_1 which varies non linearly with I_p (βvaries with the collector current and the temperature) is measured and added to I_p.

Q_1 is made of 4 transistors in parallel to share the large DC current for I_p (up to 200 mA) and to keep a low R_{cc}, necessary for the wide dynamic range.

Five precision resistors (0.1%) determine the calibration pulse accuracy.

4. CONTROL LOGIC :

The control logic (Figure 3) incorporates a memory to store the calibration parameters of a full run, a sequencer and registers for the current parameters.

These parameters are:

- DAC values (ramp for linearity measurements)
- Delay values (for timing studies)
- Pattern values (to select channels and enable crosstalk measurements)
- Number of triggers (stored in the sequencer)

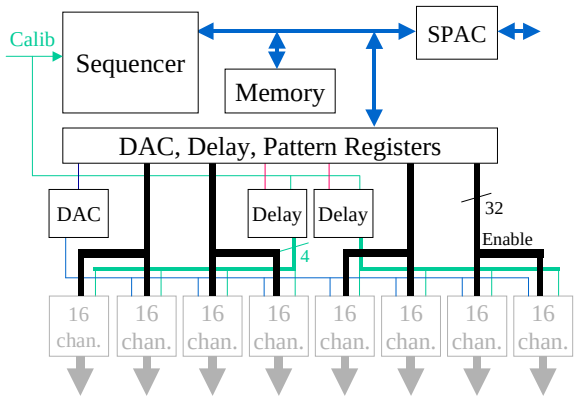

Figure 3 : Control logic

The memory and the sequencer are initialised at the beginning of a calibration run using the SPAC protocol [3]. The sequencer controlled by the calibration signal loads the registers from memory using an

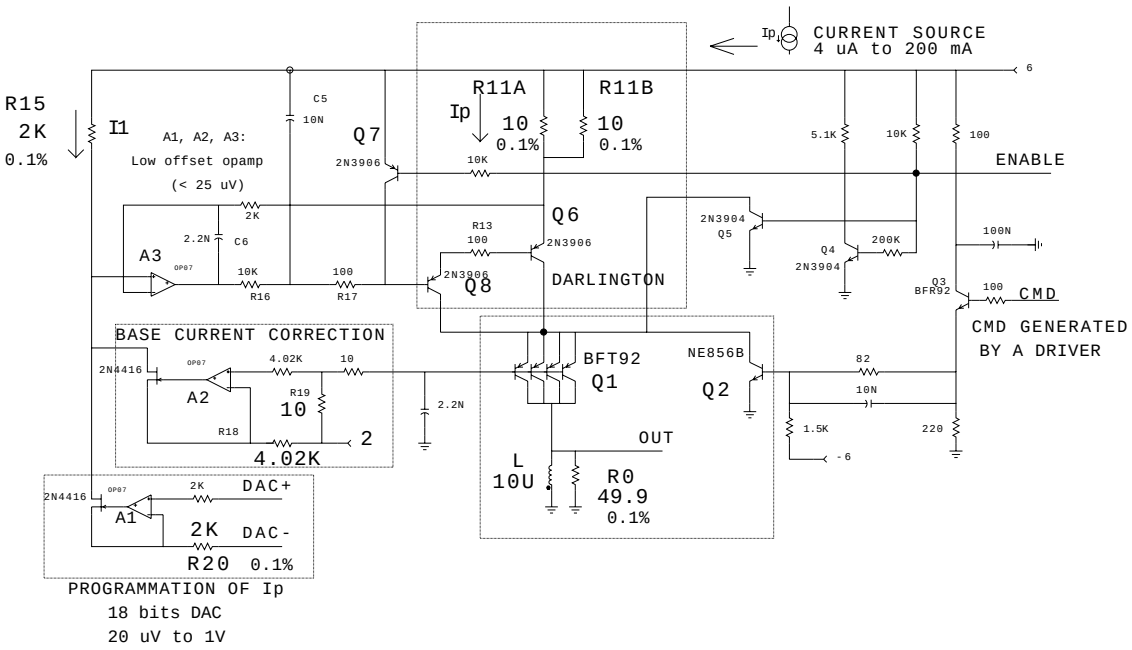

Figure 2 : Schematics of the analog part

algorithm with 3 embedded loops as shown in Figure 4.

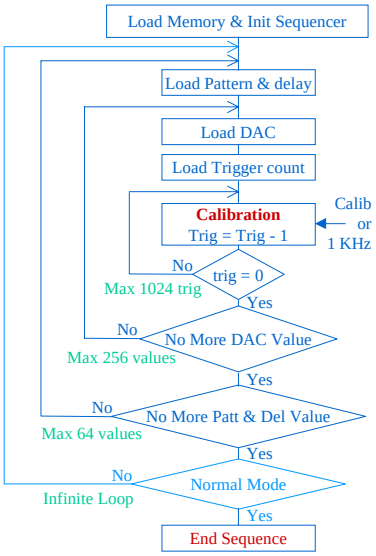

Figure 4 : Sequencer algorithm

No access to the board is necessary during one run, but the parameters stored in the registers can be read back before each calibration pulse if required.

5. PRACTICLE REALISATION

A board with 128 pulsers has been realised (Figure 5)

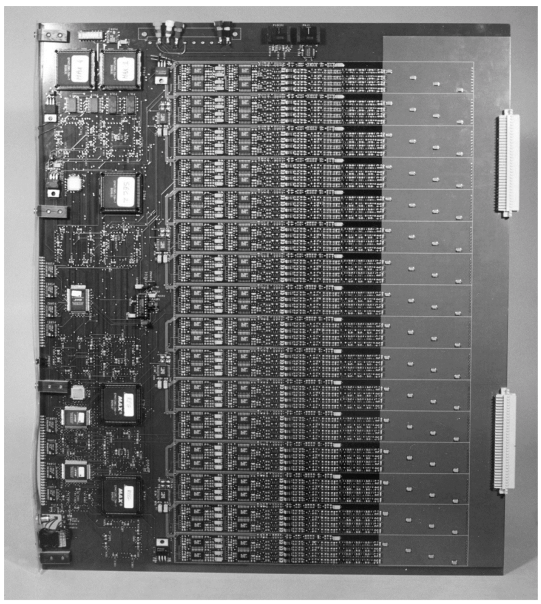

Figure 5 : Calibration board

The size of the board (490 mm x 410 mm) is determined by the front end crate dimensions [1].

The analog part contains 64 pulsers on each side of the board. The pulsers are aligned in a single row close to the output connectors to ensure good uniformity distribution. As the density is very high, surface mounted components have been used (9000 components).

The control logic is located on the top of the board, inside 13 Alteras FPGAs (EPM7128ELC84-7).

6. EXPERIMENTAL MEASUREMENTS

6.1 Signal shape

A signal measured at the output of one pulser is shown in the following plot. The pulse shape nicely follows an exponential decay as shown by the fit and the rise time is 1 ns.

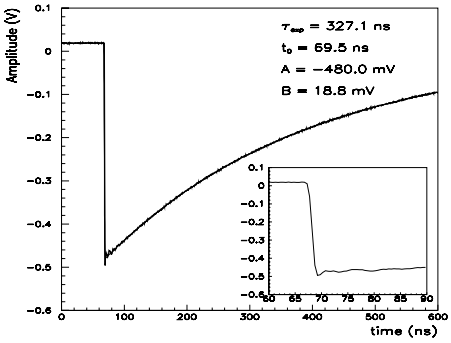

Figure 6 : Signal shape

6.2 Pulse Uniformity

There are 2 sources of non uniformity :

A dispersion in the exponential decay time of the pulse which is dominated by the inductance dispersion and a dispersion in the pulse amplitude which is defined by five 0.1% precision resistors.

The dispersion of the inductance value has been measured in 3 different ways.

- Directly on the board using an RLC meter at 1 MHz. The relative rms dispersion is about 1.7%.
- Fitting the exponential decay time of each channel when no shaping is applied. The average decay time is 346 ns with 5.7 ns dispersion resulting in a 1.6% inductance dispersion.
- Measuring the uniformity with a longer shaping (t_p = 350 ns)to be more sensitive to the exponential decay time. The rms amplitude dispersion is 0.73% which translates in a 1.5 % inductance dispersion.

These inductance dispersion measurements are in good agreement and a 0.11% non uniformity can be deduced at ATLAS shaping time.

The pulse amplitude uniformity has been measured with a 12 bits ADC after the atlas shaper ($CRRC^2$ shaper with t_p = 45 ns) at various DAC amplitudes for each board. Figure 7 shows the results for a set of 8 boards. The sigma of the dispersion is about 0.19% and a clear structure is observed corresponding to the two output

connectors. This is entirely explained by the difference in copper length between each pulser and the output connectors. Consequently it was decided to apply a software correction as a function of the channel number (the same for all boards).The sigma of the dispersion is then 0.11% as shown in Figure 8.

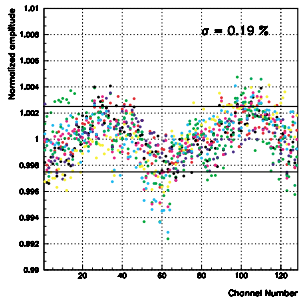

Figure 7 :
Raw uniformity
of pulse amplitude

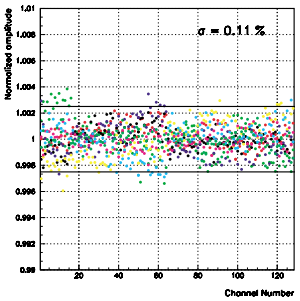

Figure 8 :
Uniformity after
software correction

6.3 Linearity

The linearity has been measured with a 12 bits ADC, sampling the signal at the peak, over the 3 gains of the ATLAS shaper (t_p = 45 ns). The time at which the signal is sampled is set on a large signal.

The integral non linearity is within ± 0.1% for all gains as shown in Figure 9. On the medium range and more obviously on the low gain a parabolic shape is observed. This is explained by a small change in rise time of the calibration signal. After shaping the position of the peak is shifted by about 1 ns but as the signal is measured at fixed phase, it results in a small non linearity.

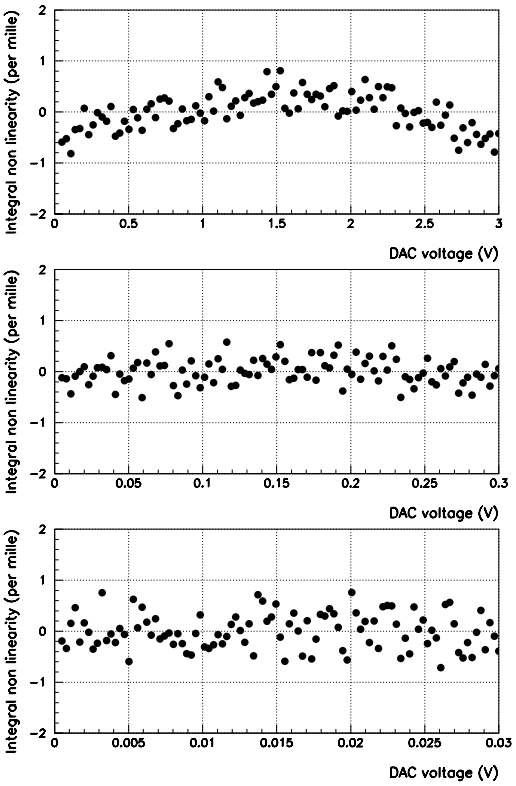

Figure 9 : Integral non linearity

6.4 Command feedthrough and injected charge

A small positive spike (15 mV – 1 ns) is due to the capacitive coupling of the command pulse (CMD) through the C_μ capacitor of Q_2, whereas Q_1 is still on. It generates a small signal on a disabled channel which is lower than 0.1% of full high gain scale after shaping (30 MeV).

A small negative spike (30 mV – 2 ns) is present when the DAC is set to zero. It corresponds to the injected charge. When Q_1 is cut off by the command pulse, the very fast voltage variation on its collector, 3V in 1 ns, results in a charge which is injected in the output through a ~1 pF parasitic capacitor between the emitter and collector of Q_1. It translates in a signal after shaping which is 3% of the full high gain scale (1 GeV) but only 0.1% at the peak sampling time (30 MeV).

6.5 Crosstalk

The crosstalk over one output connector has been measured in the ATLAS configuration (a warm cable following by a pin carrier, a vacuum cable, a second pin carrier and a pigtail [1]). The 64 channels are 50 Ω terminated.

The crosstalk is concentrated on 2 adjacent channels on each side of the pulsed channel and 3 channels on the opposite side. The maximal peak to peak amplitude is 0.3% reduced to 0.1% at signal peak position.

6.6 Board stability and noise

The signal stability has been measured by performing identical measurements at a few hours interval. The DAC output and its temperature have been monitored over a long period. The signal drift is fully explained by the DAC offset variation with temperature which is 30 µV/°K.

The calibration board should not introduce sizeable electronic noise in the readout system. We have measured it not to be higher than the noise generated by the FEB (Front End Board) in high gain.

6.7 Timing

Two four channels delay chips [4] are used per board in order to align the time of the peak of the calibration signal with respect to the physics one. The delay chips has been measured linear to ± 0.2 ns over 0 to 25 ns range with a 0.996 ns step.

The jitter dependance with the delay value has also been measured. It starts at 100 ps and increase to 300 ps

for the maximum delay value. The chips used on the calibration boards are from the earliest version and do not reflect their actual performance.

7. MAGNETIC TOLERANCE

In the front end crate, the boards will be exposed to a magnetic field of approximately 100 Gauss. Such a field can modify the inductance and then the decay time constant of the calibration pulse. The decay time constant change between 0 and 400 Gauss has been measured to be less than 1 % which correspond to 0.1% change in amplitude after shaping.

8. RADIATION TOLERANCE

Several components of the pulsers have been irradiated to neutrons (10^{13}n/cm^2) in Grenoble and gammas (20 hours with 10 Gray/hour) in Saclay, and the most sensitive elements have been found to be low offset OpAmps. Many commercial OpAmps have been tried but died after neutron irradiation. The OP177 resists to neutrons and gammas, but the increase of the offset voltage from 10 µV to 100µV is not acceptable.

A commercial dual 18 bits DAC (PCM 1700P Burr Brown) has been irradiated, but the offset voltage drifted to 1 mV after irradiation.

All other semiconductors exhibited satisfactory behaviour.

The control logic has not been tested but the Alteras are known to be not radiation tolerant.

The delay chip is in a version not yet radiation tolerant.

The voltage regulators died during the tests.

9. NEW DEVELOPMENTS

New developments [5] are necessary to fulfil the ATLAS requirements in particular concerning radiation tolerance.

- Design of a specific PMOS transistor to replace the 4 PNP transistors in parallel in the current switch to reduce the injected charge effect.
- Radiation tolerant OpAmp used in the current source. We are developing a low offset OpAmp following two approaches: a CMOS autozero OpAmp [6] which has already been developed by Mainz University but needs to be adapted and a bipolar OpAmp using external precision components and trimming to get a low offset.
- Radiation tolerant 16 bits DAC. We study two designs: a ramp DAC (charging an integrator with a DC current during a well controlled time) and an R/2R ladder DAC where the resistor network is made of discrete precision components.
- Radiation tolerant control logic. It has been decided to replace all the control logic in the Alteras FPGA by DMILL asics. The control logic will be simplified by suppressing the sequencer and an asic incorporating all the basic functions required will be developed and used throughout the board. A few COTS might still be required.

10. CONCLUSIONS

Experimental measurements on the 128 channels calibration board [7] with final ATLAS density have given good results and fulfil the calorimeter requirements.

Ten boards have been produced and 5 have been used on the test beam at CERN.

The next step is to ensure that all elements on the board exhibit satisfactory radiation tolerance, in particular the low offset OpAmp, the DAC and the digital part. New developments are underway and a decision for the production of a radiation tolerant calibration board is expected in the year 2000.

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