A 1.25Gbit/s Serializer for LHC Data and Trigger Optical Links

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ABSTRACT

Several LHC detectors require high-speed digital optical links for data transmission in both data readout and trigger systems. Commercial components can be found that meet the bandwidth requirements of most of the LHC detectors subsystems. However, they fail to meet some of the requirements frequently encountered in the LHC-HEP environment, namely: resistance to high radiation doses and operation tolerant to single event upsets. To address these problems, a high-speed transmitter ASIC (1.2Gbit/s), containing a serializer and a clock multiplying PLL was developed. The prototype was implemented in a mainstream 0.25um CMOS technology and was designed using well-established radiation tolerant layout practices to achieve resistance to high radiation doses. This implementation serves as a base for the development of radiation tolerant IC's that will make feasible the transmission of data using common local area networks protocols in typical LHC radiation hard environments.

The ASIC was embedded in a test setup that uses a commercial optical receiver and de-serializer. Error free data transmission at 1.2Gbit/s was achieved proving the prototypes to be fully functional.

1. INTRODUCTION

Several LHC detectors require high-speed (~ Gbit/s) digital optical links for transmission of data between the different sub-detectors and the data acquisition systems. Typically, high-speed data transmission is required for both the trigger systems data path and the data readout systems. In general, those links will be uni-directional with the transmitters located inside the detectors and the receivers situated in the control rooms. In this arrangement, the transmitters will be subject to high levels of radiation doses over the lifetime of the experiments. Additionally, the large numbers of high-speed optical links planned (of the order of 100K total for the four LHC experiments) impose strict constraints on both the cost and power dissipation allowed per device in the system. Moreover, in trigger links, data has to be transmitted with constant latency and synchronously with the LHC 40.08MHz reference clock - this to facilitate data alignment at the receiving end before the data is feed to the trigger processors. In other words, high-speed optical links for the high-energy physics environment require:

- hardness to total dose radiation effects (up to 10Mrad in some cases);
- operation tolerant to SEU;
- low power dissipation;
- low cost;
- and, in trigger systems, constant latency (synchronous) transmission.

Commercial optical links and components can be found that meet the bandwidth requirements of all of the planned systems. However, they fail to meet one or several of the requirements mentioned above.

To address these problems, high-speed radiation hard transmitter IC's will have to be developed. In this paper, the feasibility of such an IC employing radiation tolerant layout practices in a mainstream sub-micron CMOS technology is assessed. A prototype has been developed and it is here described. It incorporates the most critical functions of a high-speed transmitter. It includes: a serializer that transforms 10-bit parallel words into a 1.2Gbit/s (or 1.25Gbit/s) serial bit stream, a clock multiplying PLL that generates the internal 1.2GHz (or 1.25GHz) clock from the 40.08MHz LHC clock and an high-speed 50 Ω (PECL like) driver that allows the chip to interface with most common optical transmitters. The IC features a low operation voltage (2.5V) contributing to low power consumption. The prototype was conceived having in mind data transmission in trigger systems, thus allowing synchronous transmission of data at rates compatible with the LHC bunch-crossing frequency. However, the operating data rate and the data framing to be implemented have been chosen close to the industrial Gigabit Ethernet standard so that the transmitter can also be operated at a standard data-communications frequency (1.25Gbit/s) permitting testing using commercial equipment. Additionally, this will allow the IC to be used in conjunction with standard chip-sets for applications were synchronous transmission is not essential, e. g. event building, thus enlarging the users choice and allowing for flexible system development. Since data transmission will be encapsulated in an 8B/10B line-coding scheme, this will result in an effective data rate of 960Mbit/s when the transmitter is operated in the synchronous mode at

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1.2GHz (30 times the LHC clock frequency). In this mode, if the 8B/10B encoding is used, the user can thus transmit 24 bits every LHC bunch crossing. For asynchronous operation, a 1Gbit/s effective data bandwidth can be achieved if the standard 1.25GHz clock frequency is used.

In what follows, the architecture of the high-speed serializer, its main circuit details and the considerations that have lead to the particular implementation will be addressed.

2. SERIALIZER ARCHITECTURE

CMOS serializers capable of Gbit/s data rates have been widely reported in the literature (see for example [1] and [2]). In its most simple expression, a serializer is a shift register, clocked at the bit rate frequency that is periodically loaded with the data words to be serialized. Since a parallel-load shift register is usually composed of a cascade of D-flip-flops and of two-to-one multiplexers, the maximum achievable operation frequency is limited by the sum of the flip-flop clock to output propagation delay, the flip-flop setup time and the multiplexer propagation delay. For 1.25Gbit/s operation, the sum of those critical timing parameters has to be less than 800ps. For the sub-μm CMOS process used, the propagation delay and the setup time are given in Table 1 for a dynamic (DFF) and a static (SFF) flip-flop. Also shown in the table is the propagation delay of a two-to-one multiplexer. The reader should note that the propagation delays given here are slightly higher than what would normally be expected from a 0.25μm CMOS technology. This is a consequence of using enclosed transistor geometries to achieve radiation tolerance [3]. This technique introduces slightly higher capacitances in the signal path, resulting in circuits with relatively higher propagation delays.

	DFF t_{pd} (ps)	DFF t_{sup} (ps)	SFF t_{pd} (ps)	SFF t_{sup} (ps)	MUX t_{pd} (ps)
typical	145	60	309	107	104
worst	369	152	749	296	247

Table 1 Clock to output delay (t_{pd}) and setup times (t_{sup}) for dynamic (DFF) and static (SFF) flip-flops. Also shown, two-to-one multiplexer propagation delay. Only typical and worst case process corners figures are given.

As can be inferred from Table 1, reliable operation of the simple shift register structure can not be guaranteed at 1.25Gbit/s under all[2] process, power supply and temperature conditions using static flip-flops. To ensure this would require the use of the dynamic flip-flops. However, the operation of this type of flip-flops relies on the storage of charge in high impedance nodes during certain phases of the operation. This renders the dynamic flip-flops particularly sensitive to single event upsets (SEU) [4], a characteristic that is highly undesirable in radiation environments. Using static flip-flops to implement a 1.25Gbit/s serializer that will operate reliably under all process, temperature and power supply conditions requires thus the departure from the simple shift register structure. By looking at the numbers in Table 1, it can be seen that the SFF can be used to build a shift register that operates up to 770MHz under all conditions. This leaves enough room to implement a serializer where the parallel data word is split in two groups of bits that are shifted in two independent shift registers each operating at 625Mbit/s. If the shift order of the parallel data bits is properly selected and the two serial bit streams combined using a single fast multiplexer a 1.25Gbit/s serializer is obtained. This was the architecture adopted in this development because it avoids the need to use dynamic flip-flops and reduces the clocking frequency to half.

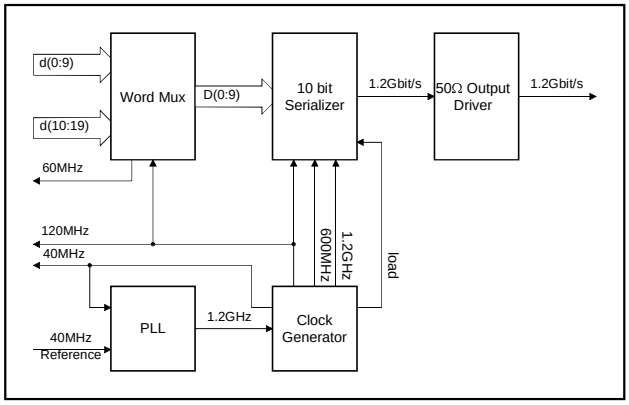

Figure 1 1.25Gbit/s serializer ASIC block diagram.

The implemented ASIC (whose block diagram is shown in Figure 1) operates as follows. The external 20-bit wide bus accepts parallel data at a rate of 60MWords/s. This data is time division multiplexed by the "Word Mux" into two 10-bit words which are then feed to the "10-bit Serializer" at a rate of 120MWords/s. Then, the serializer - as discussed before - converts the 10-bit words into an 1.2Gbit/s serial stream. Finally, the data out of the serializer is passed to the "50 Ω Output Driver" that converts the internal CMOS levels into Pseudo-ECL (PECL) levels to allow interfacing of the ASIC with commercial optical transmitters. The operation, as described above, requires several clocks and control signals at different frequencies. These are generated in the IC by the Phase-Locked-Loop (PLL) and the "Clock Generator" circuit. For operation at 1.2Gbit/s, the PLL takes as its reference the 40.08MHz LHC clock. (or a 41.66MHz clock for operation at 1.25Gbit/s) and compares it with its output signal divided by the "Clock Generator" by a factor of 30. In this way, a 1.2GHz clock is obtained at the PLL output. The "Clock Generator" provides the 60 and 120MHz clock signals required by

[2] By "all" its meant, process variations within ±3σ, power supply 2.5V±10% and junction temperature between -10 and 125°C

the “Word Multiplexer”, the 600MHz clock and the “load” signal needed by the high-speed serializer.
The implemented IC as described here does not allow transmission at the reference clock rate. This would require the implementation of 30-bit to 10-bit word multiplexer. This was not done in the prototype to avoid a high penalty in silicon area due to a highly pad limited layout. However, data transmission at the reference clock rate can be easily obtained by the addition of simple external logic.

2.1 The High-Speed Serializer

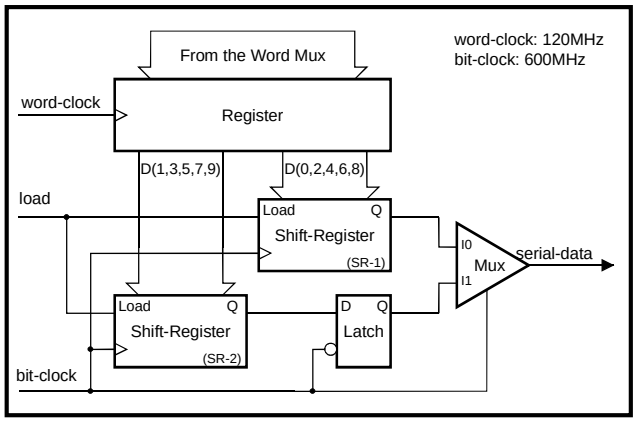

Figure 2 Simplified diagram of the high-speed 10-bit serializer.

The high-speed serializer is portrayed in some detail in Figure 1 and its operation can be described in the following way. Each “word-clock” cycle a 10-bit word from the “Word Multiplexer” is loaded into the “Register”. The output of this register is separated into two 5-bit words and loaded, some time later, into two 5-bit shift-registers (SR’s). As shown in Figure 1, splitting of the 10-bit word is done in such a way that adjacent bits are loaded into different SR’s. The output of one of the shift-registers (SR-1) drives one input of the output multiplexer while the other one (SR-2) drives a latch. This latch drives the other multiplexer input and its purpose is to delay the data shifting operation by half a clock cycle in relation to the output of the first SR. Since the select input of the output multiplexer is driven by the shifting clock (600MHz), it correctly selects between adjacent bits and constructs the desired 1.2Gbit/s bit stream. This is represented schematically in the timing diagram of Figure 3.
It should be clear that in this scheme the duration of each bit in the final 1.2Gbit/s serial stream depends on the duty-cycle of the shifting clock. That is, if the clock duty cycle is distorted the final serial data will have bits whose width will depend on the duration of the selecting level. This is of course undesirable since it translates into jitter in the transmitted data having potential ill effects on the clock and data recovery circuitry of the associated receiver. Note also that the same effect will occur if an unbalance exists in the output multiplexer. To avoid these situations two actions have been taken. First, the 600MHz-shifting clock is obtained by dividing the 1.2GHz VCO clock by two. In this way, a nearly 50% clock is obtained. This scheme has the obvious disadvantage of requiring a full speed running clock. However, this is only true for two components: the VCO and the divide-by-two flip-flop. Second, the multiplexer output data can be sampled by a flip-flop driven by the 1.2GHz clock to avoid both the effects of clock duty-cycle distortion and multiplexer asymmetry.

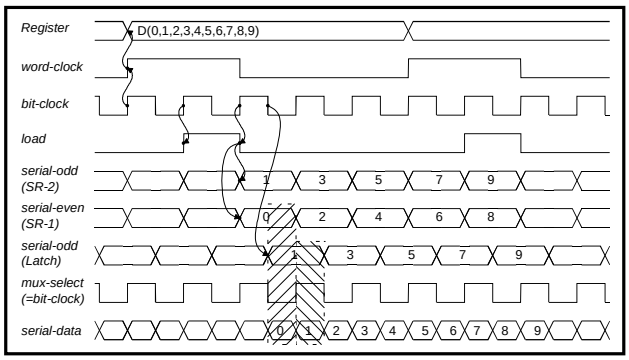

Figure 3 High-speed serializer timing diagram.

As discussed before, clocking flip-flops at 1.2GHz requires the use of dynamic circuits with all their associated drawbacks concerning single event upsets. As a safeguard, the dynamic flip-flop that samples the serializer output can be bypassed in the prototype. On the other hand, the divide by two flip-flop can not be avoided. It was however estimated that such a device (possible the only one in the circuit) would contribute very little to the ASIC SEU sensitivity. According to preliminary data [4] and based on a novel simulation method [5] it was estimated that, for example, a dynamic FF in an IC siting 1m away from the interaction point in the detector would only contribute a few tens of upsets over 10 years of LHC operation. Although this seems small its consequences in trigger systems, where many links (~1000) will be operated together, need to be assessed.

2.2 The Clock Generator

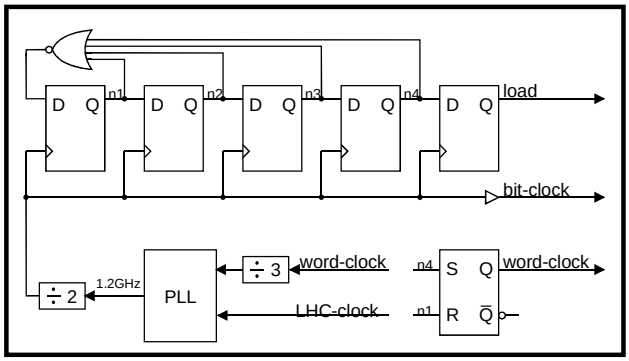

Figure 4 Clock-generator simplified diagram.

In the clock-generator circuit (Figure 4) the word-clock (120MHz), the bit-clock (600MHz) and the load signals for the shift registers are generated from the 1.2GHz PLL

clock signal. The VCO clock is divided by two by a flip-flop and then again by five by a “ring” divider to obtain a 120MHz signal. The “ring” divider circulates a “one” and four “zeros”. From this circulating “one” the load signal is directly obtained while the word-clock is produced by a SR flip-flop sensing the circulating one. The 120MHz clock after division by three is fed to the PLL where its frequency and phase are compared with the LHC 40MHz-reference clock.

2.3 The Phase-Locked-Loop

The PLL implemented in the ASIC uses a classical structure. It employs a three-state phase frequency detector, a charge pump, an RC loop-filter and a differential VCO with symmetrical loads [6], [7]. In this design the loop jitter and the sensitivity to the power supply noise were considered of major importance. Since the PLL and clock-divider multiply the reference clock by 30 a corrective action is only taken every 30 VCO cycles. To obtain a “jitter-free” clock signal, it is thus important to minimize the noise contribution of the VCO itself. In this design the VCO is composed of three differential cells. To reduce the VCO cycle-to-cycle phase noise to about 2ps a current of 1.1mA biases each cell. Behavioral level simulations were made that take into account the intrinsic VCO noise and the reference signal noise. From these simulations, assuming a reference signal with 160ps RMS jitter (1.1ns pp) the PLL is expected to generate a 1.2GHz clock with an RMS jitter of the order of 34ps RMS (232ps P-P).

3. TEST SETUP

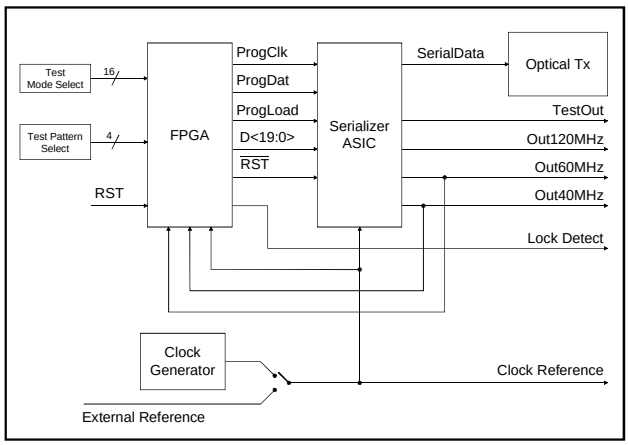

Figure 5 Serializer ASIC test-card block diagram.

A test-setup has been developed for the serializer ASIC. The block diagram of the transmitter side of the setup is depicted in Figure 5. It consists of the serializer ASIC, an FPGA, a clock generator and an optical transmitter. To avoid the use of a special package to house the serializer – due to the high frequencies involved – the ASIC is directly bonded to the PCB. The reference clock to the IC and the FPGA device is provided either from an external source or from an on board 40MHz-clock generator. The ASIC interfaces with the optical transmitter through a 50Ω transmission line that can also be used to drive the serial signal out of the board for electrical measurements. The role of the FPGA device is threefold: it is used to program the serializer test configuration, it monitors the serializer’s PLL locking state and it generates the test data patterns to be serialized. At the receiver end of the test setup a commercial receiver is used to de-serialize the incoming data and check for transmission errors.

4. EXPERIMENTAL RESULTS

At the time of writing, the IC’s had been received from the manufacturer only a few days before. This made it impossible to present here a complete set of measurement results. Nevertheless, tests were made on prototypes that proved the design to be fully functional. An eye-diagram of the electrical output signal is shown in Figure 6 (top trace). This eye-diagram was obtained during the transmission of a 256-bit long pseudo random bit sequence at 1.2Gbit/s. The measurement was made using an “HP CSA803” Communications Signal Analyzer with a SDL4 sampling head (17.5ps rise time). The jitter numbers are given in Figure 6 together with the details of the measurement (bottom trace and histogram).

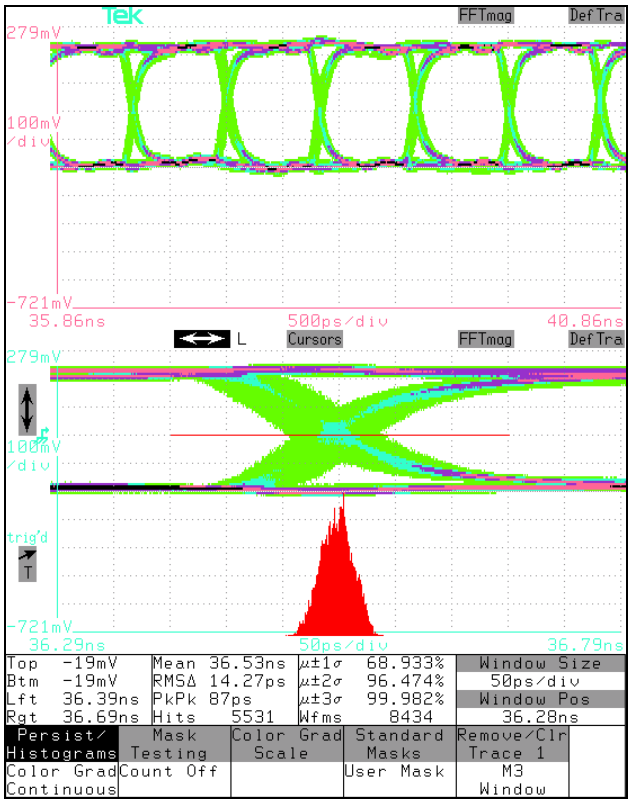

Figure 6 Eye-diagram for a 256-bit long pseudo random bit sequence at 1.2Gbit/s.

An optical transmission test was made using the test setup described previously, a commercially available receiver and de-serializer. The system was operated for 48 hours error free.

5. CONCLUSION

In this paper a 1.25Gbit/s serializer for use in HEP data and trigger links as been presented. The serializer was implemented in a 0.25μm CMOS technology using radiation tolerant layout techniques. The ASIC layout is pad-limited having a $4mm^2$ footprint area. The implementation constraints imposed by the radiation environment on the circuit design were addressed and the circuit architecture was discussed in detail. Two samples were tested and proved to be fully functional. The experimental results presented here constitute a small fraction of the tests required. To qualify the IC for use in the different LHC radiation hard environments, total dose and single event upset radiation tests are now in preparation. Future developments will be focused on system functionality, external interface and link protocol.

References

[1] C. Yang, R. Rad and M. Horowitz, "A 0.5-μm CMOS 4.0-Gbit/s serial link transceiver with data recovery using oversampling," *IEEE J. Solid-State Circuits*, vol. 33, pp. 713-722, May 1998.

[2] M. Kurisu, M. Kaneko, T. Suzaki, A. Tanabe, M. Togo, A. Furukava, K. Nakajima and Yoshida, "2.8-Gb/s 176-mW byte-interleaved and 3.0-Gb/s 118-mW bit-interleaved 8:1 multiplexers with a 0.15-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 31, pp. 2024-2029, Dec. 1996.

[3] G. Anelli, et al, "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects," presented at the 1999 NSREC conference, Norfolk, July 1999. Accepted for publication in the *IEEE Trans. Nuclear Science*, vol. 46, Dec. 1999

[4] F. Faccio, K. Kloukinas, A. Marchioro, T. Calin, J. Cosculluela, M. Nicolaidis and R. Velazco, "Single event effects in static and dynamic registers in a 0.25μm CMOS technology," presented at the 1999 NSREC conference, Norfolk, July 1999. Accepted for publication in the *IEEE Trans. Nuclear Science*, vol. 46, Dec. 1999

[5] F. Faccio, C. Detcheverry and M. Huhtinen, "First evaluation of the single event upsets (SEU) risk for electronics in the CMS experiment," *CERN CMS note 1998/054*

[6] J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1723-1732, Nov. 1996.

[7] I. Novof, J. Austin, R. Kelkar, D. Strayer and S. Wyatt, "Fully integrated CMOS phase-locked loop with 15 to 240 MHz locking range and ±50 ps jitter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1259-1266, Nov. 1996.