The APV25 Deep Submicron Readout Chip for CMS Detectors

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Abstract

The APV25 is a 128 channel analogue pipeline chip for readout of silicon microstrip detectors in the CMS tracker at the LHC. Each channel comprises a low noise amplifier, a 192 cell analogue pipeline and a deconvolution readout circuit. Output data are transmitted on a single differential output via an analogue multiplexer. The chip is fabricated in a 0.25 micron CMOS process to take advantage of the radiation tolerance, lower noise and power, and high circuit density which can be achieved.

1. INTRODUCTION

The CMS inner tracker contains approximately 10^7 channels implemented in silicon and gas microstrip technologies, read out by APV chips. For several years now these chips have been developed [1,2] to meet the demands of low-noise, low power and radiation hardness required for operation at the LHC. More recently it has been demonstrated that commercial deep submicron CMOS technologies currently available may exhibit radiation tolerance to levels in excess of those required [3], together with the possibility of operating with low noise and power consumption, as well as increased circuit density. Because of the potential for improvements we have embarked on a rapid development programme to produce a prototype APV chip in a deep submicron technology.

2. CHIP OVERVIEW

The APV25 chip has been designed in a 0.25 micron CMOS process and is very similar in concept to previous APV chips. It has 128 readout channels, each consisting of a 50 nanosecond CR-RC type shaping amplifier, a 192 element deep pipeline and a pulse shape processing stage which can implement a deconvolution operation to achieve the single bunch crossing resolution necessary at high luminosity. Analogue output samples are then multiplexed onto a single differential output for subsequent optical transmission to the DAQ system. The output data frame consists of these analogue samples preceded by a digital header which includes a digital address of the pipeline column from which the data originates. The chip can operate in one of three modes. In peak mode, following an external trigger, one sample for each channel (timed to be at the peak of the amplifier output pulse shape) is read from the pipeline and subsequently output through the multiplexer. In deconvolution mode, three samples per channel are read from the pipeline and combined in a weighted sum before output. In multi-mode a sequence of external triggers allows a number of consecutive pipeline samples to be transmitted in consecutive output data frames.
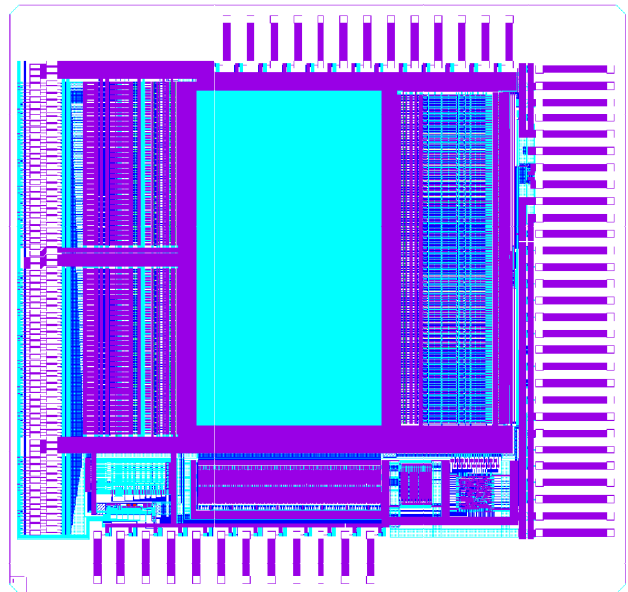

Figure 1. APV25 chip

The pipeline is used to store the amplifier outputs, sampled at the 40 MHz LHC frequency, while external trigger decisions are taken. The pipeline depth allows a programmable latency of up to 160 bunch crossings (4 microseconds) the remaining locations being used for buffering of data from up to 10 events (in deconvolution mode). For technological reasons the pipeline storage elements have been implemented using gate capacitance which allows a very dense layout for this memory array. The APV25 deep submicron CMOS chip contains all the necessary system features, including on-chip bias and calibration pulse generation, and a slow control interface for programming these features and the operating mode of the chip. The active chip area is approximately 7.2 x 6.5 mm^2. However due to its manufacture on a multi-project run, the die size is 8.2 x 8.0 mm^2.

3. FRONT END

The front-end electronics of the APV25 chip are essentially the same as those for APV6, but with slight modifications to optimise it for the deep sub-micron process characteristics
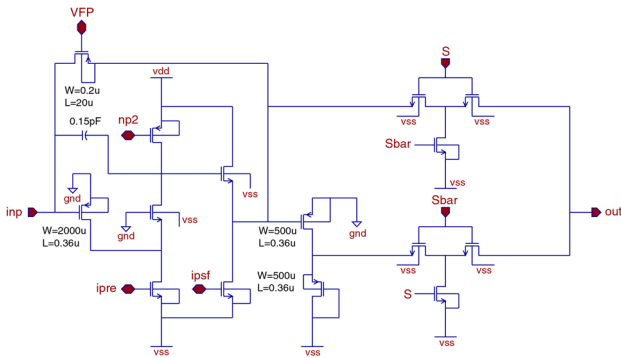
3.1 Preamplifier

Figure 2. Preamplifier Schematic

The preamplifier is a charge amplifier made from a single-ended folded cascode amplifier with a 150fF feedback capacitor. The pFET input transistor has a size of 2000 μm / 0.36 μm and is biased at 400μA. Its source is connected to GND to reduce power consumption. The output is buffered by a source follower which also provides the level shift required for DC stability through the feedback transistor. The feedback transistor also provides a discharge path in order to avoid excessive pile-up in the preamplifier. A switchable unity gain inverter is employed when detectors of opposite polarity are used to allow full use of the shaper dynamic range (limited by the 2.5V power supply). Feed-through is eliminated by pulling the centre of the switches to VSS when the switches are off. The preamplifier (including the inverter) has a gain of 18.7mV/mip (25 000 electrons) and a power consumption of 0.9mW.
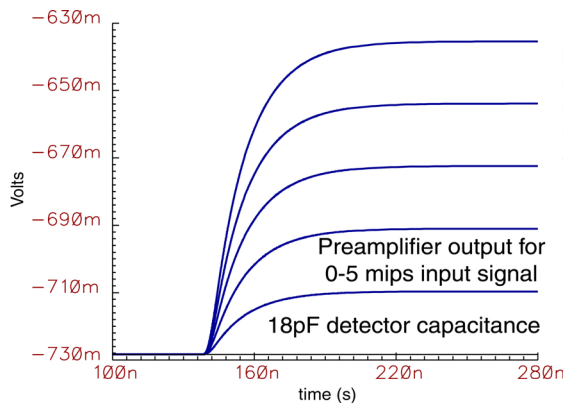

Figure 3. Response of Preamplifier

3.2 Shaper

The shaper is an effective CR-RC filter producing a 50ns shaped voltage pulse. The shaping is adjustable, over a limited range, to offset the inevitable degradation of the pulse shape which is caused by irradiation.
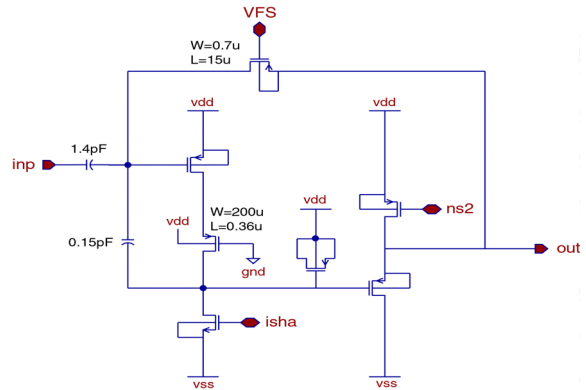

Figure 4. Shaper Schematic

The shaper is composed of a single-ended cascode amplifier (non-folded) with a feedback capacitor of 150fF and a coupling capacitor of 1.4pF. The pFET input transistor has a size of 200 μm / 0.36 μm and is biased at 48μA. The shaper has a power consumption of 0.25mW, giving a total front-end power consumption of 1.15mW. The total front-end gain is 100mV / mip with a non linearity of less than 2% over a 5 mip range.(measured at point **a** in figure 5, corresponding to the third samplet of the troplet used in *Deconvolution* mode).
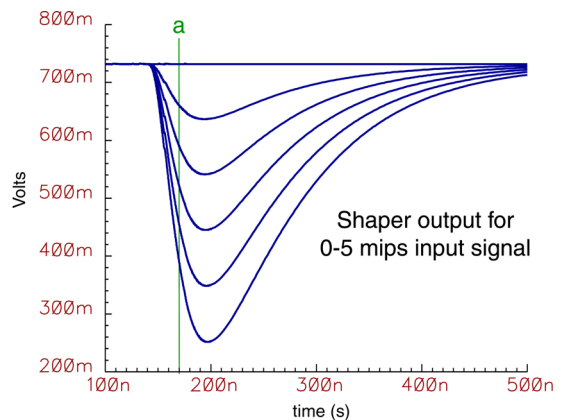

Figure 5. Response of Shaper (Hspice simulation).

3.3 Noise

By far the largest contribution to the front-end noise is the input transistor of the preamplifier. In simulation, the noise has been shown to be 246 electrons + 36 electrons / pF. With 18pF of detector capacitance, this gives 900 electrons of noise.

4. PIPELINE

The pipeline buffers data on-chip for sufficient time for the level 1 trigger to make a decision. Thanks to the smaller geometry of the deep sub-micron process the pipeline length could be increased from 160, in previous versions, to 192 thus increasing the maximum latency time up to 4μs. The FIFO depth (which determines the number of triggers which can be reserved for read-out at any one time) has also been increased from 20 to 32.

4.1 Analogue Memory

The pipeline consists of 128 channels by 192 columns of switched capacitor elements. One side of the capacitor connects to VSS and the other to the shaper output bus through a write switch, and the APSP input bus through a read switch. Due to a limit on the total area of metal-insulator-metal capacitors allowed within the chip, the pipeline capacitor has been implemented using the gate of a 7 μm x 7μm nFET (280fF). Given the DC operating point of the shaper output, the nFET gate capacitor is always in strong inversion which guarantees the best linearity for voltage to charge conversion.

4.2 Digital Control

The pipeline control sequences the writing, triggering, storing, and retrieval of data from the analogue memory. A write pointer continuously circulates the pipeline sampling the shaper output from each channel at intervals of 25ns. A trigger pointer follows behind the write pointer, separated by the trigger latency. When a trigger is received, depending on the mode of operation, either one, or three columns, marked by the trigger pointer, are reserved for reading out. Once reserved these columns cannot be overwritten until the data have been read out.

The column pairing present in previous versions of the chip (due to area limitations) has been removed. In addition, the time taken to release consecutively triggered columns in the pipeline, once they have been read, has been reduced. Latency error detection has also been improved from previous versions.

5. ANALOGUE PROCESSING

Signals from silicon strip detectors arrive at the inputs to the APV25 as single impulses of current which are integrated in the preamplifiers and then CR-RC shaped into well defined voltage pulses. These signals are then continuously sampled every 25ns, and the samples stored in the pipeline awaiting read-out.

In *Peak* mode one sample is reserved in the pipeline for reading out – this corresponds to the peak voltage of the CR-RC shaped signal. *Peak* mode is generally used when data rates are sufficiently low so that the effects of pile-up of detector signals are not significant. In this mode, the signal-to-noise ratio is maximised and the non-linearity of the signal is minimised. However, if pile-up does become

significant – at higher rates of data – then to sample just the peak of the signal is not enough since the CR-RC shaped signals will superimpose. In this situation, the chip is operated in *Deconvolution* mode.
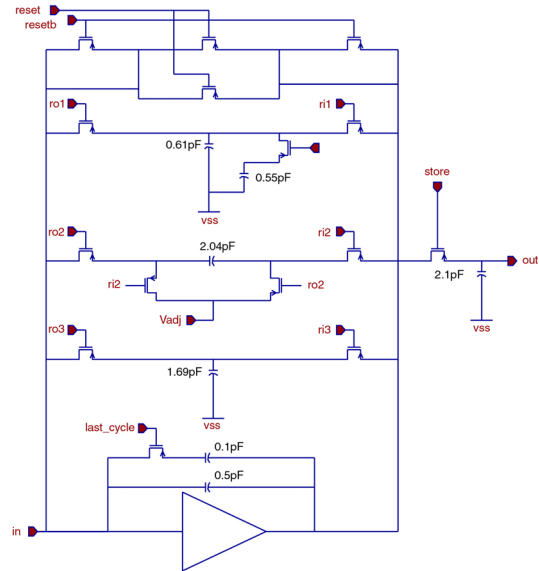

Figure 6. APSP schematic

In *Deconvolution* mode three samples are reserved in the pipeline. The third sample corresponds to the voltage at point *a* shown in figure 5 The second and first samples correspond to the voltages 25ns and 50ns (respectively) earlier. In order to determine which 25ns period the original signal occurred it is necessary to deconvolute the three samples. This operation is performed in the APSP (analogue pulse shape processor).
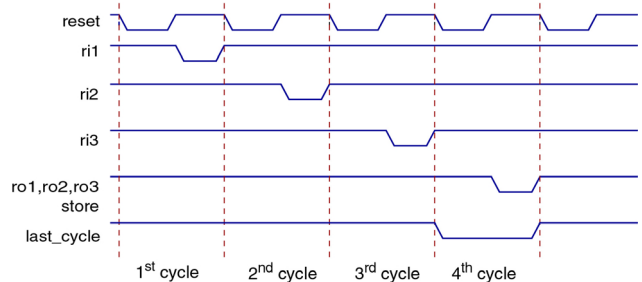

Figure 7. Timing of APSP in *Deconvolution* Mode

The APSP (figure 6) is a three weight FIR filter composed of a charge amplifier and a switched capacitor network. It is DC-coupled to the pipeline read bus and so the operating point of the charge amplifier is matched to that of the shaper.

The operation of the APSP in Deconvolution mode is shown in figure 7. The charge on each of the triggered pipeline elements is read out, in sequence (during the active low periods of *ri1*, *ri2* and *ri3*), integrated onto the APSP feedback capacitor, and the resulting voltages sampled on the three weighted capacitors. The charges

stored on these weighted capacitors are then summed (during the active low periods of *ro1*, *ro2* and *ro3*) and again integrated onto the feedback capacitor which has now been increased in size (using *last_cycle)* to reduce the gain. The resulting voltage is stored on the hold capacitor during the signal *store* (active low). This must be done while the analogue multiplexer is outputting the digital header. The DC output level of the resulting signal can be adjusted using the backplate bias *Vadj*.
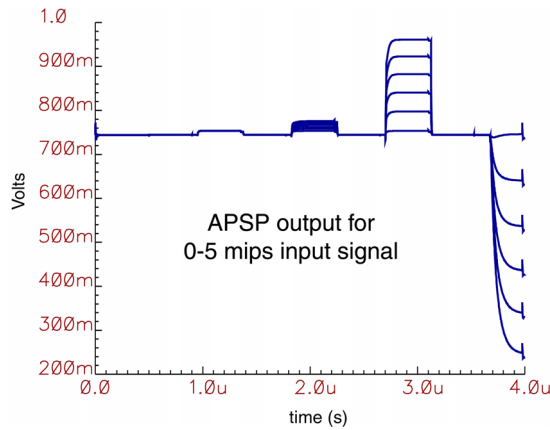

Figure 8. Output of APSP in Deconvolution mode.

Figure 8 shows the output of the APSP (before the hold capacitor) operating in *Deconvolution* mode. If the shaper signal is an ideal CR-RC shape then the first two samples should contain no signal. However it can be seen from figure 8 that there is a small signal in the second sample. This is due to a slight knee in the rising edge of the shaper signal, and this has been taken into account in the weighting of the APSP capacitors. The gain of the full analogue chain up to this point is 100mV / mip with a non-linearity of less than 2.11% over a 5 mip range.
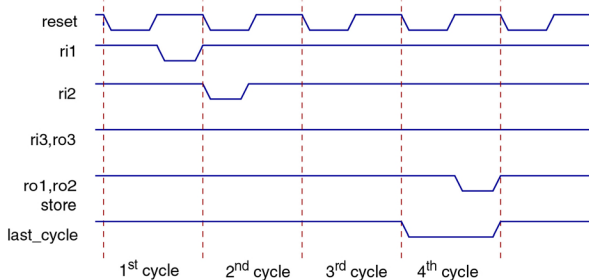

Figure 9. Operation of APSP in Peak mode.

The operation of the APSP in Peak mode is shown in figure 9. The charge stored in the single pipeline element is read out during *ri1*, integrated onto the APSP feedback capacitor and the resulting voltage sampled on the first of the weighted capacitor. During *ri2*, the APSP reset level is sampled onto the second weighted capacitor during *ri2*. The charges stored on these two capacitors are then summed and integrated on the APSP feedback capacitor (during *ro1* and *ro2*) The resulting voltage is sampled on

the hold capacitor during the signal *store*. As with Deconvolution mode, the DC output level of the APSP can be adjusted using the bias *Vadj*. This method of performing the Peak mode operation of the APSP differs from previous versions of the chip, but was implemented to ensure that in both Peak and Deconvolution modes the polarity of the output signal is consistent.
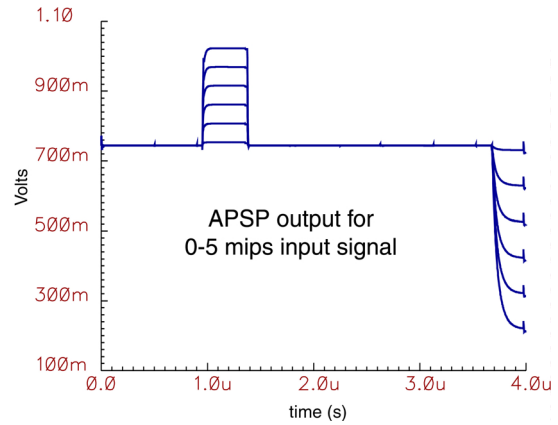

Figure 10. Output of APSP in Peak mode

Figure 10 shows the output of the APSP (before the hold capacitor) operating in Peak mode. The gain of the full analogue chain up to this point is 100mV /mip with a non linearity of less than 0.6% over a 5 mip range. The non linearity in Peak mode is better than deconvolution mode because in deconvolution mode the shaper signal is sampled on the rising edge which may be prone to slewing effects for large signals. The power consumption of the APSP is 0.2mW.

6. ANALOGUE MULTIPLEXER

The analogue multiplexer uses the same three level current mode architecture as with previous versions of the chip – with a few refinements. Firstly, the resistor used to convert the APSP voltage into a current has been made programmable with a choice of five values. This is to trim the multiplexer gain since the resistor value is only known to 20% accuracy. In addition, to overcome problems found in previous versions, channels which are not connected through to the output have their currents dumped into a load device. This is wasteful of power, but it ensures that channel readout does not affect the voltages generated on nodes within the multiplexer. The analogue gain at the output of the multiplexer is 100μA / mip. A digital header, which precedes the output of the data from the 128 analogue channels, takes the value of +/- 400μA (HI / LO respectively). With the input bias set to 50μA the power consumption is 22mW.
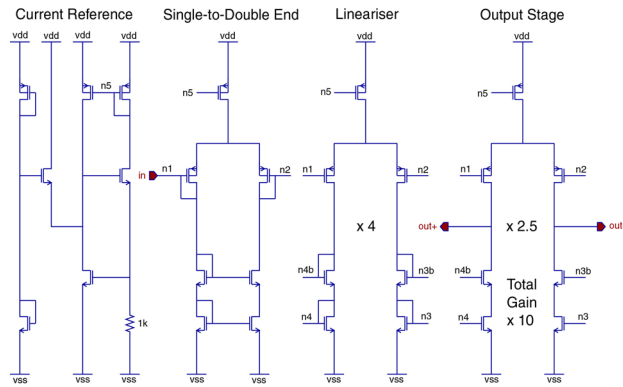
7. OUTPUT BUFFER

Figure 11. Schematic of output buffer.

The multiplexer output is converted into a differential bi-directional current by the circuit shown in figure 11. The output has an analogue gain of +/- 1mA / mip and a digital header of +/- 4mA (HI and LO respectively). The buffer has a power consumption of 20mW. Format of the data produced at the output of APV25 is shown in figure 12.

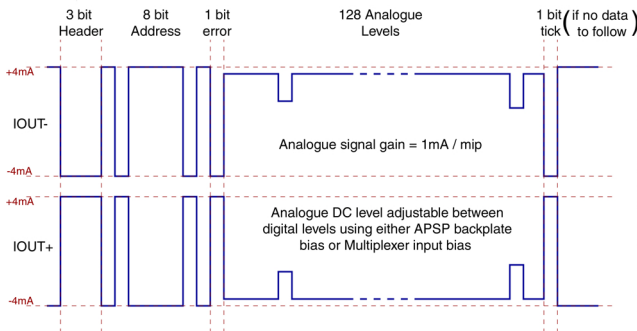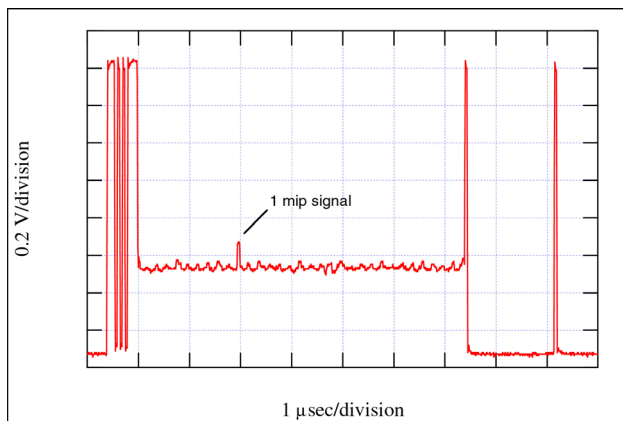**Figure 12.** APV25 data format.

8. RESULTS

Figure 13. Measured APV25 Readout Cycle

The APV25 was received back from fabrication immediately prior to submission of this paper and is currently under test. The chip is fully functional and initial results demonstrate it is working well as shown in figures 13 and 14.
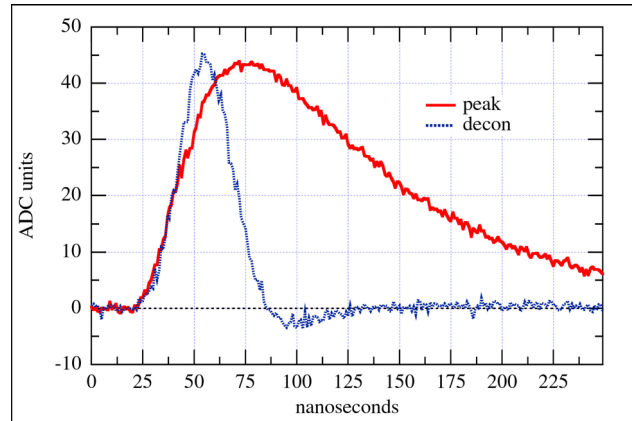

Figure 14. Measured APV25 Pulse shapes.

9. CONCLUSIONS

A new analogue pipeline has been designed in a deep sub-micron process. It is based on the APV6 with modifications which make use of the increased circuit density achievable using this process. Radiation tolerance to LHC requirements has been made using special design techniques, however SEU tolerance will not be achieved until the next version. Currently being tested, the APV25 is fully functional and radiation tests are imminent. Further information and test results can be found on http://www.rl.ac.uk/med/ .

10. ACKNOWLEDGEMENTS

11. REFERENCES

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[3] Total Dose and Single Event Effects (SEE) in a 0.25 micron CMOS Technology, F.Faccio et al, Proceedings of 4th workshop on electronics for LHC experiments, CERN/LHCC/98-36, 105-113.

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